

White-rabbit Network Interface Card (NIC) gateway

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White Rabbit Network Interface Card

- ▼ This project is concerned with the development of gateware and software to make the combination of a SPEC and a DIO mezzanine behave as a Network Interface Card (NIC) under Linux.
- ▼ Basic demo uses two SPEC boards, one configured as grandmaster and one as slave.
- ▼ Two simple use cases has been defined as basic demo.

Use case 1

- Simple transmission of PPS from the master to the slave, with nothing hooked to the external inputs of the boards.
 - The master is free-running. The master host reads system time and schedules a pulse output on the next UTC second. Then it gets an interrupt and from then on it schedules a pulse on each second.
 - The slave host does the same. Looking at the outputs on a scope we should see them perfectly aligned.

Use case 2

- ▼ Transmitting an external frequency in the 100 Hz range.
 - The user supplies a ~100Hz square wave on one of the inputs of the master card. The master host reads the UTC time of the rising edge of the external pulse upon IRQ. Then it adds a constant time (something like 1 ms) and sends a frame with that value to the slave.
 - The slave schedules a pulse to be produced at that time. On the scope we should see a constant time offset between the two pulses.

NIC project elements

Application

GN4124 drivers

FPGA gateway



We focus on this layer!

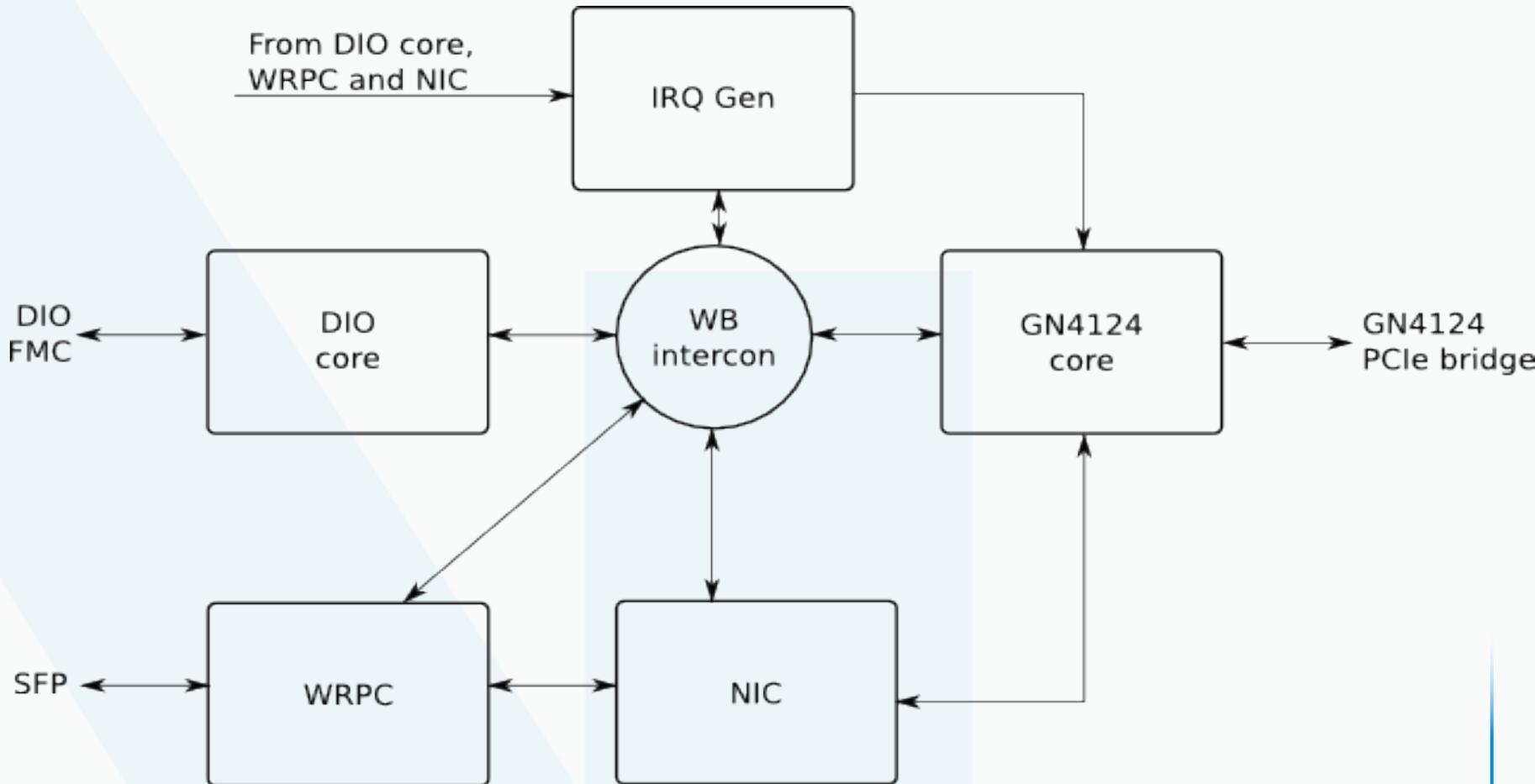
Software
(Linux PC)



Hardware
(SPEC + FMC-
DIO boards)



Basic on-chip architecture



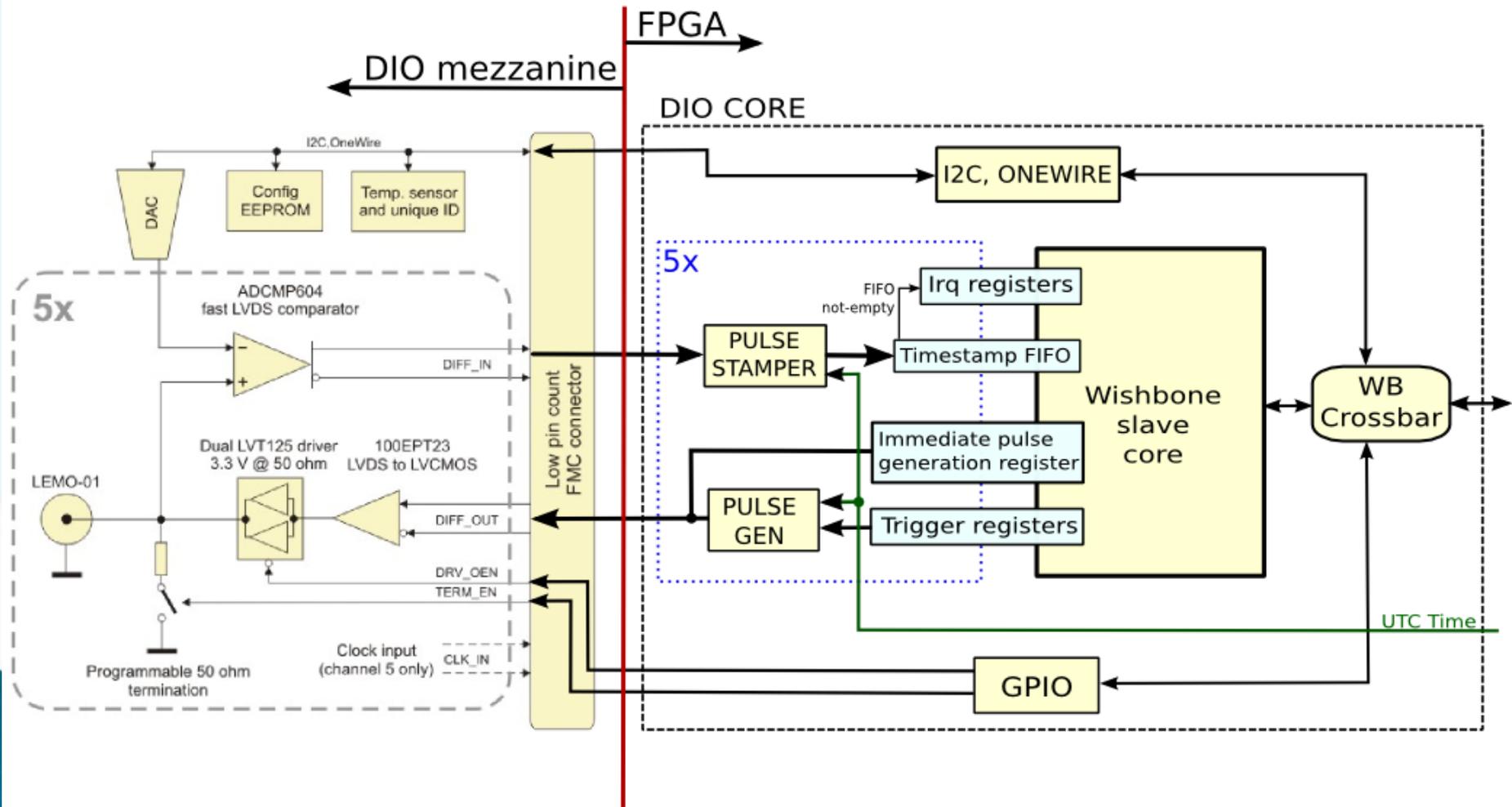
Network Interface Card elements

- ▼ The **DIO core** allows configuration of each one of the 5 channels of the mezzanine as input or output.
 - Inputs: accurate UTC time stamp for inputs and interrupt generation.
 - Outputs: schedule the generation of a pulse at a given future UTC time, or immediate generation.
- ▼ The **IRQ Gen** block receives one-tick-long pulses from other blocks and generates interrupt requests to the GN4124 core. It also includes interrupt source and mask registers.
- ▼ The **WB intercon** block ensures seamless interconnection of Wishbone masters and slaves using a crossbar topology.
- ▼ The **GN4124 core** is a bridge between the GN4124 PCIe interface chip and the internal Wishbone bus, allowing communication with the host and interrupts → PIPELINE VERSION!.

Network Interface Card elements II

- ▼ The **WRPC (White Rabbit PTP Core)** communicates with the outside world through the SFP socket in the SPEC, typically using fiber optics.
 - It deals with the WR PTP using an **internal LM32 CPU** running a **portable PTP stack**.
 - It forwards/receives non-PTP frames to/from the NIC block, using two pipelined Wishbone interfaces (master and slave for forwarding and receiving respectively).
 - It also provides UTC time to other cores, and time-tags for transmitted and received frames that can be read through Wishbone for diagnostics purposes.
- ▼ The **NIC core** ensures communication between the host and the WRPC.
 - It interrupts the host and provides a descriptor that the host can use to fetch incoming frames.
 - For outgoing frames, it receives a descriptor from the host, fetches the frame using PCIe DMA via the GN4124 core and sends it to the WRPC using a pipelined Wishbone interface.

DIO core architecture

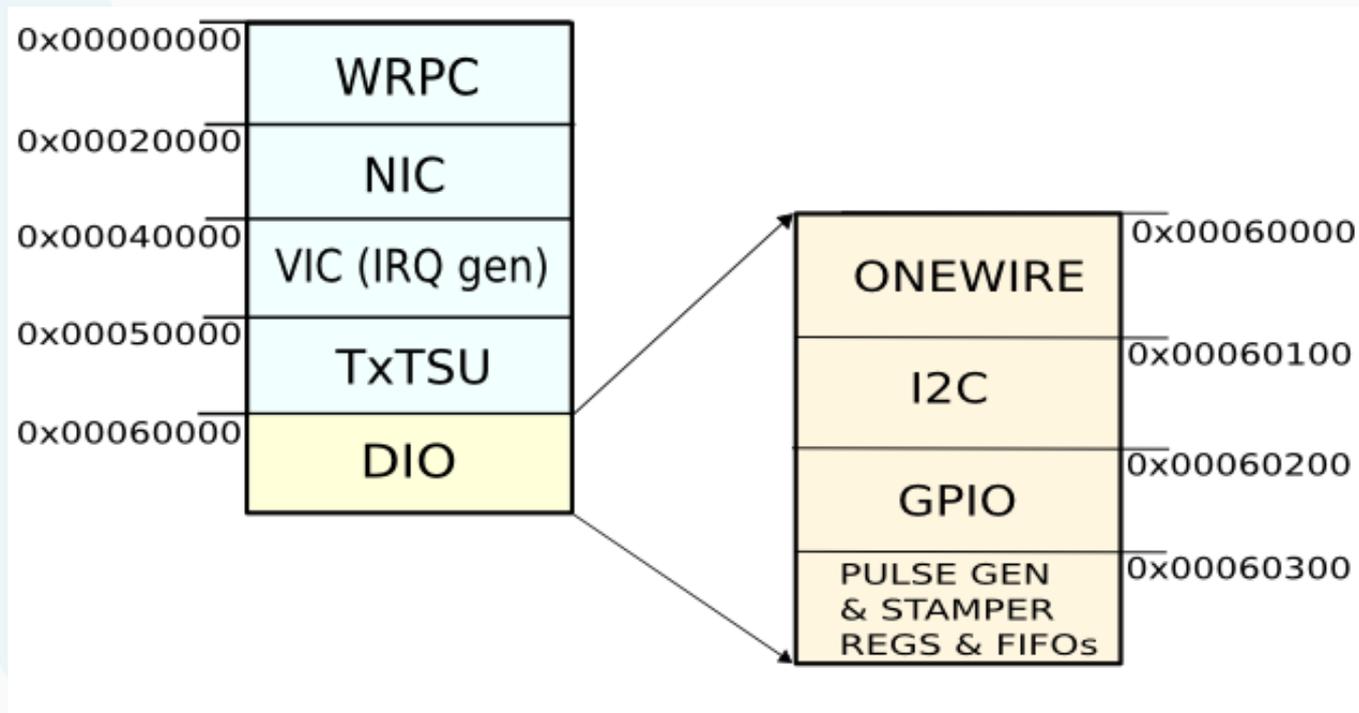


DIO core architecture II

- ▼ Modules to configure each single-bit port:
 - GPIO. It allows to enable/disable the output drivers and the termination resistors.
 - I2C. It allows to set the threshold of the ADCMP604 fast LVDS comparator and to access to write/read data to the EEPROM memory (24AA64).
 - Onewire for temperature adquisition
- ▼ Modules to generate or stamping pulses:
 - Pulse generator which produces a 1-tick-long pulse in its output when the UTC time passed to it through a vector equals a pre-programmed UTC time.
 - Pulse stamper which associates a time-tag with an asynchronous input pulse
- ▼ Wishbone slave core generated by wngen2 tool with:
 - Trigger registers (UTC-time-based for pulse generation)
 - FIFOs, to store the timestamps,
 - Interrupt registers, to configure the interrupts witch are generated when there are data in the FIFOs.
 - Monostable register, which generates a single clock cycle-long positive pulse when 1 is written to it. Used to immediate pulse generation on the output

DIO core memory map

- Within that memory space, the DIO core has mapped each one of the different modules that make up its architecture. Furthermore, any address within this memory space may be addressed by the PC to configure that modules (Onewire, I2C, GPIO ...).



Tool chain considerations

- ▼ Tool chain
 - HDLMake / Wishbone slave generator (pipelined)
 - Python scripts / SPEC driver
 - Git
 - Xilinx tool-chain under Linux (Chipscope!)
- ▼ Projects/tools versions (genum core, basic vs. pipelined cores, etc...)
- ▼ Global considerations
 - PROS: **Really powerful framework**, system design can be done really fast when elements are known → we are really impressed!
 - CONS: tools documentation need to be improved, It is really hard getting the whole system running!
Thanks to Tomasz!
- ▼ We will try to contribute providing feedback from our experience to make things easier to future users
 - I would really like the idea of using ohwr.org as repository for teaching!

Boards production

- ▼ Design is stable (includes latest Tomasz's modification)
- ▼ Test
 - PTS for SPEC already available
 - PTS for FMC-DIO almost finished (ready begin next week).
- ▼ Production chain established. Boards already checked by third-party partners, 7S and CERN and fulfilling IPC-610-2
- ▼ CE certification
- ▼ Boards ordering is open.

Final summary

- ❖ Current HDL is finished.
 - Available on “Tomas-fixed” branch.
 - Test software done based on Python scripts
 - Require final applications for complete gateway testing.
- ❖ Other tasks
 - Preliminary documentation available but need to be improved.
 - HDL testbench (genum BFM model included, work in progress).
- ❖ Board production is ready to customers

Thank you for your attention

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