



FmcDac 1

An informal description of the design

Maciej Fimiarz

August 16, 2010

Abstract

FmcDac1 is a 4 channel 16 bit 10 MS/s DAC card with internal/external trigger in FMC (FPGA Mezzanine Card) format

1. Project requirements

Maximum output update rate:	10 MSPS
Resolution:	16 bits
Output voltage range	± 10 V
Output impedance:	programmable (0 / 50 Ohm)
Board size:	low pin count FMC (FPGA Mezzanine Card)
Triggering:	separate START / STOP signal, TTL levels
Voltage stability, DNL, INL:	see p. 3
Clock:	internal clock for low jitter operation

2. Step-by-step requirements explanation

Maximum output update rate

It is possible to find a DAC with SPI interface, having excellent stability and being very easy to use, but with the speed limited to about 1 MSPS. On the other hand, there are many DACs available with output update rates exceeding 100 MSPS. Their SNR and linearity is much worse and the prices are higher. I have experienced difficulties finding a converter which would match the requirements of the project adequately (where, for example, high sampling rate is not achieved at expense of linearity).

On OHWR web page, there is an [pdf document](#) with comparison of DACs potentially suitable for the project.

Resolution

Nowadays, it is easy to find a cheap, 16-bit DAC with good linearity.

16 bits resolution with ± 10 V output voltage range means that the output value changes with step of 0.305 mV. Therefore, DAC zero offset and offset voltage and thermal stability of the output amplifier must be comparable.

Output voltage range

The DAC output drive strength is not enough to provide full range of required voltages (± 10 V), especially on 100 Ohm load (50 Ohm termination + 50 Ohm destination's impedance). Therefore, a separate output driver must be used.

Supply voltage of the output buffer must be high enough to allow the output stage to achieve required linearity in full ± 10 V range. +12 V is available directly from the carrier (and may be sufficient, provided the saturation voltage of the buffer output stage is less than 2 V at $R_L = 100$ Ohm). Negative supply voltage must be generated onboard by a switching converter. Due to high output voltage range, noise shouldn't be a problem as long as the PCB is properly designed.

Output impedance

For the output impedance of 50 Ohm (which in case of perfectly matched load, means 100 Ohm total resistive load of the output amplifier), the highest possible output current is ± 100 mA (for output voltages of +10 V / -10 V). In case all the channels are set up to the same output value, total output stage current exceeds 400 mA, hence amplifiers' circuit power consumption needs to be taken into consideration as well.

Summarizing, each output must be capable of delivering 100 mA continuous current. The outputs must also be able to withstand a short circuit where the output current can be twice as big. Saturation voltage should be as low as possible to simplify the power

supply and reduce the power dissipation. Naturally, distortion level and noise still need to be small enough to not degrade 16 bit DAC performance.

Board standard: FMC

The power dissipation capacity of an FMC card is very limited, so the power dissipation of the DAC and output driver must be as low as possible. For FmcDac1 design, however, this shouldn't be a problem as long as the components producing significant amounts of heat are properly distributed on the circuit board.

Numerous communication lines (34 pairs) allow to use a DAC having simple parallel interface with CMOS/LVTTL levels.

Triggering

The only problem I've encountered is the space limitation on FMC front panel. The card has 4 outputs and 2 trigger inputs which can't be fitted using separate SMC connectors. Camera-link or similar interface must be used. Removing one of the trigger inputs would allow us to use SMC sockets.

Voltage stability, DNL, INL

As mentioned before, the INL and DNL of a DAC decrease with growing update rate. For Analog Devices' AD5547 DAC, DNL is < 0.3 bit and INL < 0.5 bit. The parameters of another DAC which could be potentially used in FmcDac1 – MAX5895 (500 MSPS): INL is 1 bit, DNL is 3 bits. This is the price of the output speed which is unnecessary for this application.

Clock

The sampling clock taken directly from the FPGA would have too big jitter to directly drive the DAC. FmcDac1 has an internal 40 MHz clock oscillator, and the clock can be divided by any integer value inside the carrier FPGA. A single D flip flop is used to reduce the jitter generated by the FPGA divider.

It is possible to use a VCXO to allow the card to be synchronized with an external clock (*to be discussed*).

3. Power consumption and heat dissipation

A word about the power supply

To keep the number of voltage regulators low (in particular, switching regulators), +12 V available from the carrier should be used as the positive supply for the output amplifier. Negative supply voltage must be provided by a switching regulator. There is no need for a low noise regulator and a simple inverting buck regulator, such as **type** should be sufficient. Below is a simple calculation of power supply requirements:

The maximum current needed by one output in the worst conditions is about 100 mA. The output impedance of the amplifier must be increased by adding serial resistor (~ 50 Ohm). In such conditions, the voltage drop is:

- 5 V at the load,
- 5 V at the resistor (perfect matching), $5 \text{ V} * 100 \text{ mA} = 500 \text{ mW}$
- 2 V at the output, $2 \text{ V} * 100 \text{ mA} = 200 \text{ mW}$

so the minimum power delivered by the supply is 1200 mW for a single output, and about 5 W for entire card.

The output buffer operates under worst power conditions, when the power matching is the best. It means that for 12 V supply, there is 6 V on the load (50 Ohm series termination resistor + 50 Ohm load resistance). $6V / 100 \text{ Ohm}$ gives 60 mA, so the amplifier would dissipate $6 \text{ V} * 60 \text{ mA} = 360 \text{ mW}$.

DSL line drivers are convenient and cost-effective choice of an such an output stage - they are cheap and easy to obtain. But because of the power dissipation, not all of them are suitable – the maximum power dissipation of the package must be checked.