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**FMC Delay 1ns 4cha
Technical specification**

v1.2

Introduction

This document gives information about the hardware part of the FMC fine delay card.

The card uses 2 principles for programmable pulse delay:

- incoming pulse time-stamping realised by the TDC-GPX-FG chip
- generation of 4 individually delayed pulses using counters inside FPGA and fine delay chips (FDC).

In order to assure low jitter, dedicated clock generation and distribution chip was used.

Since delay of fine delay chip is process and temperature dependent, the TDC can be used for its calibration as well.

Time-stamping

The input signal (LVTTTL) is fed to the level converter (Fig. 1). Polymer fuse is used as overcurrent protection. When input current exceeds 100mA longer than a few seconds, the fuse heats up and limits the current. D5 and D6 serve as over-voltage protection and current path when over-current condition occurs. R41 is a pull-down which defines low level when input is disconnected.

Termination mode is selected using on-board jumper or by software and is indicated by one of two front panel LEDs.

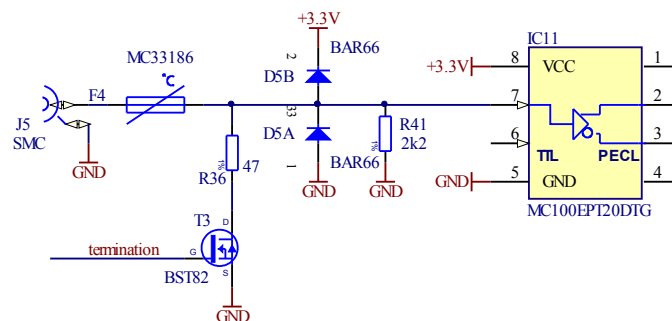


Fig. 1: Level converter

The TDC (Fig. 2) works in R-mode. This ensures 40MHz throughput per channel. TDC is driven by 125MHz/4 clock. This mode ensures 27ps resolution.

Input pulse triggers measurement, while rising edge of 125 MHz clock stops it. According to the datasheet, such clock rate fits within acceptable range (180MHz).

The TDC external voltage regulator IC6 is recommended by producer of the chip. IC5 was added due to previous experience with one. It ensures faster lock-in and more stable operation.

Communication with TDC is done over 28 bit parallel bus. Since TDC accepts LVTTTL levels, it is possible to directly cooperate with 2.5V LVCMOS FPGA defined by FMC specification. The FPGA pins must be switched to single-ended mode. Since Spartan 6 is used on the carrier board, this can be done from firmware-level.

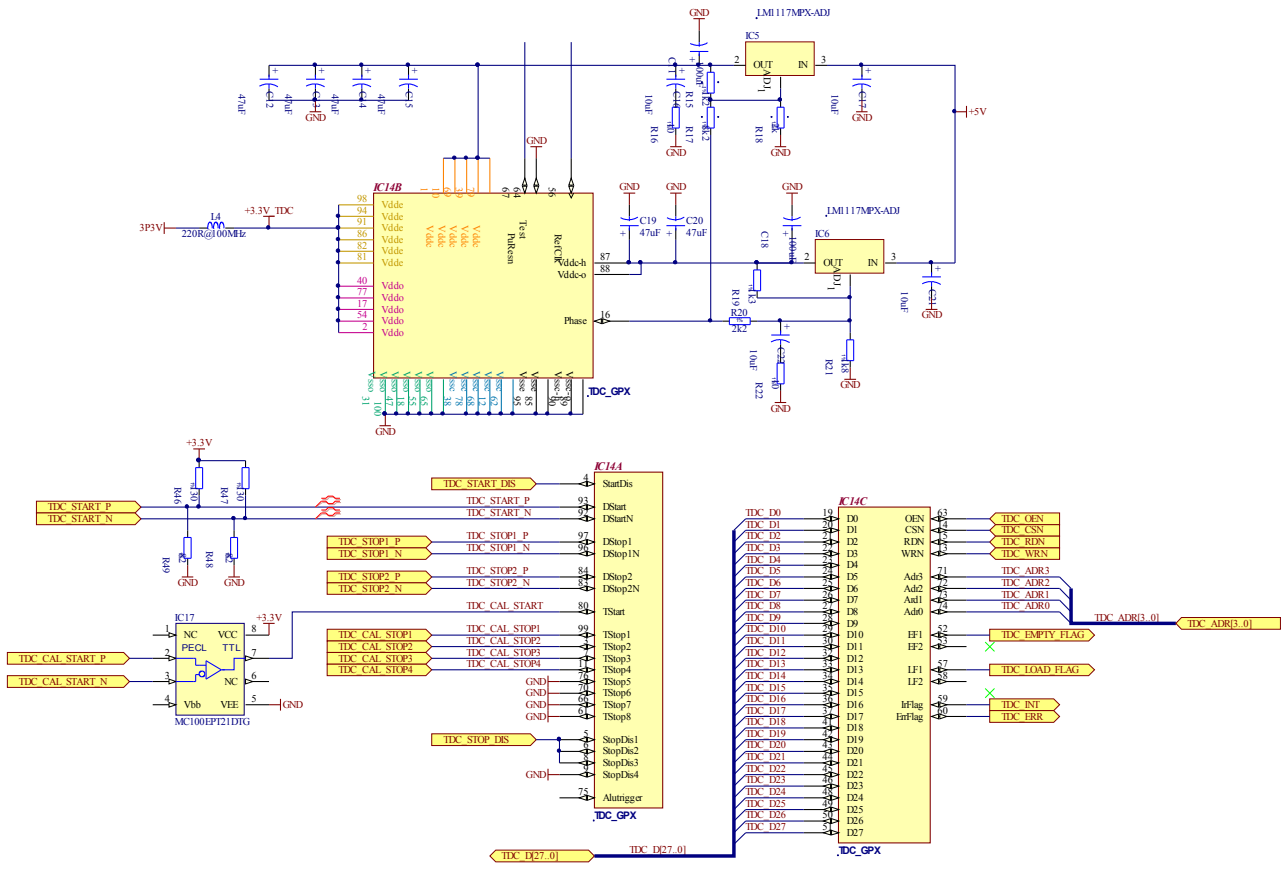


Fig. 2: TDC

The trigger input need to be fed to the FPGA as well. Since TDC measures relative time only, with respect to the clock edge, FPGA needs to calculate its absolute position. To facilitate time-stamping, lower frequency (125/4) clock can be applied to STOP2 input of the TDC and IO pin of the FPGA. Then each trigger would have 2 time stamps – one with respect to 125MHz clock, second with respect to 125/4 MHz clock.

Pulse generator

Pulse generation is based on two principles : coarse FPGA calculation and external fine delay (FDC).

The TDC value is passed to the FPGA which quickly calculates the clock cycle number and fine delay chip value to be written to the TDC. After coarse number of cycles, FPGA generates pulse which is delayed by the FDC. In order to decrease the FPGA jitter and to make sure that FDC is synchronised with same clock edge as TDC, external D-Flip-flop (IC4) was used (Fig. 3). The FDC range is 2.5..12ns, so it covers full 8ns (125MHz clock) period. IC8 converts the LVPECL signal to LVTTTL, required by output buffers.

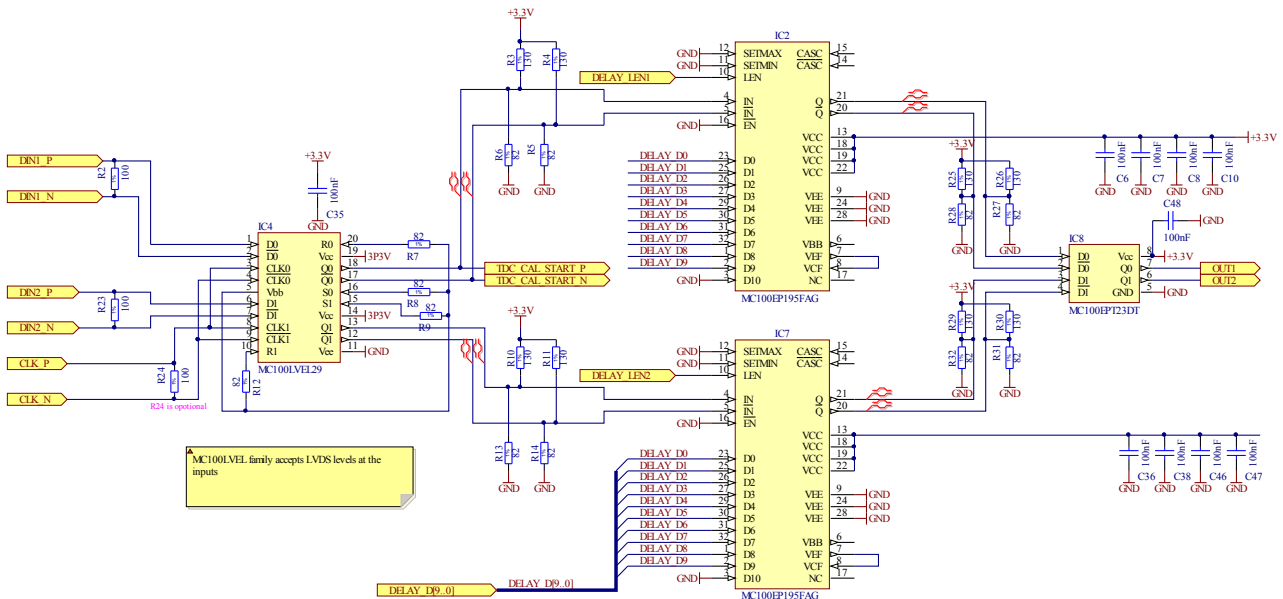


Fig. 3: Fine Delay Chip section

The output buffers (Fig. 4) perform following functions:

- ensure low output impedance
- over-voltage and over-current protection
- disconnect mode with output low level
- output for calibration circuit

Low output impedance is achieved by parallel connection of 2 line drivers. It ensures over 50mA of output current capability. F1..F5 polymer fuses are used to protect against too long short circuit and too high voltage connected to the output. BAR66 diodes are used to bypass excessive current. IC18 and reset circuit makes sure that IC9 is disconnected from the load during power-on phase, where some transients could occur.

Second, identical buffer (IC19) is used to deliver calibration pulses to the TDC. This enables possibility of on-fly calibration of whole delay chain.

The only problem is that TDC PECL input is already used as trigger source. There was installed converter from LVPECL to LVTTTL. It adds some delay which needs to be compensated.

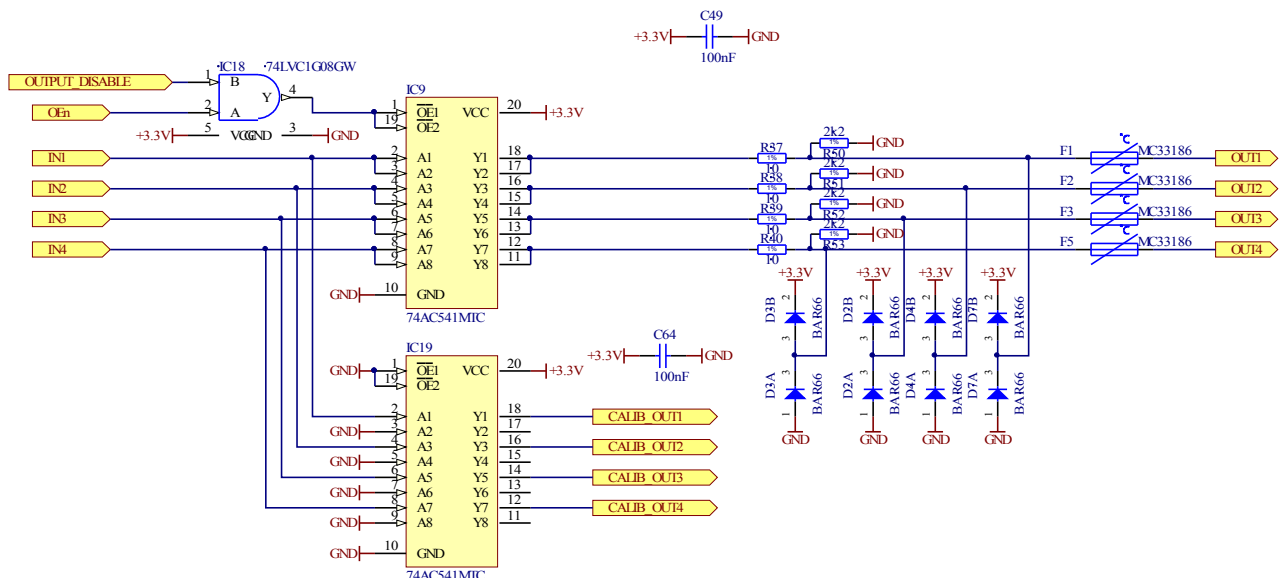


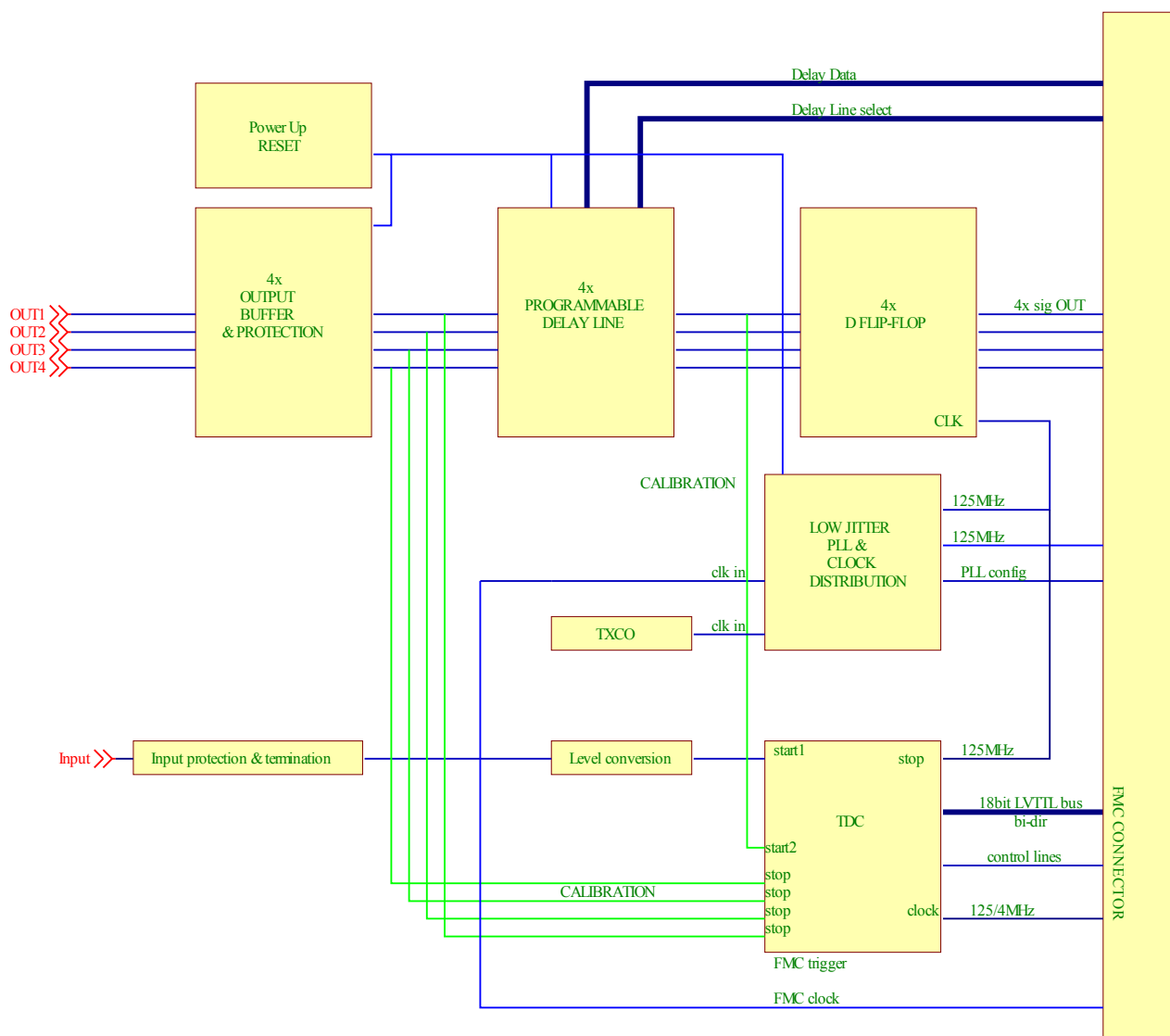
Fig. 4: Output buffers

Time base

Since it cannot be guaranteed that all possible FMC backplanes are able to deliver high quality clock, there was embedded low jitter generator. It can be synchronised to the external clock source and used to clean high jitter clocks. When no external clock is available, it is able to run from internal crystal generator or on-board TCXO. The chip delivers two outputs – one is routed to the TDC and output D flip-flop, second to the FPGA chip.

In order to prevent during power-up generation of something at the output, there is voltage supervisor which puts the output buffer into Hi-Z until all voltages are stable + 200ms.

Fine delay card block schematic



Release history

1.0 – first preliminary specifications

1.1 – added block schematic

1.2 - added detailed description + schematics