White Rabbit clock synchronization: ultimate limits on close-in phase noise and short-term stability due to FPGA implementation

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***Abstract*—This article investigates the ultimate limits of White Rabbit (WR), an high-accuracy time distribution system based on FPGA. The knowledge of such limits is essential for new emerging applications that are evaluating WR. In this article, we identify and study the key elements in the WR synchronization: the Digital Dual Mixer Time Difference phase detector and the Gigabit Ethernet transceiver. The benchmarks and experimental analysis of these key elements allow us to determine the WR Switch performance limits and evaluate their evolution with newer FPGAs. The identified performance limits are achievable by the present-day generation of WR Switch. The ultimate limits of short-term synchronization performance due to FPGA implementation have been derived through analysis and then demonstrated using the existing WR Switch enhanced with an additional daughter-board. This combination (WR Switch and daughter-board) achieves a tenfold improvement in terms of phase noise, jitter and short-term stability with respect to the current WR performance. Both phase detectors and Gigabit transceivers have a similar phase noise contribution equal to a short-term stability of MDEV 4E-13 at τ=1 s (dominated by flicker PM noise).**

Keywords—Synchronization, Synchronous Ethernet, PTP, IEEE 1588, Phase noise, Allan Deviation, Stability, PLL, Oscillator, Time transfer, Frequency transfer, Optical link.

I. INTRODUCTION

The White Rabbit (WR) project [1] is a multi-laboratory, multi-company, and multinational collaboration to develop a versatile solution for control and data acquisition systems where sub-nanosecond synchronization accuracy is required. Since its inception, WR has expanded beyond its initial application in accelerators. Newly emerging applications of WR require better synchronization performance than currently achievable. In this article, we investigate the ultimate limits of WR performance achievable respecting the design choices of the current WR implementation. We start with an introductory section that provides an overview of the WR project, describes the basic technologies employed in WR, and outlines WR applications focusing on the applications that need better performance.

The WR project started within an effort to renovate the accelerator control and timing system at European Organization for Nuclear Research, CERN. The project's initial aim was to develop a technology that fulfills CERN's stringent requirements, ensures longevity and entails commercial support. In this view, WR is based on widely-used standards and an open-source paradigm for the development of hardware, FPGA firmware and software. The open-source paradigm means that all the sources are available online. Openness facilitates collaboration and encourages new contributions while standards make solutions flexible, reliable and stable. In a short time, the number of WR applications grew beyond initial expectations while WR open-source devices became commercially available.

WR found many applications at CERN as well as outside of accelerators. At CERN, WR applications include distribution of magnetic field [2], diagnostics of the Large Hadron Collider (LHC) [3] and synchronization in neutrino experiments [4]. In the future, WR is considered for distribution of radio-frequency signals to control accelerating cavities [3]. Other accelerator facilities that use or evaluate WR include GSI in Germany [5] and ESRF in France [6]. Outside accelerators, WR is used to synchronize large distributed acquisition systems [7], such as cosmic ray observatories in Siberia [8] and China [9]. The national time laboratories in France [11], Finland and Netherlands [10] are evaluating WR for long-distance time-transfer and dissemination of Coordinate Universal Time (UTC). WR is also evaluated for space-related applications such as radio-frequency distribution for ground-based space-tracking stations [12]. It is the requirements of the national time laboratories and the radio-frequency distribution that push the limits of WR synchronization performance.

The national time laboratories provide the reference for time and frequency to institutions and compare their UTC realizations with that of other national laboratories in a common effort to calculate the global UTC. Such applications require very high stability of short-term and long-term synchronization performance in order to time transfer highly-stable frequency standards such as Hydrogen Maser (H-Maser) clocks. Notably, the current short-term stability performance of WR is a few orders of magnitude worse than that of an H-Maser clock which affects the application of WR in comparison of such frequency standards. Therefore, metrological institutes ask for an improved short-term stability of WR time-transfer [13].

The navigation and control of spacecraft requires the use of several ground stations, sharing the same knowledge of time through a time and frequency distribution network. The distance between spacecraft and the stations is measured through two–way ranging, which is based on the measurement of round-trip delay of a radio signal. Due to the propagation delays involved in deep space applications, both NASA and ESA requires very high stability for observation time from 10 s to 10000 s [12]. Notably, the current generation of WR Switch (WRS) cannot fulfill short-term stability requirements.

Time in WR is transferred from the time-reference over a WR Network that consists of WRSs – the keys component of any WR installation. The short-term performance of WR time-transfer directly depends on two design choices of the WRS: the use of an FPGA-based phase detector and the use of FPGA-based Gigabit transceivers. Other sources of uncertainty are the electro-optics and optics components. The WR project suggests a Gigabit Ethernet compliant small form factor pluggable optical transceiver (SFP) and an ITU-T G.652 single-mode optical fiber [14]. The uncertainty

contributions due to SFP's laser diode stability over temperature [15] and optical fiber chromatic dispersion stability over temperature [15] are not considered in this article. The magnitude of these contributions depends on the specific WR installation and on the optical fiber length. Using the suggested SFP and optical fiber (length up to 10 km), these contributions do not affect the short-term performance of WR time-transfer. Notably, the phase noise introduced by the suggested SFP is negligible [16].

In this article, we investigate and demonstrate the ultimate limits of WRS performance introduced by its FPGA implementation. We first shortly describe in section II the principles of WR operation. In section III, we introduce two essential building blocks of the White Rabbit implementation: the phase detector and the Gigabit Ethernet transceiver. We describe the generation and distribution of Layer 1 (L1) clocks that use the described building blocks in the WRS in section IV. Evaluation of White Rabbit performance limits requires understanding the contributions of these two important elements, phase detector and Ethernet transceiver, in terms of additive phase noise and short-term stability. In sections V and VI, we analyze these contributions in the current WRS implementation and conclude what are the limits of their optimization. In section VII, such analysis is confirmed by using a specially designed Low-Jitter Daughterboard that improves close-in phase noise and stability of the White Rabbit time and frequency transfer to the measured limits. We conclude in section VIII, claiming that any further improvements in terms of short-term performances are possible only using high-stability local oscillators combined with a reduced control loop bandwidth. Notably, for applications such as clock comparison, a reduced bandwidth may negatively impact comparison results for observation time less than the control loop time constant.

II. Overview of White Rabbit Time Transfer

All WR applications benefit from the sub-ns accuracy of synchronization that can be attributed to the WR extension to Precision Time Protocol (WR-PTP [17]) and its clever FPGA-based implementation described in [18]. While staying compatible with the PTP standard, WR PTP complements PTP with two ideas: physical Layer 1 (L1) syntonization and phase detection.

A WR Network is a PTP Network that consists of a Grandmaster (GM), Boundary Clocks (BCs) and Ordinary Clocks (OCs). In such a network, depicted in Figure 1, the GM is usually a WR Switch connected to a time reference, for example, a Global Navigation Satellite System (GNSS) receiver and/or frequency standard. This time reference is distributed by BCs (WR Switches) from the GM to all the OCs (WR Nodes) in a hierarchical tree-like topology. In typical PTP implementations, the time and frequency of local clocks in all the BCs and OCs are synchronized to that of GM using periodic exchange of PTP messages, by default every second. This means that the accuracy of synchronization greatly depends on the quality of local oscillators and thus their stability during and between PTP message exchanges. The WR uses L1 syntonization for frequency synchronization (syntonization) and the exchange of PTP messages only for synchronization of the time counter and phase-alignment.

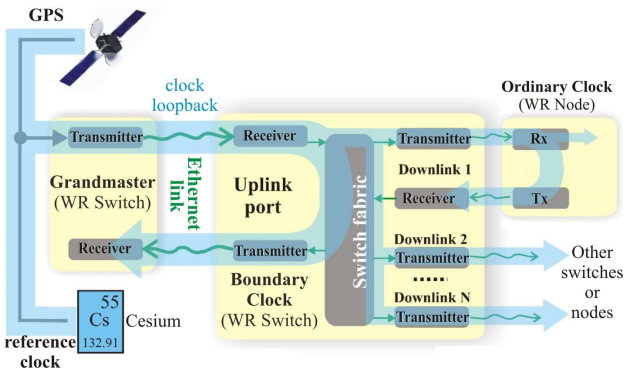

Fig. 1 - WR-PTP network.

L1 syntonization, used also in Synchronous Ethernet, distributes a physical clock signal (frequency) in the data stream. On a link between two devices, the master device encodes the transmitted data using its local clock signal. This clock signal is recovered from the received data by the slave device, downstream the network hierarchy. This device uses a jitter cleaned copy of the recovered clock to encode the data it sends. This process is repeated in a hierarchical manner on all links in the WR network providing a network-wide traceability of frequency to a common reference. Importantly, unlike in typical PTP implementations, in WR devices the quality of L1 syntonization has a substantial impact on the performance of synchronization [19].

In WR implementation, the L1 syntonization is inherently connected with clock signal recovery from data stream and phase detection. As depicted in Figure 2, Gigabit Ethernet transceiver decodes the "L1 RX clock signal" from the data stream. This signal is an input to the WR Phase-Locked Loop (WR PLL) that is based on phase detection. The WR PLL allows programmable phase shift between the two syntonized clocks: the recovered L1 RX clock signal and the Local PTP Clock. Moreover, on each link, there exists an L1 syntonization frequency loopback. Unlike in Synchronous Ethernet, in WR this frequency loopback is used. It allows enhancing the precision of timestamps from nanoseconds to picoseconds using phase detection.

The Digital Dual Mixer Time Difference (DDMTD) phase detector and the Gigabit Ethernet transceiver are implemented in FPGA. Both elements are required on all 18 ports of the WRS that uses the Xilinx Virtex-6 FPGA (XC6VLX240T). Additionally, WR implementation requires two local voltage controlled oscillators (VCXO) for its operation. The performance of these three building blocks has a direct influence on the performance of L1 syntonization and thus accuracy of synchronization. These elements are described in details for the WR Switch in the next section

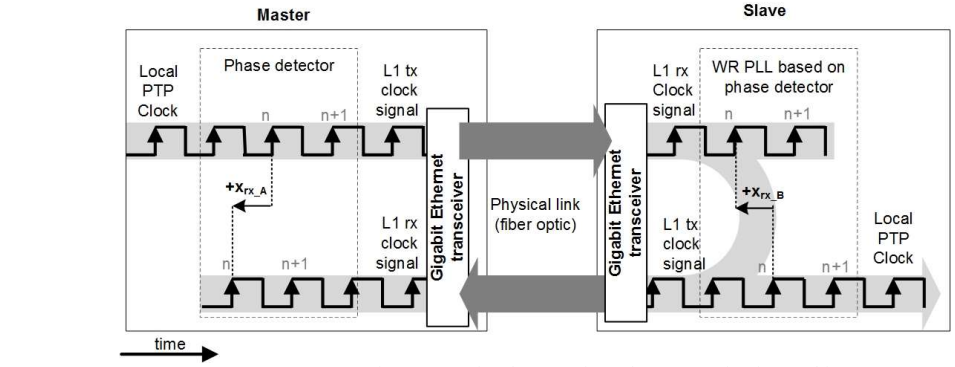

Fig. 2 – WR implementation of L1 syntonization and its frequency loopback

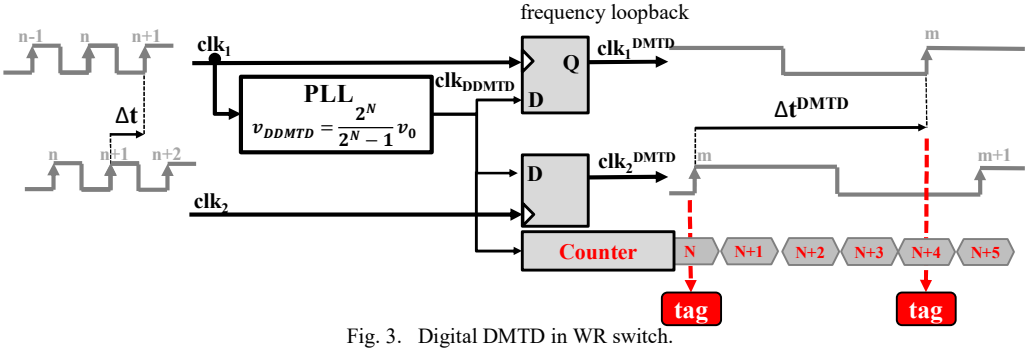

Fig. 3. Digital DMTD in WR switch.

III. BUILDING BLOCKS OF WHITE RABBIT SWITCH IMPLEMENTATIONS

A. DDMTD Phase Detector

A phase detector is a key element in any network that uses L1 Syntonization, such as Synchronous Ethernet and WR networks. In such networks, a phase detector is a part of a Phase-Locked Loop (PLL) that adjusts the frequency of the Local Oscillator (LO) with respect to the frequency recovered from the data stream. Additionally, in WR a phase detector is also used to enhance the precision of timestamps. The phase noise contribution of the phase detector propagates in the synchronization chain and therefore its implementation is crucial in highly accurate and precise time-distribution systems, such as White Rabbit.

WR requires a precise phase detector on each port of the WR Switch (WRS). With 18 ports in the WRS, an implementation that does not require external hardware for each port is preferred. The phase detector used in the WRS is based on the modified version of the Dual Mixer Time Difference technique (DMTD) [20].

The idea behind DMTD is to reduce the frequency of two input clock signals without affecting their phase relationship. In order to achieve that, the original DMTD performs analog mixing to demodulate the input clocks using so-called *DMTD clock signal* clk_{DMTD}. The *DMTD clock signal* is common to both input clock signals and has a frequency close to their frequency. As a result of mixing, the output clock signals have much lower frequency and the phase offset between them can be easily measured with a time-interval counter. Since the phase relation in radians between input and output signals is preserved, the phase offset expressed in time between the input clock signals can be easily calculated knowing the phase offset between the output clock signals.

WRS implements an FPGA-based version of the DMTD, called the Digital DMTD (DDMTD)[21][22]. The DDMTD uses a digital implementation of the analog mixing operation performed by D-type flip-flops, clocked by the *DMTD clock signal,* clk_{DMTD}, as shown in Fig. 3.

The *DMTD clock signal* clk_{DMTD} is generated from one of the input clocks (clk_1in Fig. 3) using a PLL. The frequency of clk_{DMTD} is specified as follows:

$$v_{DMTD} = \frac{2^N}{2^N - 1} v_0 \quad (1)$$

where N is an implementation-specific value that is 14 in the WRS and v_0 is the nominal frequency of the input clock.

The sampling operation performed by the flip-flops is similar to analog mixing. Therefore, the output clock signals clk_1^{DMTD} and clk_2^{DMTD} have a frequency equal to v_{DMTD}-v_0.

The phase offset between the input clock signals clk_1 and clk_2 is Δt (expressed in seconds); it is increased by the zooming effect of DMTD, as shown in (2).

$$\Delta t^{DMTD} = \Delta t \cdot \frac{v_0}{v_{DMTD} - v_0} \quad (2)$$

The phase offset Δt^{DMTD} is measured by a counter that timestamps each rising edge of clk_1^{DMTD} and clk_2^{DMTD}; such timestamps are called *phase-tags* in the WR implementations. Each WRS has 20 sources of *phase-tags*: one from each of the 18 Ethernet ports, one from LO and one from External 10 MHz ref. input.

In WRS, the implementation values of v_0 and v_{DMTD} are equal to 62.5 MHz and 62.503815 MHz, respectively. The counter is clocked by v_{DMTD}, therefore the resolution of the phase-tags is better than 1 ps.

While a detailed description of the DDMTD architecture can be found in [22], the next section introduces the second basic element of the WRS implementation, the Xilinx Gigabit Ethernet Transceiver.

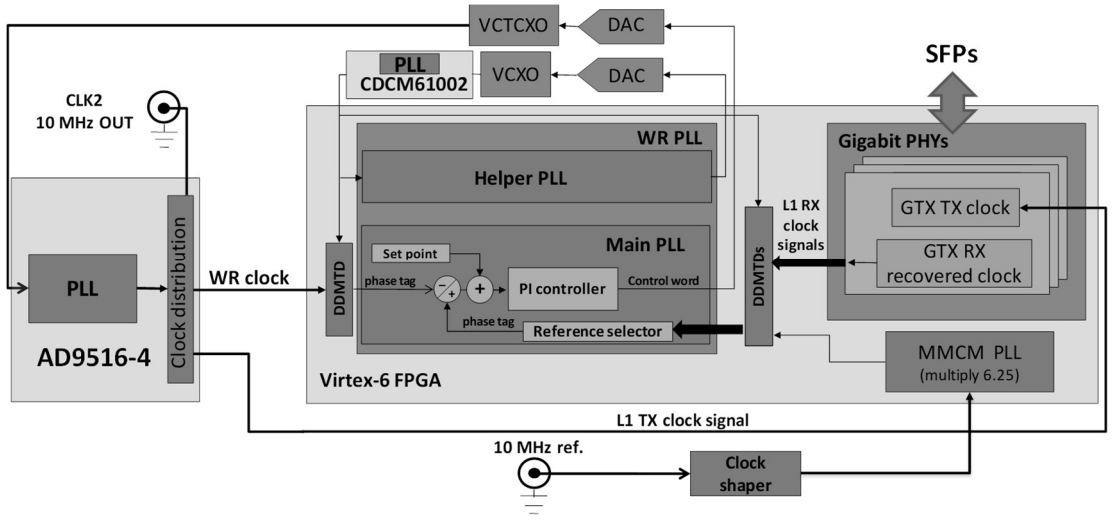

Fig. 4 WRS L1 clock generation and distribution.

B. *Xilinx Gigabit Ethernet Transceiver*

The WRS uses 18 Gigabit transceivers to implement an Ethernet L2 Switch. These transceivers are implemented inside the FPGA using a Xilinx-provided core codenamed "GTX". Each GTX implements:

- Clock & data recovery (CDR)
- PLL

The CDR circuit in the GTX transceiver extracts a clock signal (i.e. L1 RX clock signal) and data from an incoming serialized data stream. The PLL uses the L1 TX clock signal as a reference clock to produce a 1.25 GHz clock signal. The 1.25 GHz clock is used to perform the data serialization and transmission. Both components of the GTX, CDR and PLL, have a bandwidth exceeding 100 kHz.

The WR PLL is based on the DDMTD phase detector and requires two external local oscillators. The characteristics of these local oscillators contribute to the performance of the DDMTD and the quality of the synchronization, thus they are described in the following section.

C. *Local Oscillators*

The time-distribution functionalities of WRS require two oscillators:

- Helper LO
- Main LO

The Helper LO generates the *DMTD clock signal.* This LO is implemented using a voltage controlled crystal oscillator (VCXO, FRETHE025) and a hardware PLL (Texas Instruments CDCM61002) to multiply the frequency of the VCXO by a factor of 2.5. The VCXO has a nominal frequency of 25 MHz and a frequency pulling range exceeding ±100 ppm.

The Main LO generates the *Local PTP Clock signal*. This LO is implemented using a temperature compensated VCXO (VCTCXO, Mercury VM53S3) and another hardware PLL (Analog Devices AD9516-4) that multiplies the VCTCXO's frequency by a factor of 2.5. The VCTCXO has a nominal frequency of 25 MHz and a pull-range exceeding ±5.6 ppm, compliant with Synchronous Ethernet requirements.

It should be noted that the intrinsic noise of WRS's LOs in free-running mode (i.e. WR PLL disabled) results in both close-in phase noise and stability worse than commercial Cesium frequency standards (e.g. Symmetricom Cs4000).

Both LOs are controlled by WR PLL, a software implementation of a PLL, described in Section IV.

IV. THE WRS CLOCK GENERATION & DISTRIBUTION

The WRS has a complex clock generation and distribution scheme that consists of 20 digital phase detectors, two LOs, and five PLLs. A simplified diagram of the WR schema is depicted in Fig. 4 and described in this section.

The goal of the WR clock generation and distribution scheme is to generate a *WR clock* (i.e. Local PTP clock) that is synchronized with its source of time. This source is either an input 10 MHz clock signal (for GM), or another WR device (for BC/OC) connected over a fiber optic and SFPs. In the former case, the 10 MHz clock signal is multiplied to the frequency of the WR clock by *MMCM PLL* (Mixed Mode Clock Manager PLL). In the latter case, the L1 rx clock signal is recovered from the data stream by the GTX. In both cases, the WR clock is syntonized with the *reference clock signal* (from GTX or 10 MHz input) using the WR PLL that maintains a programmable phase-offset between the clock signals. Thus, the WR PLL effectively produces the WR clock.

The WR PLL is a discrete-time system, operating at the sample rate of the acquisition of phase-tags, i.e. 3.815 kHz. The WR PLL processes the phase-tags coming from two of the 20 phase detectors and internally consists of two PLL: the "Helper PLL" and the "Main PLL".

The *Helper PLL* produces the *DMTD clock signal* by controlling a VCXO – the *Helper LO*. Its only purpose is to guarantee that eq (1) is satisfied, using the *reference clock signal* as reference.

The *Main PLL* produces the *WR clock* by controlling the VCTCXO – the *Main LO*. It works by comparing the phase-tags of the *reference clock signal* to the phase-tags of the *WR clock signal*, phase-shifted by a programmable setpoint that is provided by WR PTP protocol implementation. The *Main PLL* is implemented using a proportional integrative (PI) controller, with a control bandwidth of about 30 Hz [19].

The VCTCXO does not generate the *WR clock signal* directly. It produces a 25 MHz clock signal that is multiplied and fanned out by an AD9516-4. This chip generates:

- *WR clock signal*; it has a nominal frequency of 62.5 MHz and it is used in WR applications.

- *L1 TX clock signal* it is required by GTX and has a nominal frequency of 125 MHz synchronous to the *WR clock*
- *CLK2 10 MHz output*: it is a synchronous copy of the *WR clock*, accessible from the front-panel of WRS. While the implementation uses a more complex scheme to generate this clock, its performance in terms of phase noise and stability are dominated by *Main PLL* and so the additional elements are not mentioned here.

The ability to correct the *Main LO* with a rate of 3815 corrections per second is a great asset in the WRS design. It allows the use of a control loop bandwidth greater than 100 Hz. It has been shown in [19] that this allows to control and reduce the intrinsic phase noise of the *Main LO*, achieving sub-tens of picoseconds precision using a cheap VCTCXO. The choice of the *Main PLL* bandwidth depends on several key figures: intrinsic noise and stability of the *Main LO,* the noise of the *reference clock* and the *additive* noise of the phase detectors.

The noise contributions of DDMTD and GTX affect *WR clock* performance from 0 Hz to the bandwidth of the Main PLL's PI controller. The study of the phase noise & stability limitations of DDMTD phase detector and the study of the GTX clock recovery circuitry, together allow to assess the WRS's performances limits due to the choice of using an FPGA-based digital phase detector and an FPGA-based Gigabit Ethernet transceivers. These studies are presented in the following sections V and VI.

V. DDMTD: Phase Noise & Stability

This section analyzes the noise introduced by the DDMTD with experimental results.

The DDMTD is extensively used in WR as a cost-effective phase-detector. The performance of such phase detector is critical in a time distribution system since the carrier close-in phase noise is not filtered by *Main PLL*.

The additive phase noise of the DDMTD depends on a number of factors that are similar to the analogue DMTD [23]:

- resolution & stability of the counter,
- phase noise of *DMTD clock signal,*
- noise of the Low-Voltage Differential Signaling (LVDS) input clock buffer and FPGA's clock distribution,
- noise of the D-type Flip-Flops (DFF), e.g. meta-stability window, thermal noise, etc.

An accurate analysis of noise contributions is performed in the following subsections. We first describe in V.A the experimental setup used to measure the contributions. We use this setup in V.B to investigate the resolution and stability of the time-interval counter used in DDMTD. The same setup is used in V.D to analyze phase noise of the *DMTD clock signal* and its effects on the DDMTD measurement. We also evaluate the additive DDMTD phase noise in V.E and identify the main contributor to DDMTD flicker noise in V.F. Finally, we outline the overall contribution of DDMTD to the WRS time and frequency transfer in V.G, and provide an outlook for implementation of DDMTD in new FPGA families in V.G

A. The experimental setup

Fig. 5 shows the experimental setup used to assess the intrinsic noise of DDMTD. The setup is composed by a Cesium reference time-base (Symmetricom Cs4000), a phase noise and time-interval analyzer (Microsemi 3120A) referred to Cs4000, a low-noise clock synthesis board (AD9516-4-EVB), and a WRS equipped with a "WRS SMA board".

The "WRS SMA board" [25] is a custom board used to directly feed LVDS clock signals to the FPGA by means of a spare connector [28]. An additional modification was made to probe the *DMTD clock signal* directly from one of the CDCM61002 outputs.

The AD9516-4-EVB is configured to generate two clean clock signals at 62.5 MHz, using Symmetricom Cs4000 as frequency reference (AD9516-4 PLL bandwidth ~100 kHz). One of them is also used by the *Helper PLL* as *reference clock signal*. Fig. 6 shows the phase noise measurement of this clock signal (divided by 2 in order to respect the maximum frequency limit of the Microsemi 3120A).

The experimental setup is designed to measure the phase noise contributions of DDMTD (i.e. *additive* phase noise). Therefore, the results in terms of stability and close-in phase noise may exceed the absolute phase noise and stability performance of Cs4000. The experimental setup was in a thermal equilibrium before each experiment, with room temperature stable within ±1 °C during each experiment (about 30 minutes per experiment).

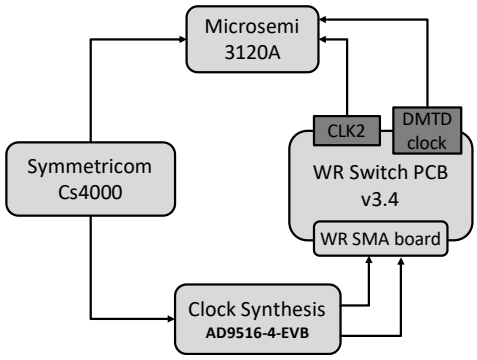

Fig. 5. Experimental setup to evaluate phase noise and stability of DDMTD.

B. Resolution & stability of the time-interval counter

In WRS, the counter is used to produce phase-tags and it is clocked by the *DMTD clock signal,* as shown in Fig. 3. The counter noise contributions that affect the measurement of Δt^{DMTD} are:

- time-resolution of the counter,
- stability of the counter's time-base.

The time-resolution of the counter is about 16 ns. However, as a result of Eq. (2), the phase offset (Δt) measured by the counter has a resolution better than 1 ps.

The counter measures the phase offset using the *DMTD clocks signal* as the time-base. In particular, between producing two phase-tags, the counter is incremented using the *DMTD clock signal*. The larger the phase offset, the longer the time-interval (Δt^{DMTD}) between the phase-tags and the bigger is the effect of time-base instability on the measurement. In WRS, the time-interval Δt^{DMTD} depends on the setpoint value provided to the *Main PLL* by the WR PTP daemon. The setpoint is the fixed offset between the recovered *L1 rx clock signal* and the *WR clock signal* that must be maintained to ensure sub-ns phase-alignment with

the reference clock(i.e. the *WR clock* of the GM). The maximum value of the setpoint is equal to one period of the *WR clock*, i.e. $\Delta t = 16\ ns$. Therefore, the maximum measurement duration is $\Delta t^{DMTD} = 262$ µs.

In order to assess the contribution of the counter's time-base stability to the measurement uncertainty of the DDMTD, the stability of the *DMTD clock signal* is measured using the experimental setup described in V.A

Table I shows the experimental results. The Allan Deviation of the *DMTD clock signal* is about 3 ppb at $\tau = 1\ ms$. For instance, if the *DMTD clock signal* has a frequency transient error of 10 ppb during the measurement interval, the worst-case error is equal to $16\ ns\ \times 10\ ppb$ which is below the DDMTD resolution and thus negligible. The long-term accuracy is preserved since the counter clock is phase-locked to the *reference clock signal*.

TABLE I STABILITY OF THE DMTD CLOCK SIGNAL, MEASURED WITH MICROSEMI 3120A.

Allan Deviation of clk_{DMTD} (ENBW 500 Hz)	
Integration period τ (s)	***Allan Deviation (s/s)***
0.001 s	$3 \cdot 10^{-9}$
0.01 s	$7 \cdot 10^{-10}$
0.1 s	$8 \cdot 10^{-11}$
1 s	$1 \cdot 10^{-11}$

C. *Phase noise of the DMTD clock signal and its effect on the DDMTD measurement*

The DDMTD uses the *DMTD clock signal* to demodulate the input clocks. Ideally, if the input clocks are aligned ($\Delta t = 0\ ns$), the phase noise of the *DMTD clock signal* is rejected [20]. However, this condition is never met in real scenarios; therefore, an estimation of the *additive* phase noise due to the *DMTD clock signal* is important.

The effect of the *DMTD clock signal* stability on a DMTD stability floor has been analyzed in [23][24]. The result of the analysis, after a conversion in the phase noise domain, shows that the phase noise of the *DMTD clock signal* affects the additive DDMTD phase noise. Moreover, the impact on the noise floor has a dependency on the setpoint value of the *Main PLL*. Formula (3) shows this relationship where $L_C(f)$ is the phase noise of the *DMTD clock signal* and Δt^{DMTD} is the phase-offset between the output signals (i.e. the phase offset between the input clocks increased by the DDMTD zooming effect).

$$L_{DDMTD}(f) \cong L_C(f) + 10 \cdot \log_{10}\left(4 \cdot sin^2(\pi f \Delta t^{DMTD})\right) \quad (3)$$

Formula (3) shows that the *DMTD clock signal* phase noise is high-pass filtered and the worst-case scenario is when the setpoint is at the maximum value. The worst-case additive phase noise $L_{DDMTD}(f)$ can be estimated using the phase noise data of the *DMTD clock signal*, depicted in Fig. 6, with Δt^{DMTD} =262 µs (i.e. the maximum value of Δt^{DMTD}).

The results presented in the following section will show that the phase noise of the *DMTD clock signal* described in this section is a negligible contribution to the additive phase noise of the DDMTD.

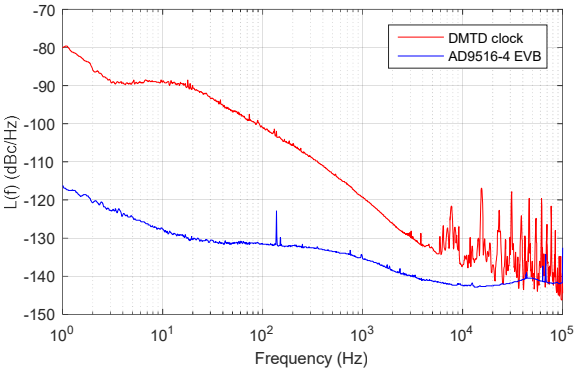

Fig. 6 Red trace is the phase noise of DDMTD clock $L_C(f)$; blue trace is the phase noise of AD9516-4 EVB's clock output. Traces obtained using Microsemi 3120A. For sake of clarity, the phase noise is scaled for an equivalent 10 MHz carrier.

D. *Experimental evaluation of the additive DDMTD phase noise*

The characterization of the additive noise of a DMTD-based phase detector can be performed by feeding two identical copies of a clean clock signal into two DDMTD phase detectors. Ideally, the *phase-tags* of the two DDMTD blocks, after subtraction, should show a constant phase offset value. Experimentally, the result is a phase signal containing the noise introduced by each element that is not in the common signal path.

The experimental characterization was performed using the experimental setup shown in Fig. 7. An AD9516-4-EVB board was used to generate two clock signals at 62.5 MHz, routed to the FPGA's pins by a WR SMA board. Fig. 7 shows the logic blocks implemented inside the Virtex-6. The two clock signals were connected to the FPGA's clock distribution network by the "IOBUFDS" primitive, which translate the LVDS clock signal to a proprietary signal standard used in the FPGA fabric. Two DDMTDs blocks were instantiated, generating *phase-tags* for each input clock. The *phase-tags* were collected by WR PLL and transmitted to a personal computer (P.C.) for post-processing.

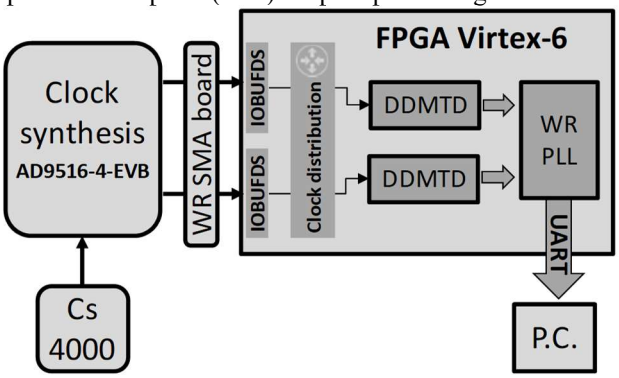

Fig. 7 Experimental setup to evaluate the additive DDMTD phase noise.

The post-processed signal is a time-error function; it can be used to calculate the time jitter (calculated as standard deviation of the time-error function) and the phase noise introduced by the DDMTD phase-detector. The experimental setup uses two matched length cable to obtain a $\Delta t \approx 0\ ns$. To obtain $\Delta t \approx 16\ ns$, the *phase-tags* are processed using the data of the previous sample.

The experimental results show a time jitter of about 4 ps RMS for both delays ($\Delta t \cong 0\ ns$ and $\Delta t \cong 16$ ns). Fig. 8 shows the phase noise of DDMTD where the blue line is the

phase noise of the DDMTD itself and the red line is the additive phase noise of *DMTD clock* phase noise according to eq. (3). Notably, the noise spectrum is limited to 2 kHz due to the discrete-time nature of the DDMTD.

The results show that the noise of the DDMTD comprises flicker PM noise and white PM noise. The flicker noise is dominant below 10 Hz and it is typically due to transistor noise related to the process technology [26]. The white noise limits the phase noise to -108 dBc/Hz and it can be traced to thermal noise, DFF meta-stability window and/or to phase noise folding due to aliasing (as DDMTD is a sampled system). The effect of the *DMTD clock signal* phase noise on the results is shown for Δt=16 ns in Fig. 8 (red line). The effect of the *DMTD clock* phase noise is negligible.

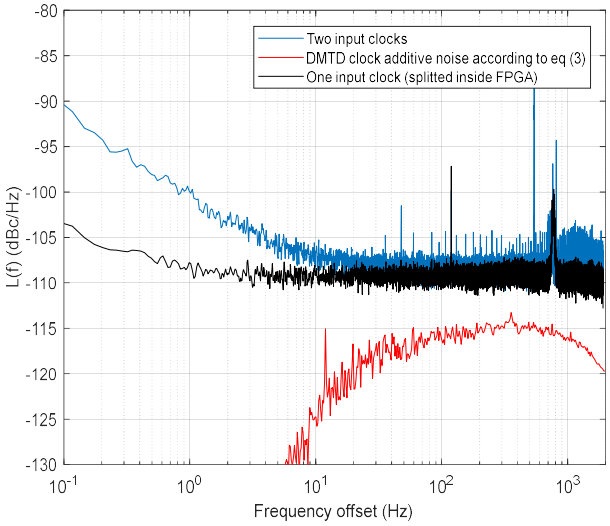

Fig. 8 Additive phase noise contributions of DDMTD. Blue line is the additive phase noise of the DDMTD, red line is the additive phase noise due to the *DMTD clock signal* phase noise. Black line is the additive phase noise of the DDMTD (single input clock).

Fig. 9 shows the Modified Allan Deviation (MDEV) calculated from the *phase-tags*. The limiting factor of the DDMTD is the flicker PM noise, which is limiting the MDEV at τ =1 s to 4E-13. In order to determine the source of the measured phase noise, the experiment in the following subsection was performed.

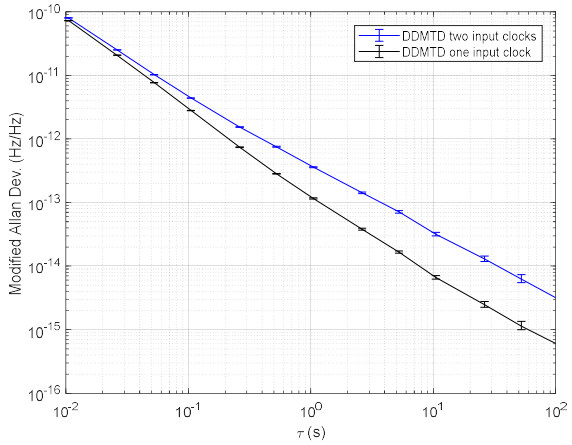

Fig. 9 Modified Allan Deviation (MDEV) of DDMTD. Blue line is MDEV of the DDMTD using two input clocks, black line is MDEV of the DDMTD using one input clock (clock duplication inside the FPGA). The experimental data is derived from phase-tags post-processing, with an equivalent noise bandwidth of 50 Hz (ENBW 50 Hz).

E. Experimental identification of the main contributor to DDMTD flicker noise

The experiment is very similar to the one performed in the previous section, however, only one clock signal is supplied to the FPGA. The second clock signal is derived from the first one, using a DDMTD block manually placed near the first one. This setup allows decoupling the effect of the D-type flip-flops (DFF) sampling performance (due to thermal noise, metastability, etc.) from the LVDS input clock buffer (IOBUFDS) and clock distribution. The idea is that any noise introduced by IOBUFDS and clock routing act as a common noise error on the *phase-tags* and it is rejected by the post-processing procedure.

Additionally to the results from the previous subsection (labeled “two input clocks”), Fig. 8 shows the phase noise of DDMTD obtained in the experiment described in this section (“one input clock” label). The flicker noise of the ”one input clock” is greatly reduced, from -100 dBc at 1Hz down to -107 dBc at 1Hz (mixed with white PM noise). The short-term stability of the DDMTD is lower, with a dominant flicker PM noise for observation time greater than 10 s. as shown in Fig.9 (”one input clock” trace).

These results suggest that the flicker noise measured in Section V.D is dominated by the LVDS input clocks buffer and clock routing.

F. Overall contribution of DDMTD to the WRS time and frequency transfer

The additive phase noise and stability limits measured in Section V.D show a mix of white PM noise and flicker PM noise. Notably, the phase noise above the Main PLL bandwidth is filtered by WR PLL. The phase noise within the Main PLL bandwidth is additively propagated by WR PLL.

The most limiting factor introduced by DDMTD is the flicker PM noise, limiting the MDEV at τ =1 s to 4E-13. In particular, the flicker PM noise is still dominant at τ =100 s, as shown in Fig. 9. Last, the main contributors to flicker PM noise are the IOBUFDS LVDS input clocks buffer and clock routing.

The WR PTP daemon updates the setpoint using a control loop time constant of about 5 s. Notably, the PTP daemon cannot improve the stability performance affected by DDMTD flicker noise because the WR PTP uses data provided by DDMTD to calculate the setpoint itself.

G. An outlook for future implementations

The performance of the FPGA-based DDMTD implementation relies on the process technology used to manufacture the FPGA in use. The WRS uses Xilinx Virtex-6, released in 2008, manufactured using 40 nm technology. New implementations of WR are expected to use newer FPGAs with a decreased transistor size due to newer process technology. According to [26][27] the DDMTD flicker noise is expected to be worse using smaller transistor size, but our experiment results contradict this assumption.

Fig. 10 shows the MDEV of DDMTD implemented on two new FPGAs, “Kintex-7” and “Kintex UltraScale”, manufactured using a 28 nm and 20 nm process technology, respectively. Evaluation boards with these two FPGAs were used to measure the performance of DDMTD in an experimental setup similar to the one used in V.A and depicted in Fig. 5.

The results presented in Fig. 10 seemingly contradict [26]. The stability at τ =1s, although still dominated by flicker PM noise, is better on Kintex-7 (28 nm) and Kintex UltraScale (20 nm) than in Virtex-6 (40 nm) in the WRS. Probably, the transistors size of IOBUFDS and clock routing circuitry are scaled down less than the process technology.

The DDMTD performs slightly better on the newer FPGAs than on the old ones; newer implementation of WR can benefit from using DDMTD without any performance compromise. Moreover, the proposed measurement setup can be used to evaluate the FPGA technology before adopting it for mass production of WR Switch.

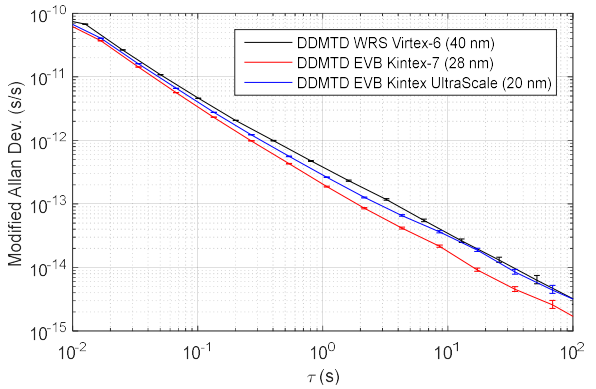

Fig. 10 Modified Allan Deviation (MDEV) of the DDMTD using two input clocks in WRS, Kintex-7, and Kintex Ultrascale, shown with black, red and blue lines respectively. The experimental data is derived from phase-tags post-processing.

VI. GTX: Phase Noise & Stability

The *L1 RX clock signal* recovered by the GTX is used by the DDMTD-based WR PLL to produce the *WR clock* by adjusting the VCTCXO. The performance of the GTX is critical and it must be characterized as well.

To characterize the performance of the GTX, the phase noise and stability of GTX transceivers are evaluated in VI.A and VI.B using two different experimental setups. The former one uses the "ML605 Virtex-6 Evaluation Kit", the latter is based on the WRS. After the evaluation of GTX performance, we describe its overall contribution to the WRS time and frequency transfer in VI.C.

A. Stability (ML605 board)

The stability performance of the GTX is evaluated using the "IBERT Core" in the experimental setup depicted in Fig. 11.

The setup of Fig. 11 is based on the ML605 Evaluation board, the AD9516-4-EVB clock synthesizer, and the Microsemi 3120A phase noise test probe. The *IBERT Core* is implemented in ML605 Evaluation board. The AD9516-4-EVK is used to generate the *L1 TX clock signal*. The *L1 TX clock signal* is used by the GTX to phase-lock its 1.25 GHz PLL. The 1.25 GHz clock is then used to output the serialized "TX DATA". Using a loopback cable, the "TX DATA" is sent back to the GTX. The GTX performs a clock recovery using the RX DATA. The *L1 RX clock signal* recovered and the "TX DATA" pins of GTX are fed to a low-noise clock divider. Finally, Microsemi 3120A is used to analyze both phase noise and stability performances. The *IBERT Core* allows to evaluate the behavior of GTX that receives a stream of random data (PRBS 7-bit) or a clock-like data (Ethernet IDLE pattern). These two test patterns are used to analyze the stability of the recovered clock.

Fig. 12 shows the MDEV of the recovered clock using the two test patterns. It can be seen that the recovered clock exhibits a flicker PM noise, with an MDEV of about 4E-13 at τ =1 s, similar to the stability value of the DDMTD. Notably, since the performance measured with both test patterns is the same, we conclude that the quality of the recovered clock is not pattern-dependent. The TX pins show a short-term stability $\sqrt{2}$ times better than L1 RX clock at τ=1s with a dominant flicker PM noise.

Although the short-term stability of GTX is very similar to DDMTD, the L1 TX clock is not fed via IOBUFDS, it uses a dedicated Low Voltage Positive Emitter Coupled Logic (LVPECL) input buffer.

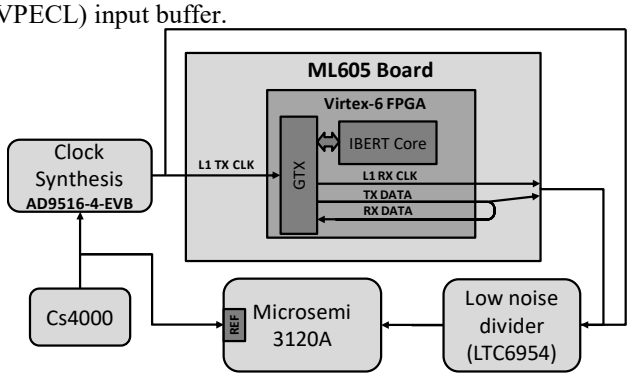

Fig. 11 Experimental setup to evaluate phase noise and stability of GTX.

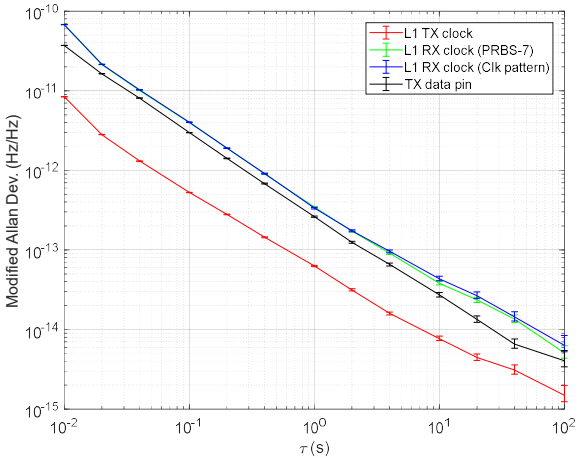

Fig. 12 Modified Allan Deviation of GTX measured using 3120A (ENBW 50 Hz)..

B. Phase noise and stability (WRS board)

The evaluation of GTX performance described in this section analyzes whether the PCB of the WRS introduces performance deterioration, with respect to the performance evaluated using ML605 board in the previous section.

The phase noise and stability of the clock recovered by GTX can be measured using various methods. The most obvious one is to route the recovered clock to the output pins of the FPGA (using the WRS SMA clock board). However, the mere act of routing and probing the L1 RX clock signal could introduce additional phase noise due to the setup. For this reason, an alternative method is used: a DDMTD records the phase of the L1 RX clock signal. Since the performance

of the DDMTD has been fully characterized in Section V, it's easy to infer the phase noise of the clock recovered by GTX.

The experimental setup, depicted in Fig. 13, includes two WRSs (acting as GM and BC), the AD9516-4-EVK clock synthesizer, and the Microsemi 3120A phase noise test probe. The two WRSs are connected using recommended SFPs (AXGE-3454-0531 & AXGE-1254-0531, [14] and a short fiber optic (3 meters). The DDMTD is used to record the recovered clock phase noise, using as reference clock signal a clean clock signal provided by AD9516-4-EVB via the WRS SMA clock board. Due to the performance limitations of the current WRS in GM mode, a hardware modification was done to improve its performance, as described in [28] . The GM phase noise constitutes the experimental noise floor in the characterization of the phase noise and stability of the second WRS acting as BC. Fig. 14 shows the phase noise of the GM measured using Microsemi 3120A. During the measurements made using the experimental setup in Fig. 13, the data from the DDMTD and from Microsemi 3120A were collected simultaneously, with a duration of about 30 minutes.

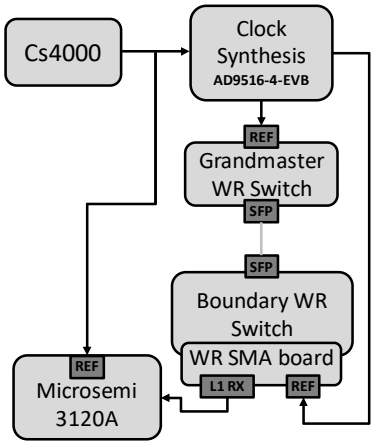

Fig. 13 Experimental setup using WRS to evaluate performance deterioration due to PCB.

Fig. 14 shows the results of the phase noise measurements using the 3120A. The red trace shows the phase noise of the recovered clock, scaled to an equivalent 10 MHz carrier for the sake of clarity. The phase noise below 10 Hz is very similar to the additive noise of DDMTD. The phase noise at 100 Hz-100 kHz is filtered by the *Main PLL* transfer function. Spurs at 1Hz-10kHz can be observed in the blue trace, probably related to a periodic noise from noisy electronic components.

Fig. 15 shows the phase noise of the recovered clock, as seen by the DDMTD (blue line). As previously indicated, the DDMTD is fed from the WRS SMA clock board to measure the phase offset between the recovered clock and the reference clock. In Fig. 15, the black line is the DDMTD additive noise, estimated (in the previous section) as a combination of white PM noise (-108 dBc) combined with flicker PM noise (-100 dBc at 1 Hz). The measured GTX recovered clock phase noise is depicted with a blue line in Fig. 15. It has a White PM noise of about -106 dBc, probably due to the higher frequency jitter noise folding. Moreover, the phase noise below 10 Hz has a flicker PM behavior, with a phase noise of -97 dBc at 1 Hz. Since the measured phase noise is higher than the DDMTD noise floor of about 2-3 dB, we can infer that the L1 RX recovered clock noise has a phase noise almost equal to the one of the DDMTD.

Fig. 16 shows the stability measurements of L1 RX clock signal using DDMTD (black trace) and Microsemi 3120A (blue trace). The blue trace shows a flicker PM behavior with an MDEV of 6E-13 at τ =1 s. As previously discussed, the results are a combination of noise coming from L1 RX clock and from DDMTD. The red trace shows the same stability measurement performed using 3120A to evaluate the recovered clock stability, showing a stability of 4E-13 at τ =1 s.

C. *Overall contribution of GTX to the WRS time and frequency transfer*

The additive phase noise introduced by the transmission circuitry and CDR circuitry of GTX is as significant as the additive phase noise introduced by DDMTD. Notably, the L1 RX clock noise exhibits a flicker PM noise having a magnitude comparable to that of DDMTD (-100 dBc at 1 Hz and stability of 4E-13 at τ=1 s). As a result, the noise contributions that affect the short-term stability of the WR time-transfer are equally shared between DMDTD and GTX, which is confirmed by the experiment in VI.B.

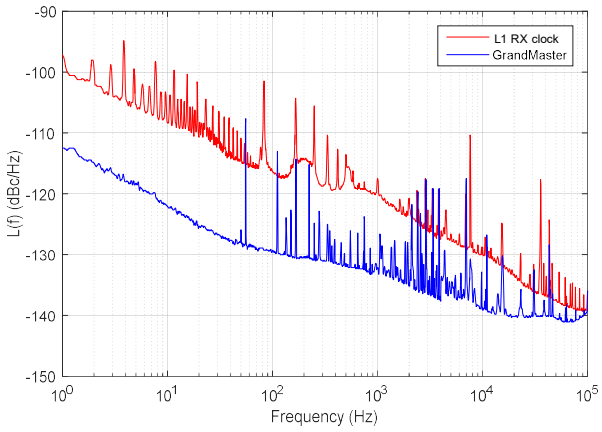

Fig. 14 Phase noise measured with 3120A. Blue trace is the phase noise of the modified Grandmaster, red trace is the phase noise of the L1 RX recovered clock. For the sake of clarity, the plots have been scaled to an equivalent 10 MHz carrier.

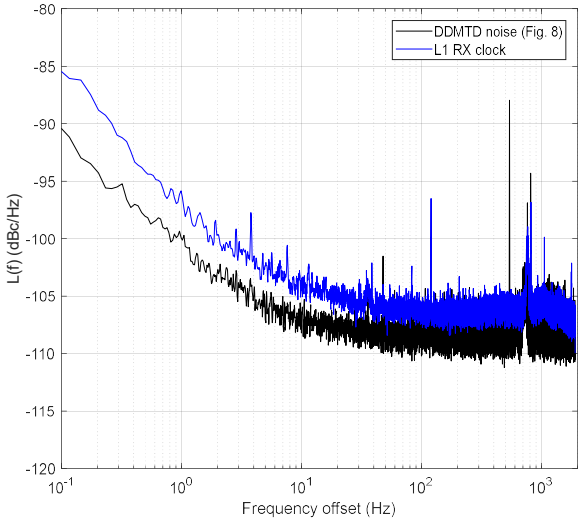

Fig. 15 Phase noise measured with DDMTD. Blue line is the calculated phase noise of recovered clock. Black line is the DDMTD noise of Fig. 8 ("two input clocks"). For the sake of clarity, the plots have been scaled to an equivalent 10 MHz carrier.

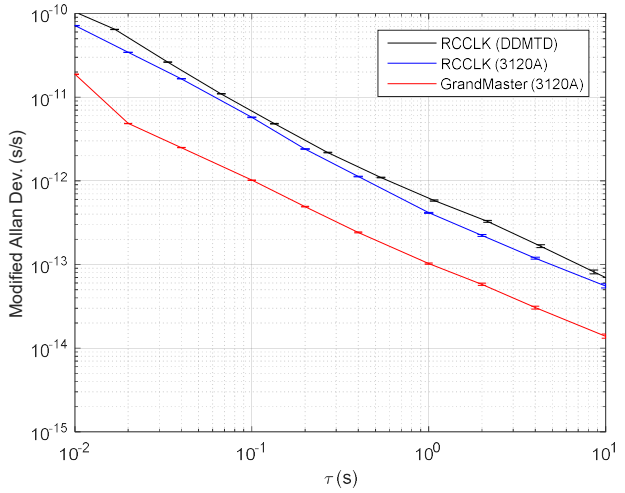

Fig. 16 Modified Allan Deviation of the L1 RX recovered clock (RCCLK), calculated from DDMTD data (black line) and measured by 3120A (blue line). In both measurements, ENBW is 50 Hz.

VII. REACHABILITY OF ULTIMATE LIMITS

Previous sections described the performance limits imposed by the use of DDMTD and GTX. The current implementation of the WRS suffers from some additional issues related to non-optimal design choices. These issues result in a jitter which is one order of magnitude worse than the fundamental limits explored in this article. The main culprits are the use of a noisy internal MMCM PLL (shown in Fig. 4) in the Virtex-6 in Grandmaster mode, and instabilities in the Main LO induced by cooling airflow in the WRS enclosure (box). The former issue is due to the phase noise of the clock synthesized by MMCM PLL, the clock signal has high phase noise at a frequency offset around 1 MHz [19]. Due to the discrete-time nature of DDMTD and of WR PLL, the phase noise is folding back in baseband. The latter issue was partially solved in [19] with an increased control loop bandwidth (from 30 Hz to 200 Hz) of the Main LO.

The above-mentioned issues are solved by a Low-Jitter Daughterboard (LJD) [29] that can be plugged into the main board of the existing WRS. The board uses a dedicated PLL (Analog Devices AD9516-4) to perform the required clock synthesis, without using the MMCM PLL, and a VCTCXO (Connor-Winfield DOT050-25M) oscillator protected from the airflow. The LJD allowed us to demonstrate that the ultimate limits established in this paper can be reached in reality without changing the control loop bandwidth of the Main LO. The complete description of the LJD design and its long-term performance are out of the scope of this paper and they will be presented in a future article.

The experimental setup of Fig. 17 is used to characterize the ultimate limits of WR time-transfer using the LJD. The setup uses Symmetricom Cs4000 as time-reference for GM WRS and Microsemi 3120A. A 10 km optical fiber is used to connect the GM to the BC switch. An Ethernet traffic generator (Spirent Smartbits 6000c) is used to generate a broadcast traffic of 1 MB/s as realistic traffic conditions for the evaluation of the WR time-transfer performance. Microsemi 3120A is used to record phase data and stability over 3 h of measurement time for both GM and BC.

Fig. 18 shows the phase noise measurement of the currently available WRSs without and with the LJD. With the LJD, the improvement in terms of additive phase noise exceeds 20 dB for frequency offset below 30 Hz (i.e. within Main PLL bandwidth). TABLE II shows the integrated jitter: notably, the BC has a random jitter reduced by an order of magnitude.

The measured MDEV of GM with the LJD, depicted in Fig. 19, has a flicker PM noise that closely matches the short-term stability of DDMTD. Moreover, the stability of the BC with the LJD has a stability value at τ =1 s that closely matches the root sum squared of the three contributions: GM DDMTD stability, BC DDMTD stability, and BC GTX stability.

The above experimental results confirm the analysis performed in the previous sections and demonstrate the reachability of the ultimate limits.

The ten-fold improvement with respect to the current release of the WRS is a significant step towards high-stability time-transfer applications using WR.

Last, it is worth noting that some application fields (e.g. deep space applications) with short-term stability requirements may not match the performance limits of WRS with LJD. Those applications may benefit from the use of a high-stability Main LO, combined with a lower control loop bandwidth (i.e. lower than 1 Hz). It should be remarked that (for observation time greater than the control loop time constant) the WR time-transfer stability is affected by DDMTD and GTX. Therefore, knowing the ultimate performance limits showed in this paper is a necessary element in the proper design of such applications.

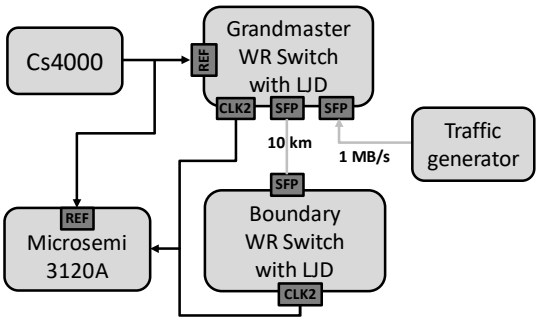

Fig. 17 Experimental setup to evaluate reachability of the ultimate performance limits presented in this article.

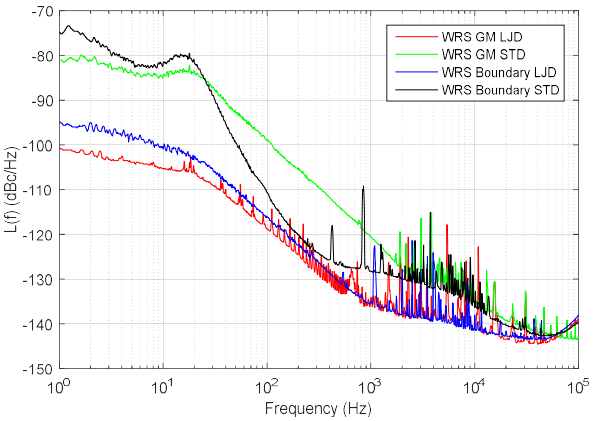

Fig. 18 Phase noise measured with Microsemi 3120A using the CLK2 10 MHz output

TABLE II JITTER MEASUREMENT USING 3120A

Node	Integrated random jitter (ps RMS)			
	Standard WRSs		WRSs with LJD	
	1 Hz-30 Hz	*100 Hz – 100 kHz*	*1 Hz-30 Hz*	*100 Hz – 100 kHz*
Grandmaster	7.7	2.5	0.6	0.8
Boundary	11	1.2	1.1	0.8

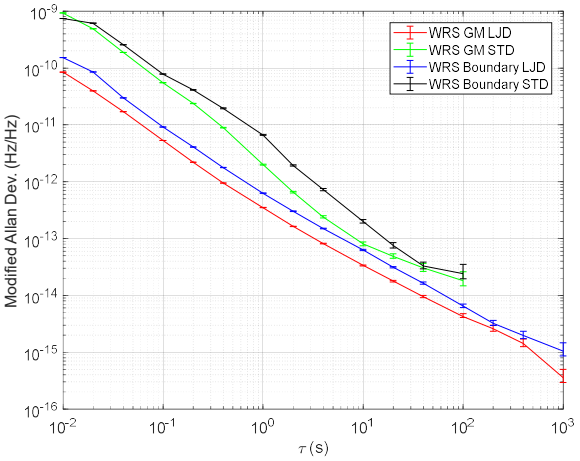

Fig. 19 MDEV measured with Microsemi 3120A (ENBW 50 Hz) using the CLK2 10 MHz output

VIII. CONCLUSIONS

WR is a high-accuracy time and frequency distribution system based on FPGA. Designed for CERN's needs, WR is now being considered by national time laboratories for high-stable time-transfer. This article analyzed the ultimate performance limits introduced by FPGA implementation of phase detectors and gigabit transceivers that have a direct effect on WR performance.

The phase detector introduces a limitation in short-term stability equal to MDEV 4E-13 at τ =1 s (ENBW 50 Hz), with a flicker PM behavior from τ =1 s to τ =100 s and more. The origin of flicker PM is due to the LVDS input clock buffer of the currently used FPGA and its related internal clock distribution. Similar results are observed for newer FPGAs, where a (slightly reduced) flicker PM is still present.

Notably, the FPGA-implemented Gigabit Transceiver has a noise contribution, in terms of short-term stability, almost equal to the contribution of the phase detector.

The experimental proof of the reachability of these ultimate limits have been performed with a Low-Jitter Daughterboard plugged onto the currently available WR switch. The results show an improvement of an order of magnitude in terms of close-in phase noise, jitter, and short-term stability, compared to the performance of the WR switch without the board. The enhancements to WR obtained with this board are useful for metrology applications, like inter-laboratory clock comparison. For example, they allow reduction of the observation time required to infer the noise introduced by WR time-transfer with respect to the noise of the clocks under test.

ACKNOWLEDGMENT

The authors thanks Javier Serrano (CERN) for his assistance and improvements on the paper, Tomasz Wlostowski (CERN) for his assistance on the experimental setups, Erik Van Der Bij (CERN) for his assistance in the development of the LJD, Anders Wallin (VTT Mikes Metrologia), Tjeerd Pinkert (Physikalisch-Technische Bundesanstalt), Henk Peek (Nikhef) and Paul-Eric Pottie (Observatoire de Paris SYRTE) for their valuable suggestions on the characterization of DDMTD and WR PLL.

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