



FmcAdc100k16b13cha
An informal description of the design

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Abstract

FmcAdc100k16b13cha is a 13 channel 16 bit 100kS/s ADC board with internal/external triggering in FMC (FPGA Mezzanine Card) format

FmcAdc100b13cha general information

FmcAdc100k16b13cha is the multichannel ADC board in FMC (FPGA Mezzanine Card) format.

Parameter	Value
Max Sampling speed	200 kSPS
Number of channels	- 13 (custom made cable) - 11 (standard camera-link interface)
Input connector	Mini D Ribbon 26, 13 differential pairs, separately shielded
Resolution	16 bits
Mezzanine to carrier interface	FMC low pin count connector
ADC interface	Standard parallel (\RD, \WR, data)
Sampling sequence	Simultaneous for all the channels
Clock source	On-board DAC controlled 20 MHz VCXO for the synchronization ability
Triggering	Internal and external - one of the inputs can work as a trigger input
Input voltage range	+/-5 V, +/- 10 V – software selectable
Analog bandwidth	14 kHz @ +/-5 V 22 kHz @ +/-10 V
Input type	Differential
Input impedance	1 MOhm
Antialiasing filter	2 pole, included
INL	+/-0.5 LSB typ. +/- 2 LSB max.
SNR	90 dB

ADC choice

For defining the parameters that could be achievable by our design, I did small research over the most famous ICs producing company's webpages. The result are available at following link: [OHWR: 16 bit multichannel ADC comparison](#).

The requirements to be passed by ADC are described below:

- ability of sampling the voltage simultaneously for all the channels,
- as many channels in the package as possible (at least 4),
- 100 kSPS sampling speed,
- 16 bits resolution,
- antialiasing filter on board,
- high impedance input buffer or amplifier is welcome,
- low SNR, INL and distortion factor,
- if there is no need to deliver negative voltage for the supply the ADC, it will simplify the design.

The most suitable choice of the ADC is the **AD7606** which pass all the points shown above. Using the Analog Devices ADC will cause the circuit to be simple and elegant without destroying the performance.

The only problem is the **AD7606**'s maximum input signal frequency, which is lower than given in the spec of the ADC board (22 kHz @ +/-10 V input voltage range instead of the required 25 kHz). It has been decided, that the difference is small enough to be tolerated, and the features of the ADC predominate over this small disadvantage.

The schematic of the design is available here: [OHWR: FmcAdc100k16b13cha schematic](#)

Input connector/interface

Looking at the spec of the board you can treat it as the audio-like device. Because of the low frequency of the desired measured signal, there is no need to worry about the line matching, or the shape of the signal edges. The more disturbing problem is the cross-talk over the input cable. It was decided to use the interface, where every signal is separately shielded. Differential input of the ADC is useful feature for the noise / cross-talk cancelation. On the other hand, many industrial standards of the signal providing use differential lines. As a result of the searching for the useful, robust and reliable standard, it was decided to use CAMERA-LINK interface.

CAMERA-LINK description:

- 11 separately shielded differential pairs. Because of the connector, allowing to connect 13 differential pairs, custom made cable can provide lines for maximum 13 inputs,
- Mini D Ribbon 26 connector. Electrically and mechanically reliable, long term industrial standard,
- Availability of halogen free cables allow the interface to pass the fire protection standard.

Clock source

To avoid the noise added by unstable clock, low jitter generator use is necessary. The sampling moment couldn't be defined by standard or even clock line of FPGA because of the edge jitter.

Small calculation:

clock jitter that wouldn't have a negative impact on the performance is given by the equation:

$$t_j = \frac{1}{\pi * f_{sig} * 2^{N+1}} = \frac{1}{3.14 * 25000 \text{ Hz} * 2^{17}} = 97 \text{ ps} \quad \text{where:}$$

- f_{sig} - maximum input signal frequency (about 25 kHz)
- N - resolution of the ADC (16 bits)

The jitter of the signal generated directly by the FPGA would be closer to +/- 1ns, so it wouldn't be acceptable. It is decided to use simple D flip-flop based synchronizer to make possible the sampling with the period which can be the multiple of the period generated by the oscillator ($N * 1 / 20 \text{ MHz} \Rightarrow N * 50 \text{ ns}$).

The signal source is the voltage controlled crystal oscillator. Adding the serially driven DAC will not increase the price of the board much, but it will give the possibility of synchronizing the sampling frequency with external clock signal.

Power supply

Great advantage of the AD7606 is that it needs only the single supply for being powered. The current consumption from the analog voltage at the max. sampling speed is only 16 mA for one ADC, so standard linear regulator is be used. Power loss over the regulator is:

$$(V_{in} - V_{out}) * I_{supply} = (12V - 5V) * (2 * 16 \text{ mA}) = 224 \text{ mW}$$

No switching regulators on-board means no additional noise sources and no problems with electrical compatibility.

