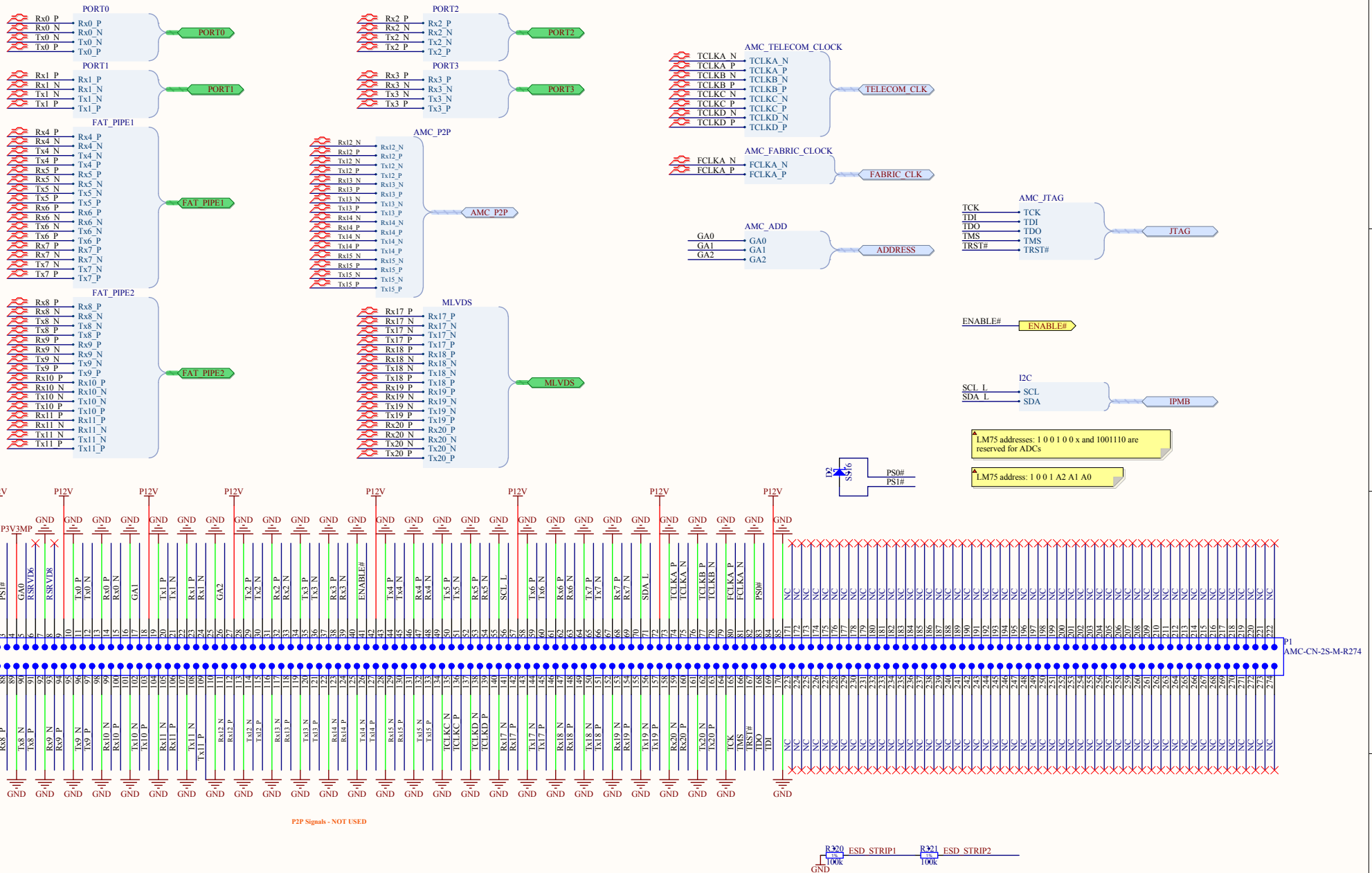
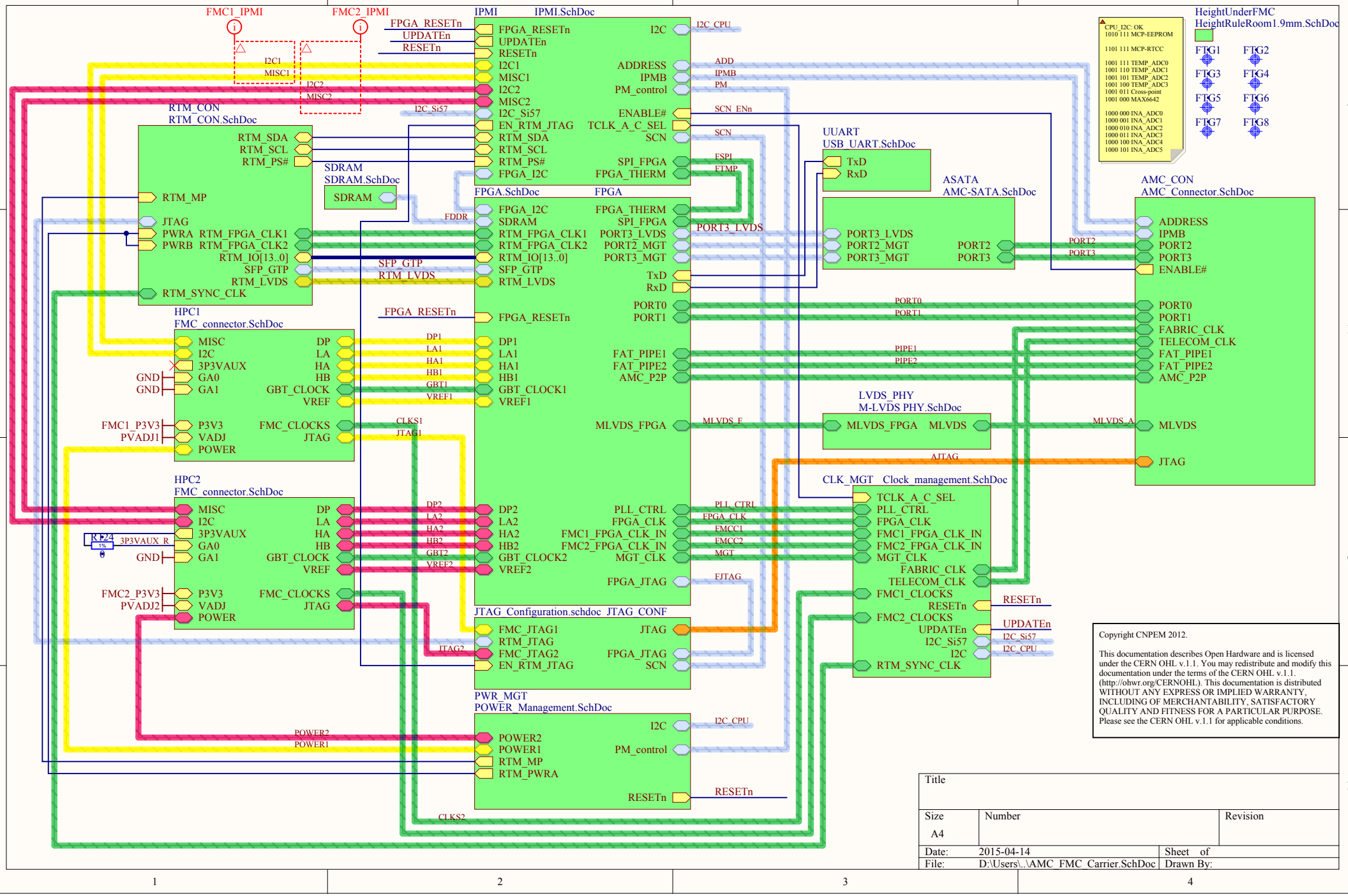


- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

Sheet Title	*AMC Top Sheet*		*ProjectOrganization* *ProjectAddress1* *ProjectAddress2* *ProjectAddress3* *ProjectAddress4*
Project Title	*ProjectTitle*		
Size: A3	Item: Item not interpreted	Revision: ItemRevision not interpreted	
Date: 2015-04-14	Time: 20:13:40	Sheet 1 of 30	
File: AMC_Connector.SchDoc			

Altium



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Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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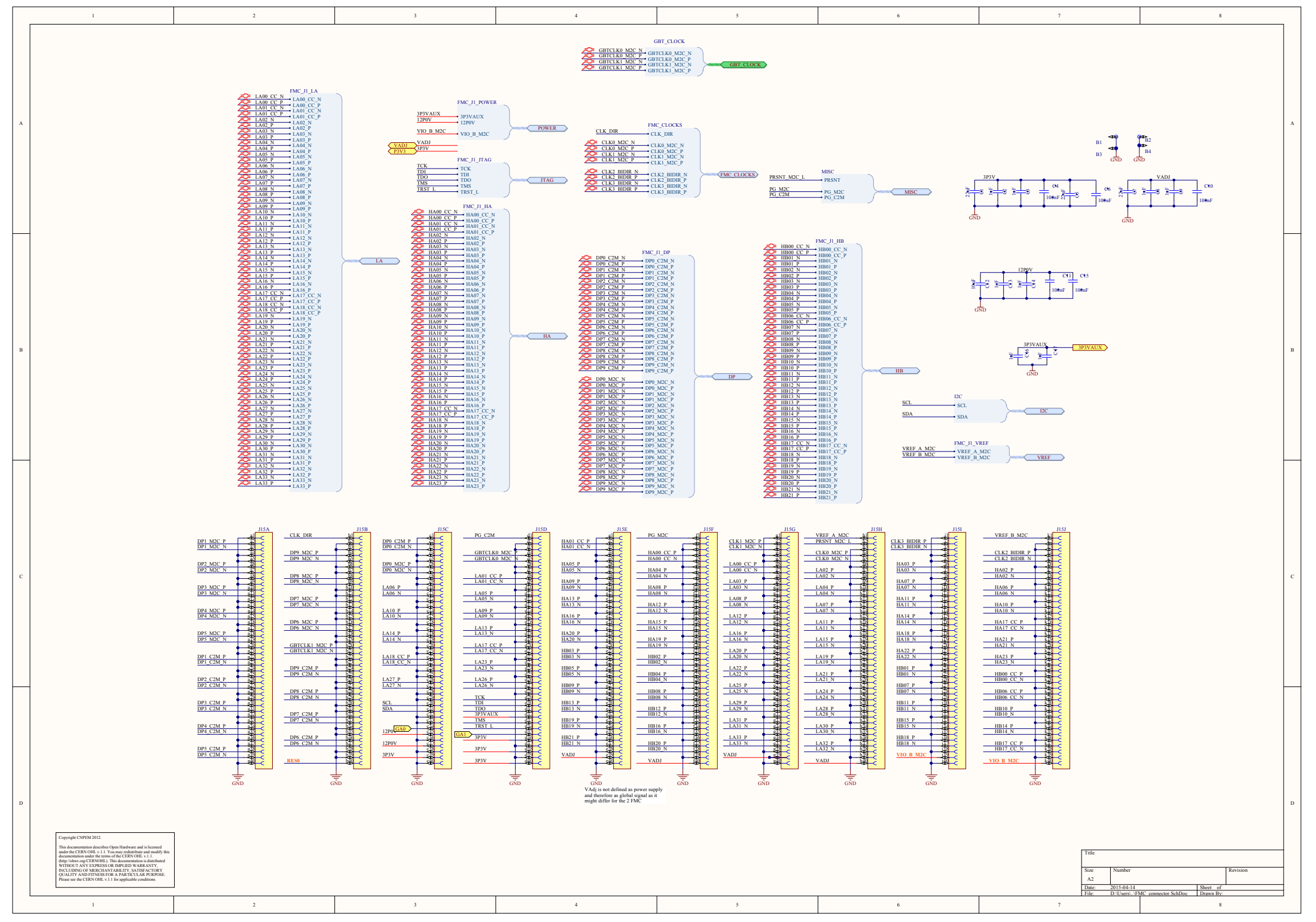

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Date: 2015-04-14	Sheet of	
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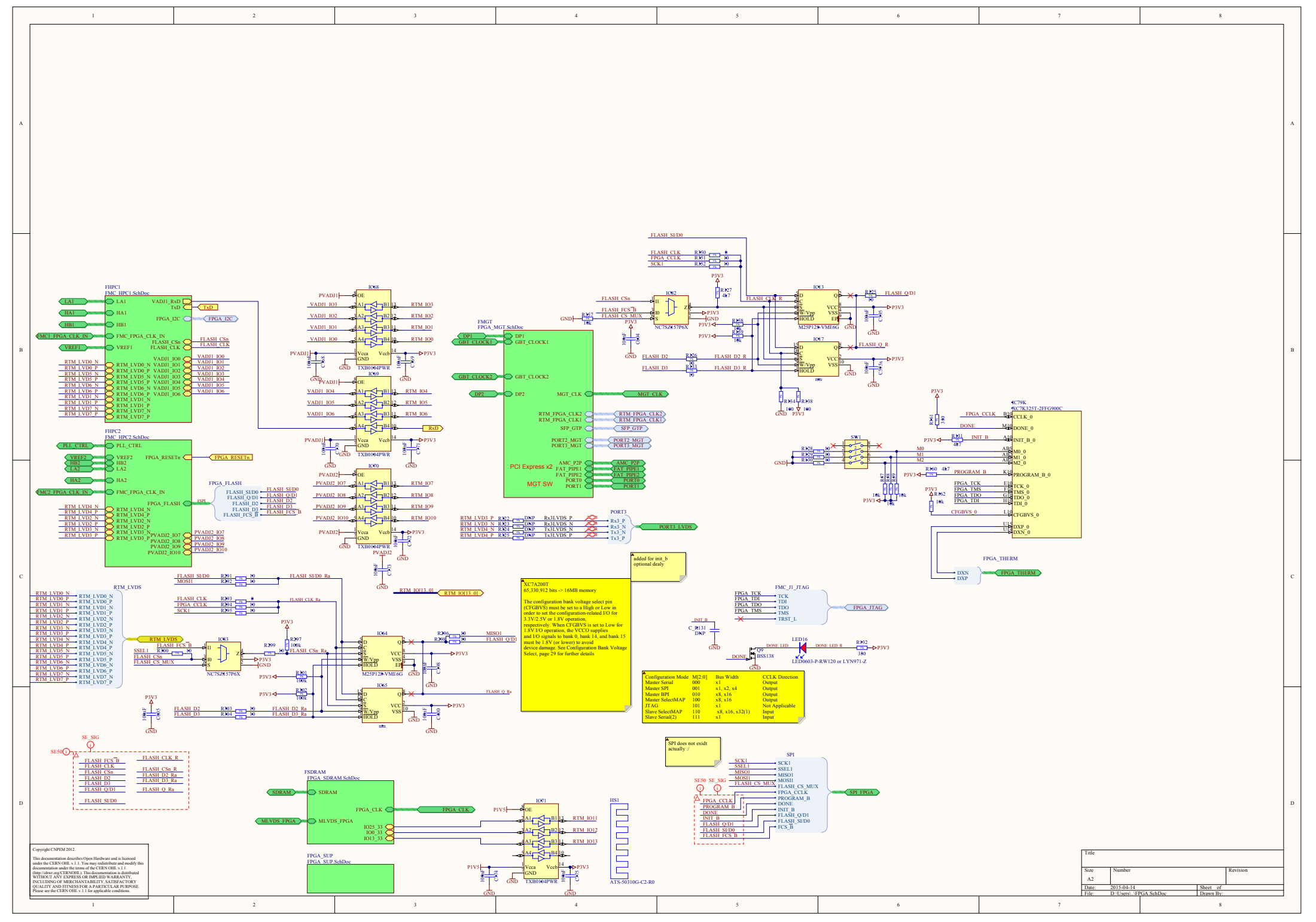
FHPC1
FMC_HPC1.SchDoc
FHPC2
FMC_HPC2.SchDoc
FMGT
FPGA_MGT.SchDoc
PCI Express x2
MGT SW
FSDRAM
FPGA_SDRAM.SchDoc
FPGA_SUP
FPGA_SUP.SchDoc
RTM_LVDS
FPGA_FLASH
FMC_J1_JTAG
SPI
SE50 SE_SIG
HS1
ATS-50310G-C2-R0
XC7A200T
65,330,912 bits -> 16MB memory
The configuration bank voltage select pin (CFGBVS) must be set to a High or Low in order to set the configuration-related I/O for 3.3V/2.5V or 1.8V operation, respectively. When CFGBVS is set to Low for 1.8V I/O operation, the VCCO supplies and I/O signals to bank 0, bank 14, and bank 15 must be 1.8V (or lower) to avoid device damage. See Configuration Bank Voltage Select, page 29 for further details
added for init_b optional dealy
SPI does not exidt actually :/
Configuration Mode M[2:0] Bus Width CCLK Direction
Master Serial 000 x1 Output
Master SPI 001 x1, x2, x4 Output
Master BPI 010 x8, x16 Output
Master SelectMAP 100 x8, x16 Output
JTAG 101 x1 Not Applicable
Slave SelectMAP 110 x8, x16, x32(1) Input
Slave Serial(2) 111 x1 Input
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Number
Revision
Date: 2015-04-14
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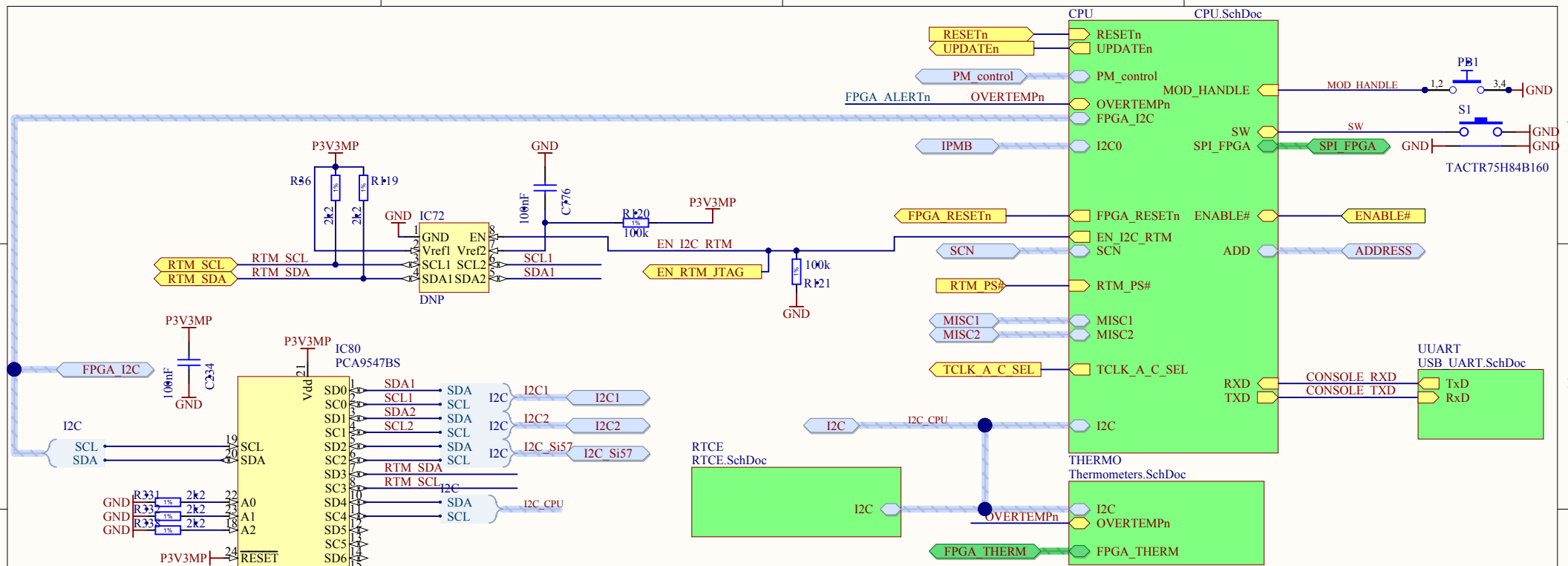
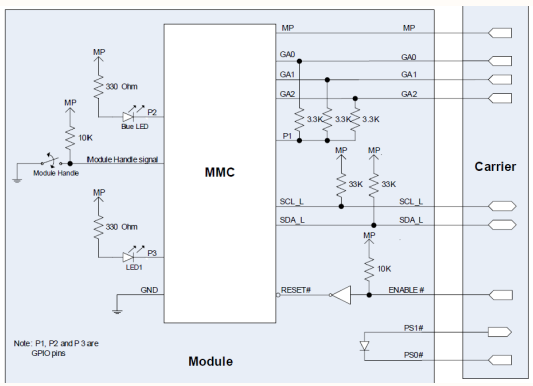
Drawn By:



GA[2..0]	IPMB-L address	MicroTCA Carrier's AMC Slot ID	AMC Carrier AdvancedTCA Board's AMC Slot ID	Module Physical address	
				Site Number	Site type
GGG	70h	Reserved	Reserved	NA	NA
GGU	72h	1	A1	1	AMC (07h)
GUG	74h	2	A2	2	AMC (07h)
GUU	76h	3	A3	3	AMC (07h)
UGG	78h	4	A4	4	AMC (07h)
UGU	7Ah	5	B1	5	AMC (07h)
UUG	7Ch	6	B2	6	AMC (07h)
UUP	7Eh	7	B3	7	AMC (07h)
UPU	80h	8	B4	8	AMC (07h)
UPP	82h	9	NA	9	AMC (07h)
PUU	84h	10	NA	10	AMC (07h)
PUP	86h	11	NA	11	AMC (07h)
PPU	88h	12	NA	12	AMC (07h)
GGP	8Ah	NA	NA	13	AMC (07h)
GUP	8Ch	NA	NA	14	AMC (07h)
GPG	8Eh	NA	NA	15	AMC (07h)
GPU	90h	NA	NA	16	AMC (07h)
GPP	92h	NA	NA	17	AMC (07h)
UGP	94h	NA	NA	18	AMC (07h)
UPG	96h	NA	NA	19	AMC (07h)
PGG	98h	NA	NA	20	AMC (07h)
PGU	9Ah	NA	NA	21	AMC (07h)
PGP	9Ch	NA	NA	22	AMC (07h)
PUG	9Eh	NA	NA	23	AMC (07h)
PPG	A0h	NA	NA	24	AMC (07h)
UUU	A2h	NA	NA	25	AMC (07h)
PPP	A4h	NA	NA	26	AMC (07h)



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Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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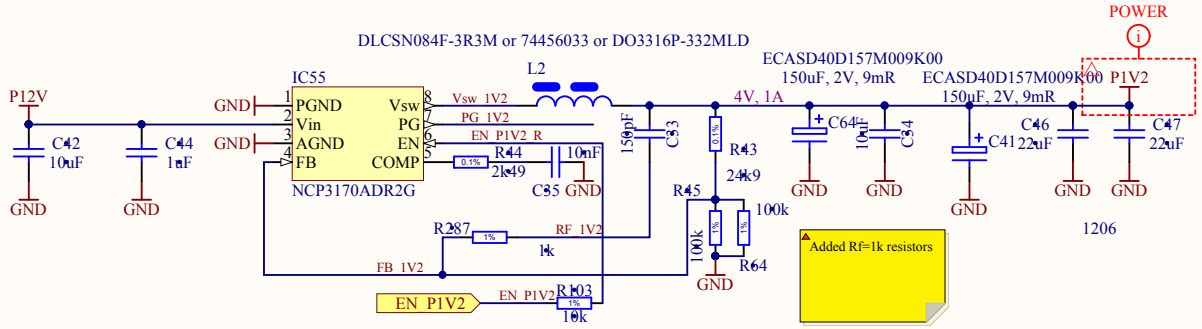
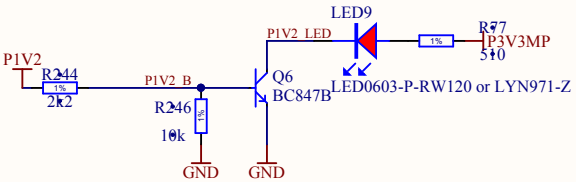
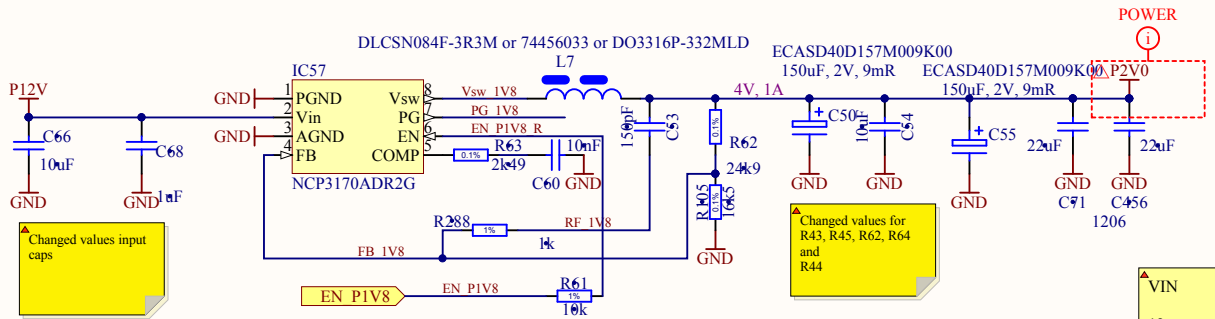
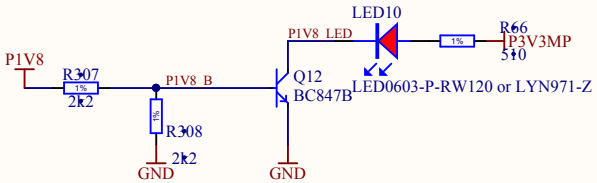
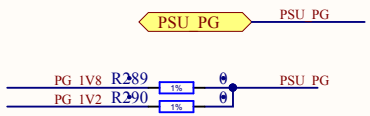


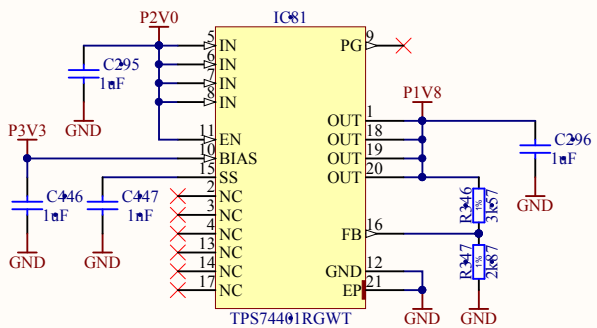






VIN	Vout	Lout	R1	R2	Rf	Cf(pF)	Cc(nF)	Rc(k) for Current Gain	Cp(pF)	Resistance
12	0.8	1.8	24.9	NI	NI	NI	NI	NI	15	3.6
12	1.0	2.5	24.9	100	1	150	15	0.825	NI	4
12	1.1	2.5	24.9	66.5	1	150	10	2	NI	20
12	1.2	2.5	24.9	49.9	1	150	10	2	NI	20
12	1.5	3.6	24.9	28.7	1	150	10	2.49	NI	20
12	1.8	3.6	24.9	20	1	150	10	2.49	NI	20
12	2.5	4.7	24.9	11.8	1	150	8.2	3.74	NI	25
12	3.3	4.7	24.9	7.87	1	150	6.8	4.99	NI	27
12	5.0	7.2	24.9	4.75	1	150	3.9	10	NI	27





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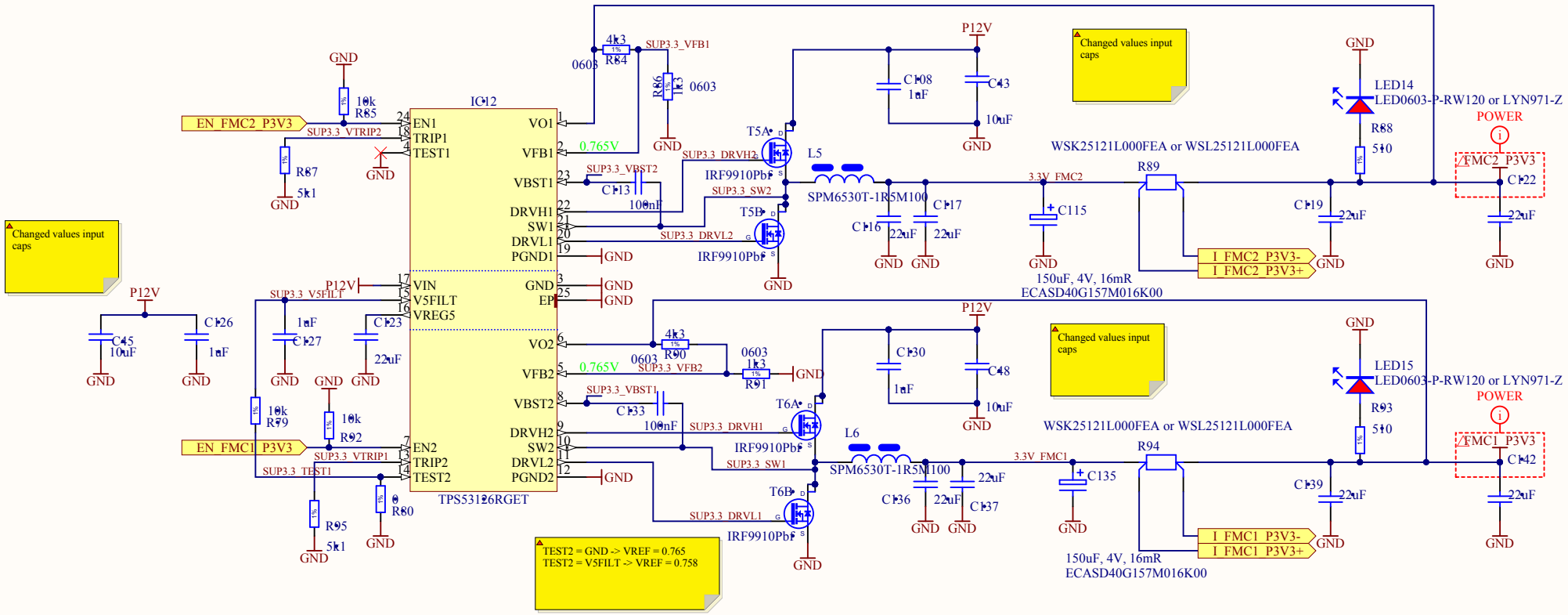

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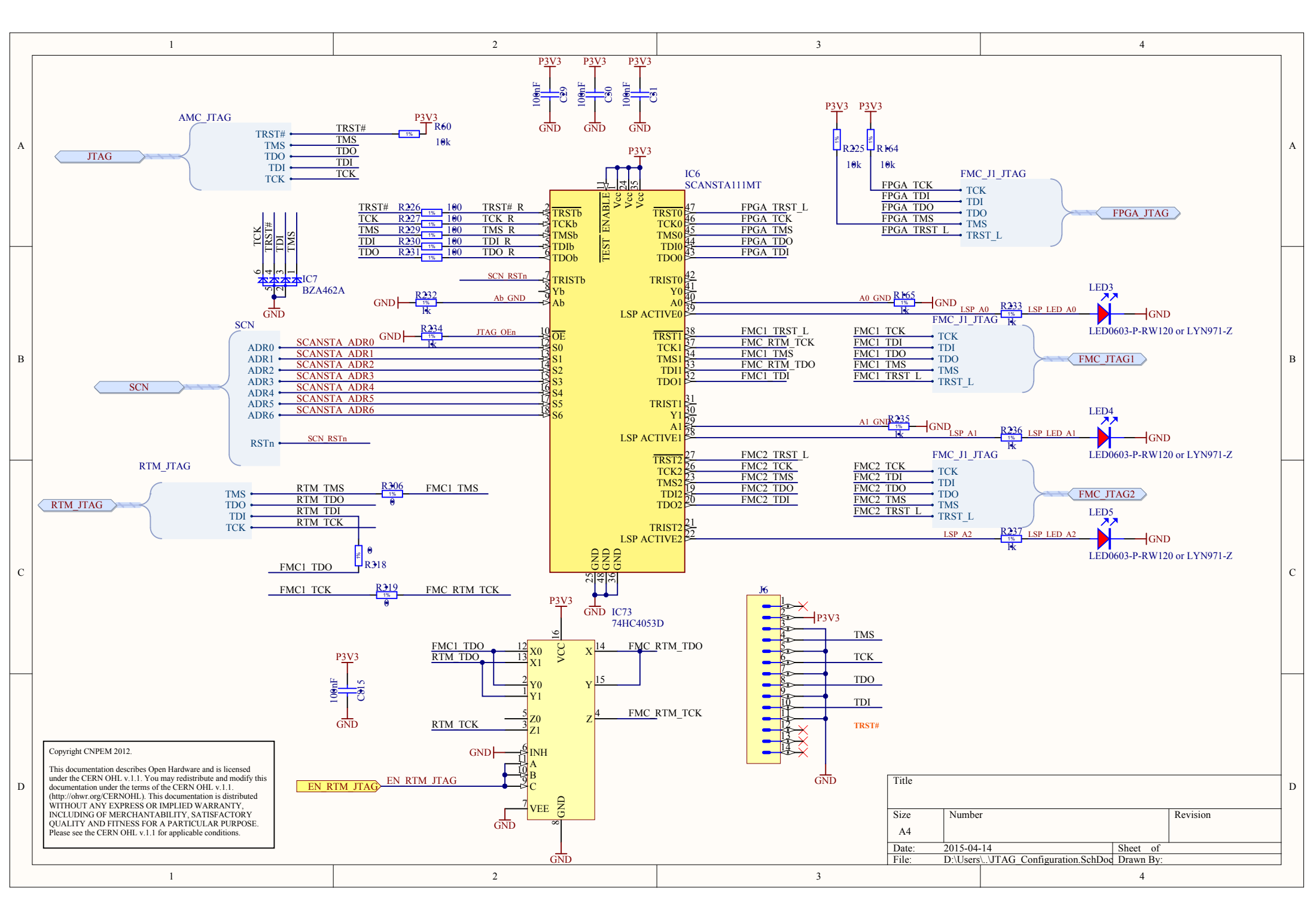
AMC_JTAG
JTAG
TRST#
TMS
TDO
TDI
TCK
P3V3
R60
10k
IC6
SCANSTA111MT
TRSTb
TCKb
TMSb
TDIb
TDOb
TEST_ENABLE
Vcc
TRST0
TCK0
TMS0
TDI0
TDO0
FPGA_TRST_L
FPGA_TCK
FPGA_TMS
FPGA_TDO
FPGA_TDI
FMC_J1_JTAG
FPGA_JTAG
R225
R164
IC7
BZA462A
SCN_RSTn
Ab_GND
A0_GND
A1_GND
JTAG_OEn
LSP_A0
LSP_A1
LSP_A2
LSP_LED_A0
LSP_LED_A1
LSP_LED_A2
LED3
LED4
LED5
LED0603-P-RW120 or LYN971-Z
SCN
ADR0
ADR1
ADR2
ADR3
ADR4
ADR5
ADR6
RSTn
SCANSTA_ADR0
SCANSTA_ADR1
SCANSTA_ADR2
SCANSTA_ADR3
SCANSTA_ADR4
SCANSTA_ADR5
SCANSTA_ADR6
OE
S0
S1
S2
S3
S4
S5
S6
LSP_ACTIVE0
LSP_ACTIVE1
LSP_ACTIVE2
FMC1_TRST_L
FMC_RTM_TCK
FMC1_TMS
FMC_RTM_TDO
FMC1_TDI
FMC1_TCK
FMC1_TDO
FMC2_TRST_L
FMC2_TCK
FMC2_TMS
FMC2_TDO
FMC2_TDI
FMC_JTAG1
FMC_JTAG2
RTM_JTAG
RTM_TMS
RTM_TDO
RTM_TDI
RTM_TCK
R306
R318
R319
IC73
74HC4053D
EN_RTM_JTAG
J6
C29
C30
C31
C45
100nF
GND
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Number
Revision
Date:
2015-04-14
Sheet of
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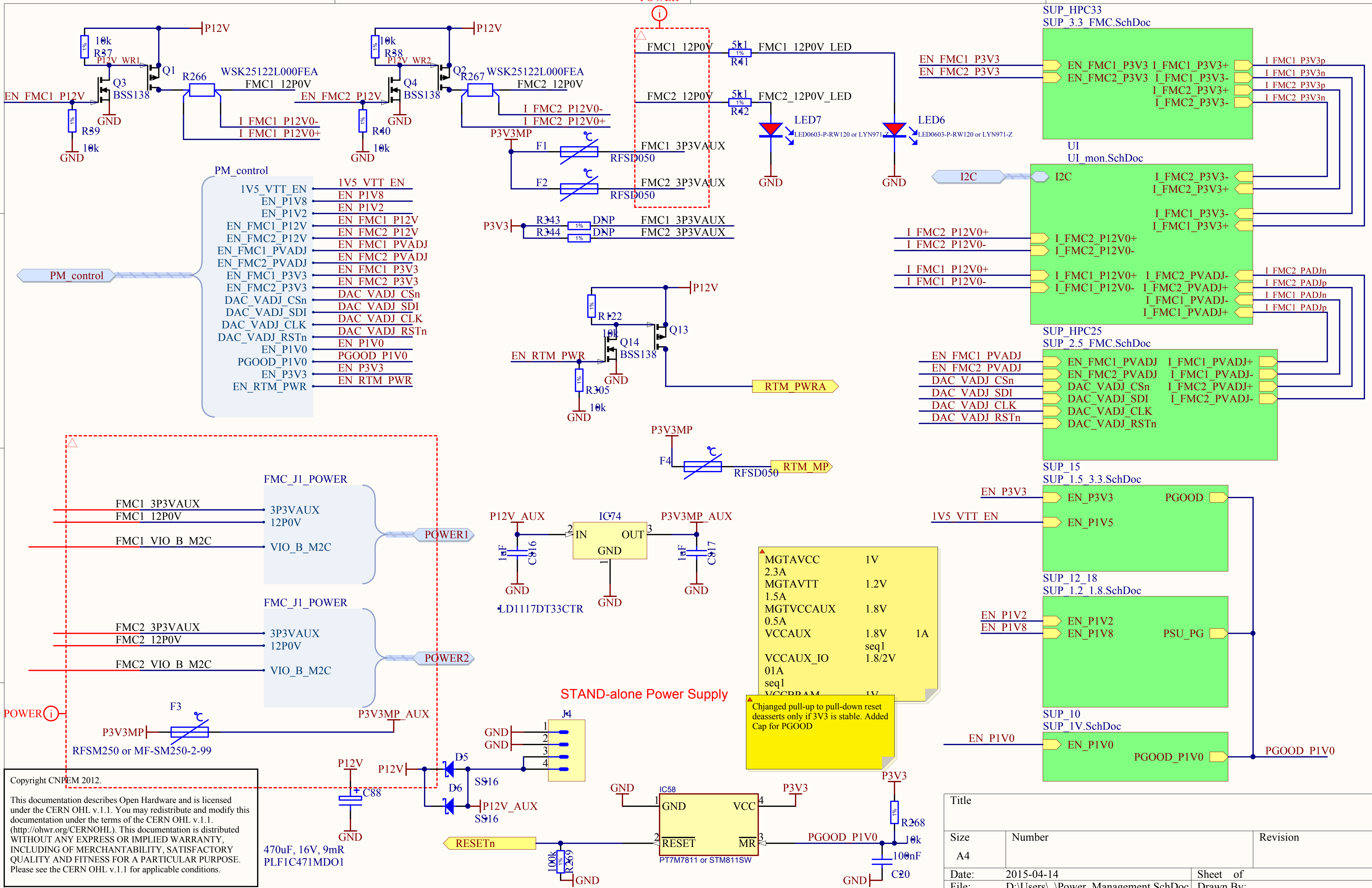
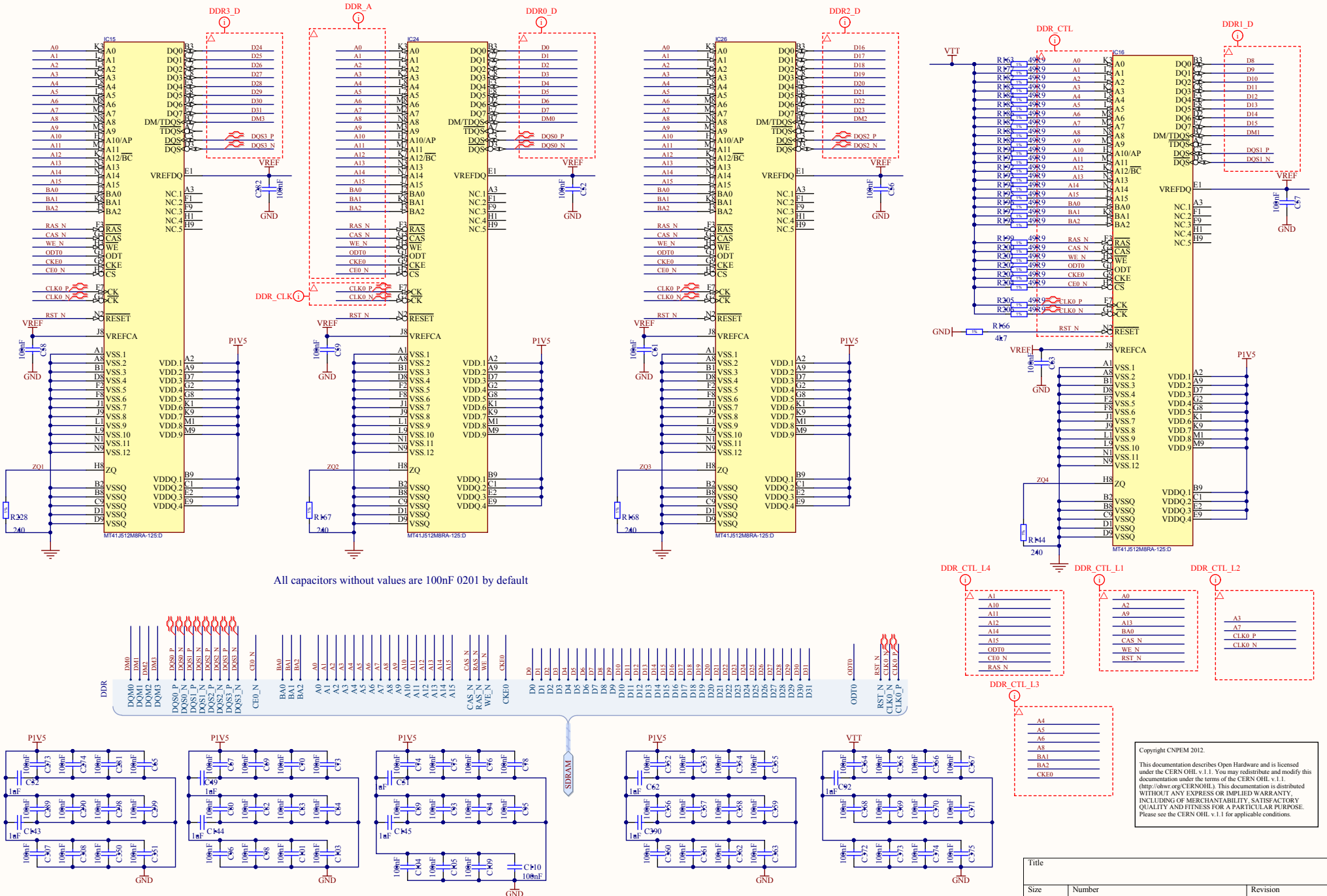
Drawn By:



POWER
P12V
10k
R37
P12V_WR1
Q1
Q3
BSS138
R266
WSK25122L000FEA
FMC1_12P0V
EN_FMC1_P12V
GND
R39
I_FMC1_P12V0-
I_FMC1_P12V0+
R38
P12V_WR2
Q2
Q4
R267
FMC2_12P0V
EN_FMC2_P12V
R40
I_FMC2_P12V0-
I_FMC2_P12V0+
P3V3MP
F1
F2
RFSD050
FMC1_3P3VAUX
FMC2_3P3VAUX
5k1
R41
R42
FMC1_12P0V_LED
FMC2_12P0V_LED
LED7
LED6
LED0603-P-RW120 or LYN971-Z
P3V3
R343
R344
DNP
PM_control
1V5_VTT_EN
EN_P1V8
EN_P1V2
EN_FMC1_P12V
EN_FMC2_P12V
EN_FMC1_PVADJ
EN_FMC2_PVADJ
EN_FMC1_P3V3
EN_FMC2_P3V3
DAC_VADJ_CSn
DAC_VADJ_SDI
DAC_VADJ_CLK
DAC_VADJ_RSTn
EN_P1V0
PGOOD_P1V0
EN_P3V3
EN_RTM_PWR
R122
Q13
Q14
R305
RTM_PWRA
F4
RTM_MP
SUP_HPC33
SUP_3.3_FMC.SchDoc
I_FMC1_P3V3+
I_FMC1_P3V3-
I_FMC2_P3V3+
I_FMC2_P3V3-
I_FMC1_P3V3p
I_FMC1_P3V3n
I_FMC2_P3V3p
I_FMC2_P3V3n
UI
UI_mon.SchDoc
I2C
I_FMC2_PVADJ-
I_FMC2_PVADJ+
I_FMC1_PVADJ-
I_FMC1_PVADJ+
I_FMC2_PADJn
I_FMC2_PADJp
I_FMC1_PADJn
I_FMC1_PADJp
SUP_HPC25
SUP_2.5_FMC.SchDoc
SUP_15
SUP_1.5_3.3.SchDoc
PGOOD
EN_P1V5
SUP_12_18
SUP_1.2_1.8.SchDoc
PSU_PG
SUP_10
SUP_1V.SchDoc
FMC_J1_POWER
3P3VAUX
12P0V
VIO_B_M2C
FMC1_VIO_B_M2C
FMC2_VIO_B_M2C
POWER1
POWER2
P12V_AUX
IC74
IN
OUT
1uF
C816
C817
P3V3MP_AUX
LD1117DT33CTR
MGTAVCC 1V
2.3A
MGTAVTT 1.2V
1.5A
MGTVCCAUX 1.8V
0.5A
VCCAUX 1.8V 1A
seq1
VCCAUX_IO 1.8/2V
01A
seq1
STAND-alone Power Supply
Chjanged pull-up to pull-down reset deasserts only if 3V3 is stable. Added Cap for PGOOD
F3
RFSM250 or MF-SM250-2-99
J4
D5
D6
SS16
C88
470uF, 16V, 9mR
PLF1C471MDO1
RESETn
IC58
GND
VCC
RESET
MR
PT7M7811 or STM811SW
R268
100nF
C20
100k
R269

Title		
Size: A4	Number	Revision
Date: 2015-04-14		Sheet of
File: D:\Users\..\Power_Management.SchDoc		Drawn By:


DDR3_D
DDR_A
DDR0_D
DDR2_D
DDR_CTL
DDR1_D
DDR_CLK
VTT
VREF
P1V5
GND
MT41J512M8RA-125:D
All capacitors without values are 100nF 0201 by default
DDR_CTL_L4
DDR_CTL_L1
DDR_CTL_L2
DDR_CTL_L3
SDRAM
DDR
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Size
A3
Number
Revision
Date: 2015-04-14
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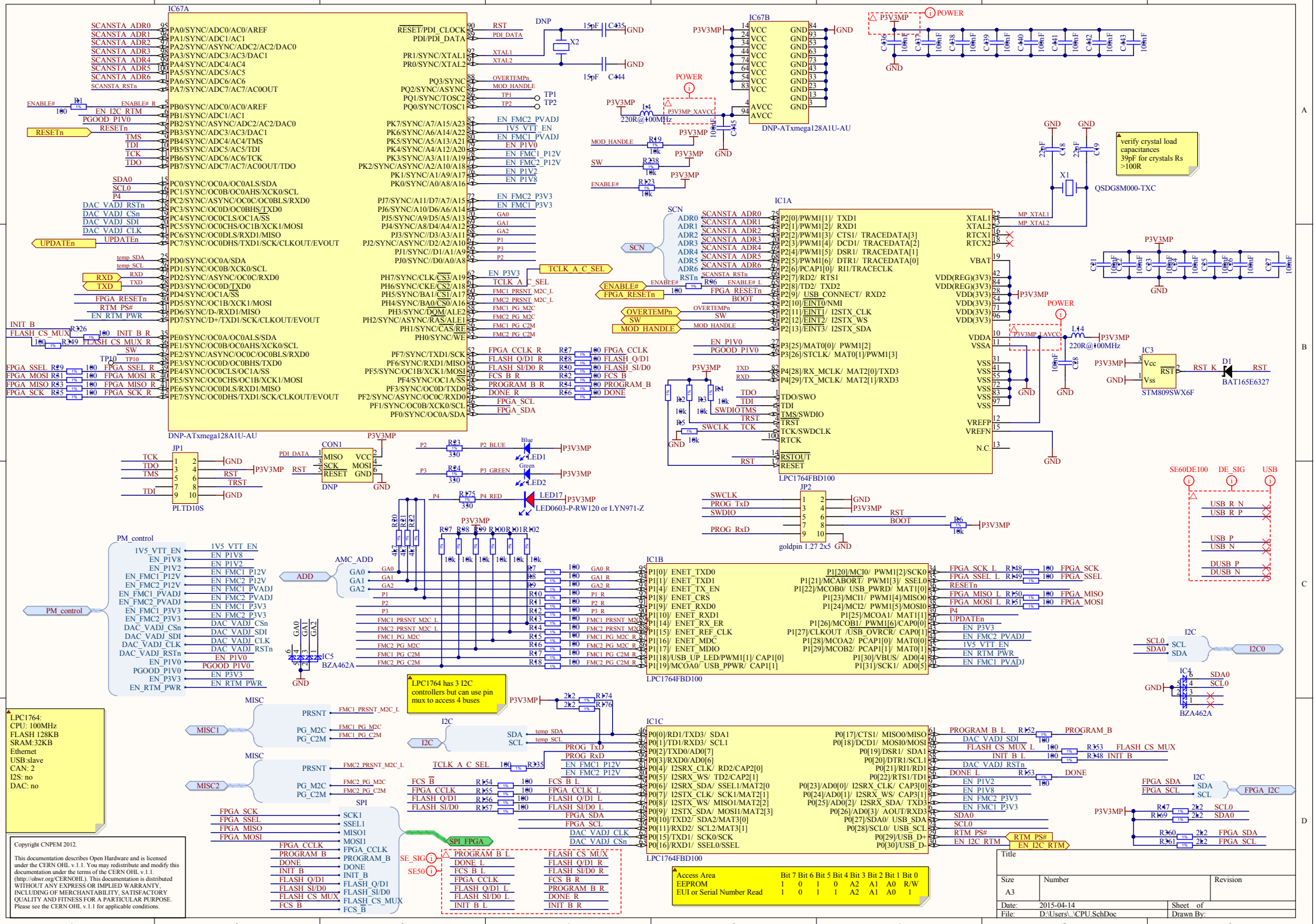
IC67A
DNP-ATxmega128A1U-AU
IC67B
DNP-ATxmega128A1U-AU
IC1A
LPC1764FBD100
IC1B
LPC1764FBD100
IC1C
LPC1764FBD100
PM_control
AMC_ADD
MISC
MISC1
MISC2
SPI
SPI_FPGA
I2C
I2C0
FPGA_I2C
JP1
PLTD10S
JP2
goldpin 1.27 2x5
CON1
DNP
IC3
STM809SWX6F
D1
BAT165E6327
IC4
BZA462A
IC5
BZA462A
X1
QSDG8M000-TXC
LED1
LED2
LED17
LED0603-P-RW120 or LYN971-Z
POWER
DNP
TP1
TP2
SCN
verify crystal load capacitances
39pF for crystals Rs >100R
LPC1764 has 3 I2C controllers but can use pin mux to access 4 buses
LPC1764:
CPU: 100MHz
FLASH 128KB
SRAM:32KB
Ethernet
USB:slave
CAN: 2
I2S: no
DAC: no
Access Area
EEPROM
EUI or Serial Number Read
Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0
1 0 1 0 A2 A1 A0 R/W
1 0 1 1 A2 A1 A0 1
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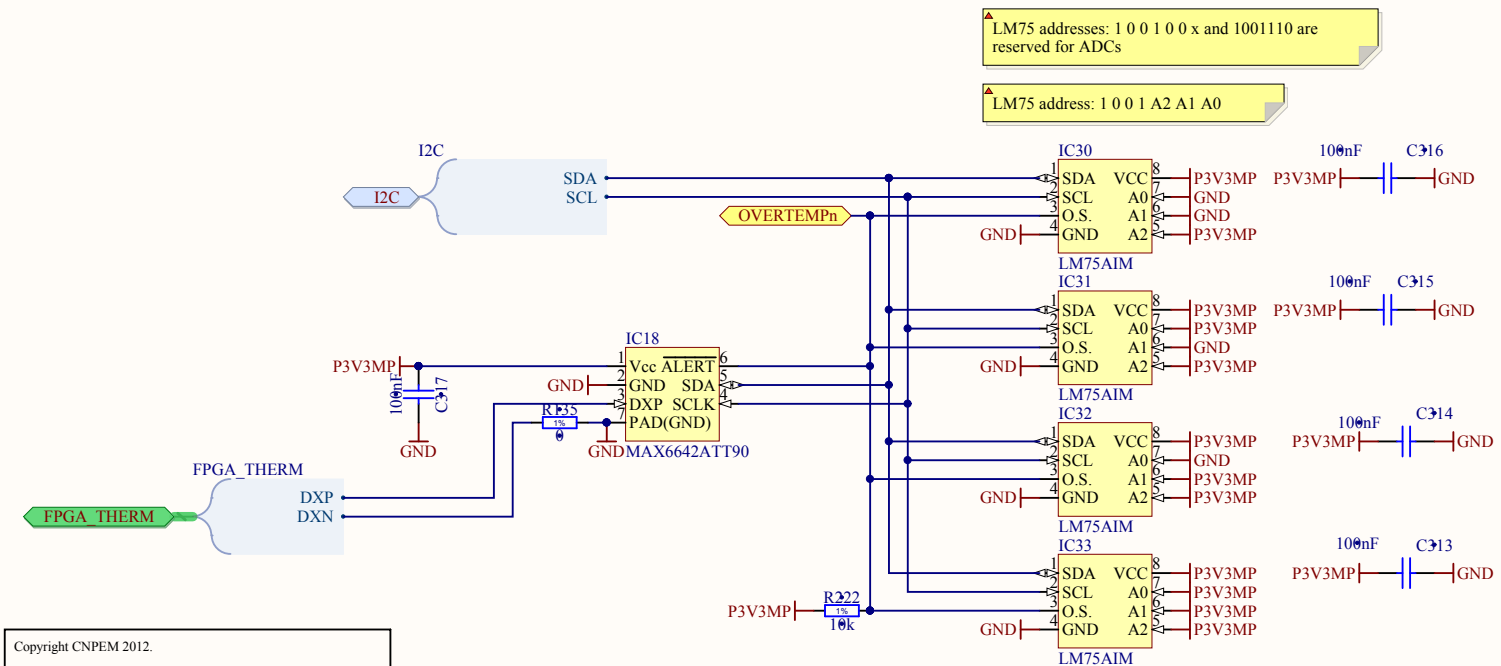
Title
Size A3
Number
Revision
Date: 2015-04-14
File: D:\Users\..\CPU.SchDoc
Sheet of
Drawn By:



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Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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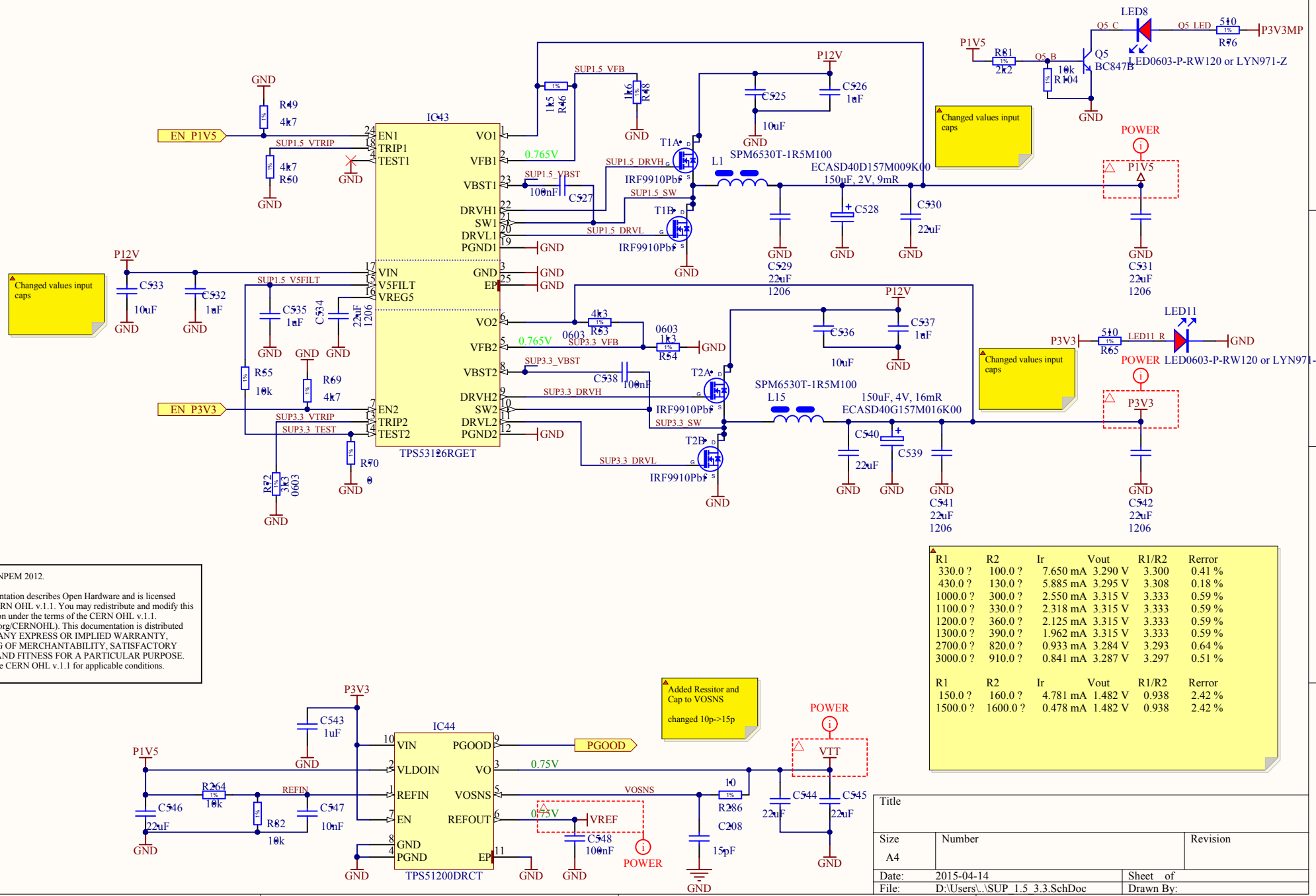

R1	R2	Ir	Vout	R1/R2	Rerror
330.0 ?	100.0 ?	7.650 mA	3.290 V	3.300	0.41 %
430.0 ?	130.0 ?	5.885 mA	3.295 V	3.308	0.18 %
1000.0 ?	300.0 ?	2.550 mA	3.315 V	3.333	0.59 %
1100.0 ?	330.0 ?	2.318 mA	3.315 V	3.333	0.59 %
1200.0 ?	360.0 ?	2.125 mA	3.315 V	3.333	0.59 %
1300.0 ?	390.0 ?	1.962 mA	3.315 V	3.333	0.59 %
2700.0 ?	820.0 ?	0.933 mA	3.284 V	3.293	0.64 %
3000.0 ?	910.0 ?	0.841 mA	3.287 V	3.297	0.51 %

R1	R2	Ir	Vout	R1/R2	Rerror
150.0 ?	160.0 ?	4.781 mA	1.482 V	0.938	2.42 %
1500.0 ?	1600.0 ?	0.478 mA	1.482 V	0.938	2.42 %

Title		
Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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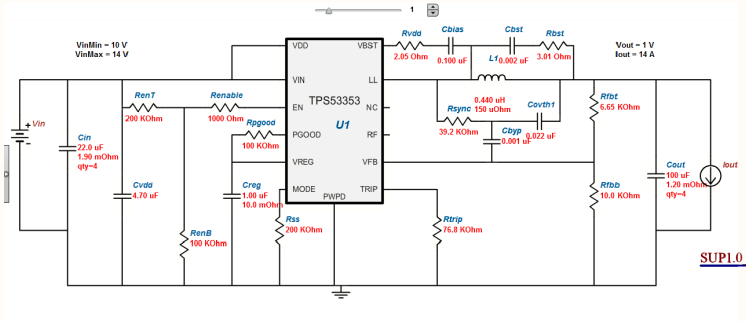

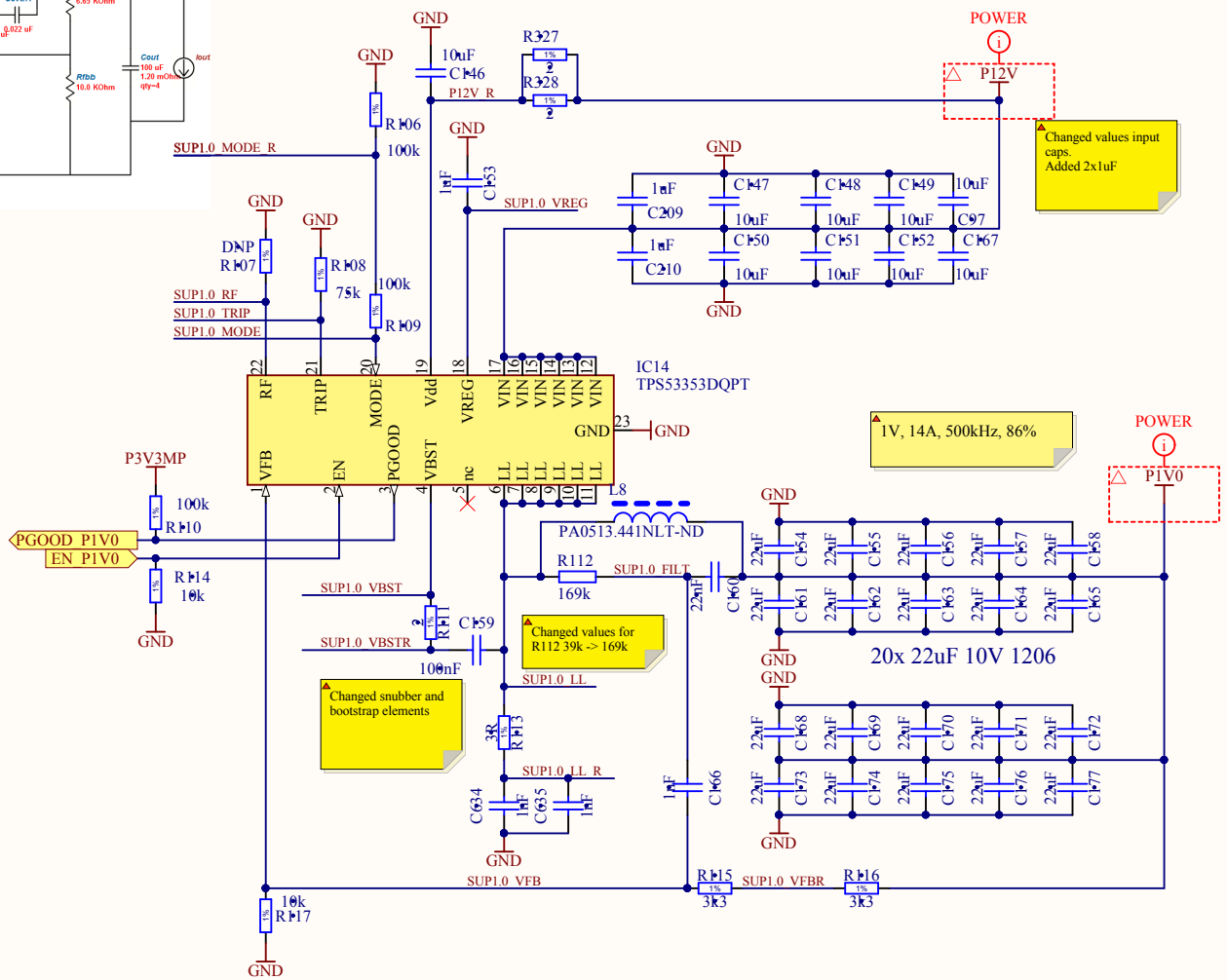

Title		
Size A4	Number	Revision
Date: 2015-04-14		Sheet of
File: D:\Users\..\SUP_1V.SchDoc		Drawn By:

VCCINT
3x330uF, 5x4.7uF

VCCAUX
4x47uF, 4x4.7uF

VCCBRAM
2x100uF, 5x4.7uF

C79T
XC7K325T-2FFG900C

C79S
XC7K325T-2FFG900C

C79P
XC7K325T-2FFG900C

C79R
XC7K325T-2FFG900C

C79Q
XC7K325T-2FFG900C

P1V0 — C106, C107, C226, 4.7uF C229, 4.7uF C230, 4.7uF C231, 4.7uF C232, 4.7uF C233
330uF, 2V, 9mR 330uF, 2V, 9mR 330uF, 2V, 9mR

L12 — ELLVGG1R0N — 1uH, 2.2A, 52mR Panasonic — P1V8 → VCCAUX
L23 — ELLVGG1R0N — 1uH, 2.2A, 52mR Panasonic — P2V0 → VCCAUX_IO
L10 — ELLVGG1R0N — 1uH, 2.2A, 52mR Panasonic — P1V0 → VCCBRAM

VCCAUX: C245, C246 4.7uF, C247, C248 4.7uF
VCCAUX_IO: C248 4.7uF
VCCBRAM: 100uF C235, 100uF C236, 4.7uF C237, 4.7uF C238, 4.7uF C239, 4.7uF C240, 4.7uF C241

POWER → FB6 → P1V0 → MGTAVCC
POWER → FB7 → P1V2 → MGTAVTT
POWER → FB1 → P1V8 → MGTVCCAUX

MGTAVTT — 1.2V+/- 0.3
MGTAVCC — 1V+/- 0.3
MGTVCCAUX — 1.8V+/- 0.5

MGTAVCC: C253–C256 22nF; C257–C259, C262 470nF; C263–C266 1uF, 4.7uF
MGTAVTT: C267–C270 22nF; C271–C276 470nF; C277–C280 1uF, 4.7uF
MGTVCCAUX: C249, C250 22nF; C251 1uF; C252 4.7uF

Changed TL431QDBVT -> TS3431
This gives 1.25V instead of 2.5V

Changed pinout Pin1 = REF, Pin2 = Cathode

P1V0 — 1V+/- 0.3 — VCCBRAM — 1V+/- 0.3
P3V3 — C260 470nF
VP_0 R15, VN_0 T14
VREFP_0 L15, VREFN_0 K14 → GND
POWER → VREF_XDAC → R213 1% 330 → P3V3
C613 470nF
IC45 TS3431
GNDADC_0 P14 → GND; VCCADC_0 P15 → VCCAUX
1.8V+/- 0.9 — C614 470nF
VCCAUX_IO — 1.8V+/- 0.9 — VCCAUX_IO_G0
VCCAUX — 1.8V+/- 0.9 — VCCAUX
VCCBATT_0 C10 → VCCBATT — 1...1.89V
POWER → VCCBATT → C615 470nF → BH1 SR60 Keystone 2998 → BAT1 SR60 battery

P3V3 → P1V5
PVADJ2 → PVADJ2_1V8
PVADJ1 → PVADJ1

PVADJ2_1V8: C284 100uF
PVADJ2: C283, C285, C286 100uF
PVADJ1: C287, C288, C291, C292 100uF
P1V5: C293, C294 100uF

MGTAVCC	1V	2.3A		
MGTAVTT	1.2V	1.5A		
MGTVCCAUX	1.8V	0.5A		
VCCAUX	1.8V	1A		seq1
VCCAUX_IO	1.8/2V	01A		seq1
VCCBRAM	1V	1.8A		seq0
VCCINT	1V	6A		seq0
VCCO_1.2		1.2V	3.2A	seq2
VCCO_1.35	1.35V	0.9A		seq2
VCCO_1.5		1.5V	0.9A	seq2
VCCO_1.8		1.8V	0.9A	seq2
VCCO_2.5		2.5V	0.9A	seq2
VCCO_3.3		3.3V	0.9A	seq2

power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX
power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.
When VMGTAVTT is powered before VMGTAVCC and VMGTAVTT ? VMGTAVCC > 150 mV and VMGTAVCC < 0.7V, the VMGTAVTT current draw can increase by 460 mA per transceiver during VMGTAVCC ramp up. The duration of the current draw can be up to 0.3 x TMGTAVCC (ramp time from GND to 90% of VMGTAVCC). The reverse is true for power-down.
? When VMGTAVTT is powered before VCCINT and VMGTAVTT ? VCCINT > 150 mV and VCCINT < 0.7V, the VMGTAVTT current draw can increase by 50 mA per transceiver during VCCINT ramp up. The duration of the current draw can be up to 0.3 x TVCCINT (ramp time from GND to 90% of VCCINT). The reverse is true for power-down.

Title		
Size A3	Number	Revision
Date: 2015-04-14		Sheet of
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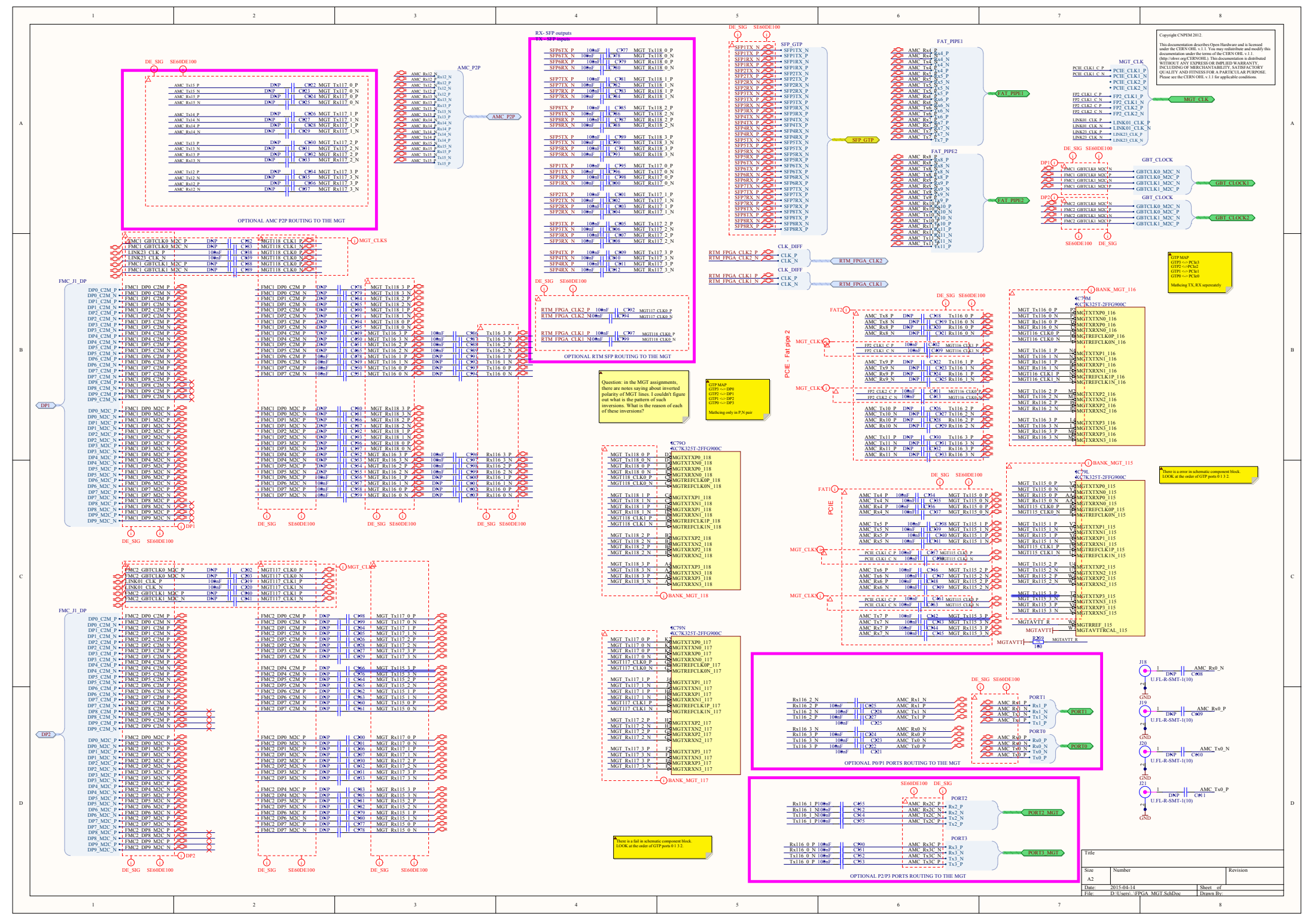
AMC_P2P
OPTIONAL AMC P2P ROUTING TO THE MGT
RX- SFP outputs
TX- SFP inputs
RTM_FPGA_CLK2_P
RTM_FPGA_CLK2_N
RTM_FPGA_CLK1_P
RTM_FPGA_CLK1_N
OPTIONAL RTM SFP ROUTING TO THE MGT
SFP_GTP
FAT_PIPE1
FAT_PIPE2
MGT_CLK
GBT_CLOCK
GBT_CLOCK1
GBT_CLOCK2
RTM_FPGA_CLK2
RTM_FPGA_CLK1
CLK_DIFF
FMC_J1_DP
FMC_J1_DP
BANK_MGT_116
BANK_MGT_115
BANK_MGT_118
BANK_MGT_117
PCIE - Fat pipe 2
PCIE
OPTIONAL P0/P1 PORTS ROUTING TO THE MGT
OPTIONAL P2/P3 PORTS ROUTING TO THE MGT
PORT1
PORT0
PORT2_MGT
PORT3_MGT
Question: in the MGT assignments, there are notes saying about inverted polarity of MGT lines. I couldn't figure out what is the pattern of such inversions. What is the reason of each of these inversions?
GTP MAP
GTP3 <-> DP0
GTP2 <-> DP1
GTP1 <-> DP2
GTP0 <-> DP3
Mathcing only in P,N pair
GTP MAP
GTP3 <-> PCIe3
GTP2 <-> PCIe2
GTP1 <-> PCIe1
GTP0 <-> PCIe0
Mathcing TX, RX seperately
There is a fail in schematic component block. LOOK at the order of GTP ports 0 1 3 2.
There is a error in schematic component block. LOOK at the order of GTP ports 0 1 3 2.
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Title
Size
A2
Number
Revision
Date: 2015-04-14
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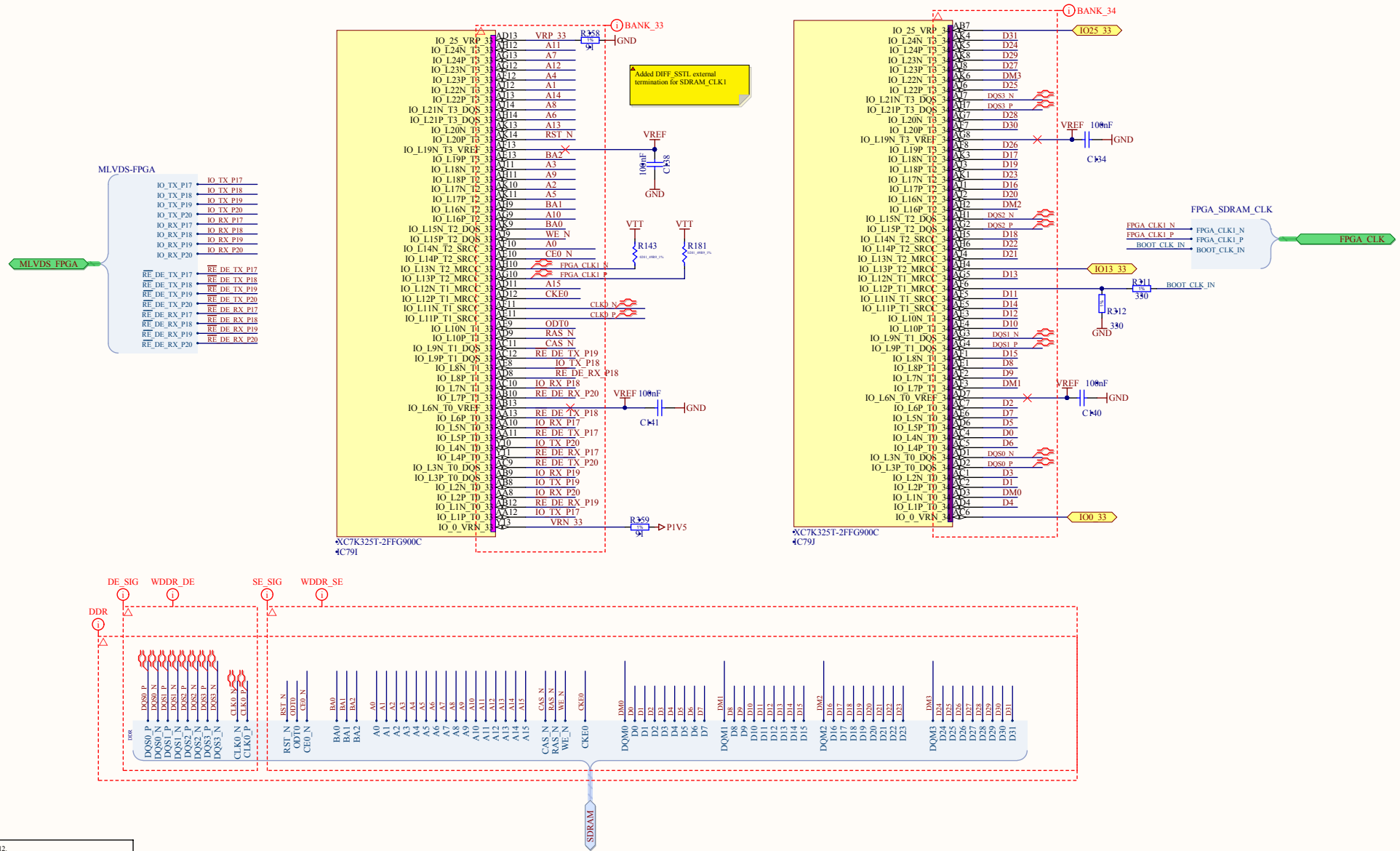
Sheet of
Drawn By:



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Size: A3	Number	Revision
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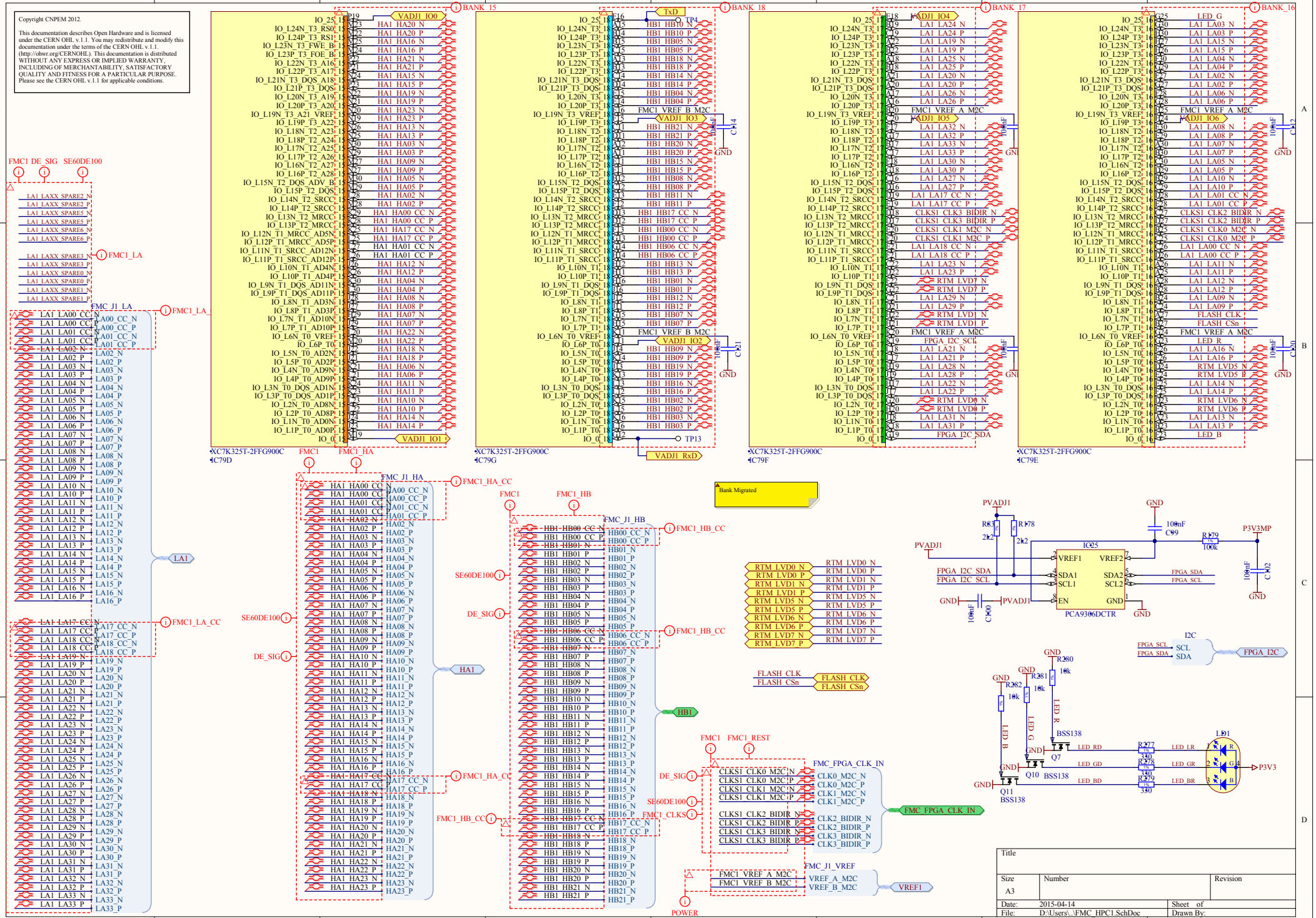

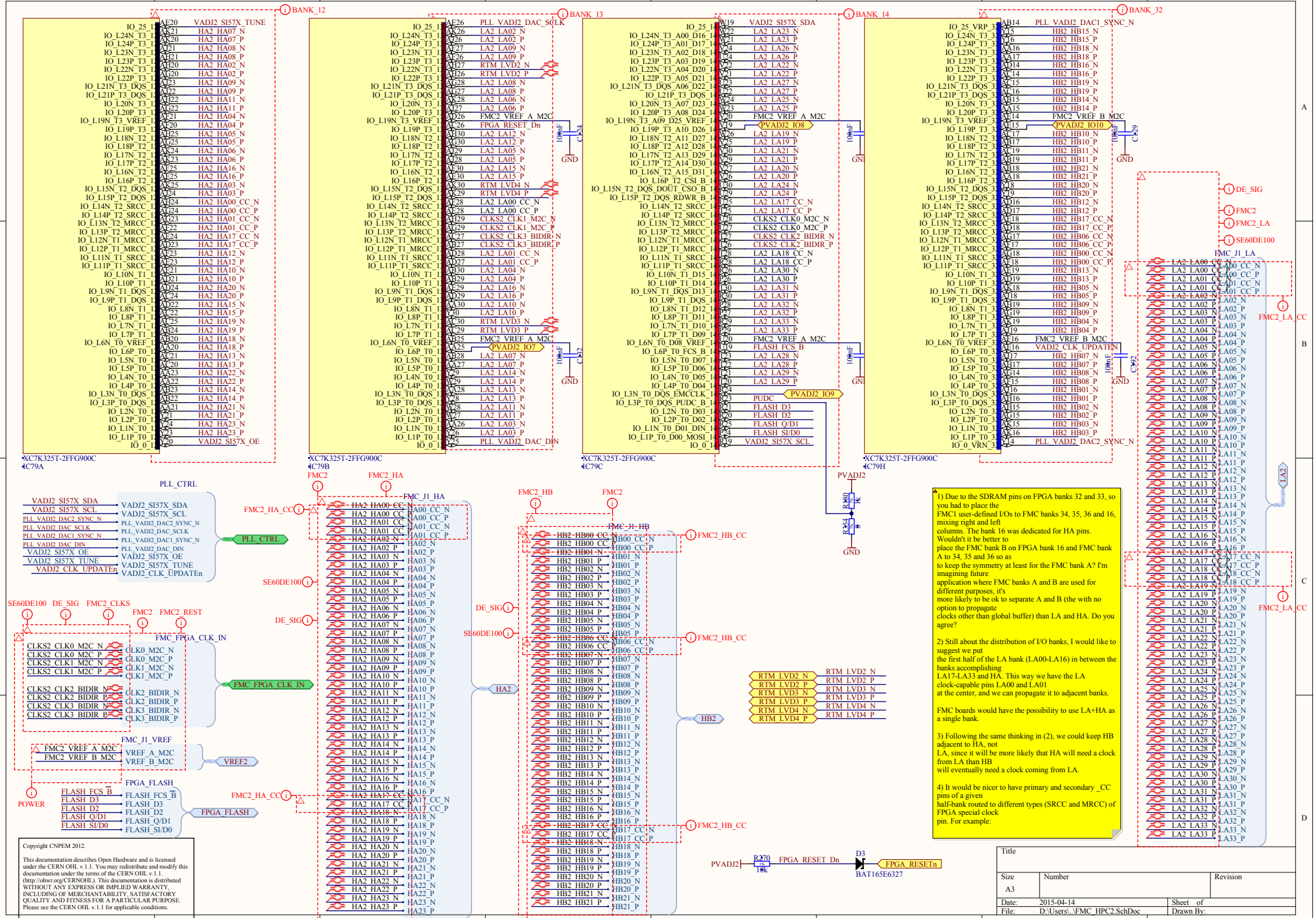

1) Due to the SDRAM pins on FPGA banks 32 and 33, so you had to place the FMC1 user-defined I/Os to FMC banks 34, 35, 36 and 16, mixing right and left columns. The bank 16 was dedicated for HA pins. Wouldn't it be better to place the FMC bank B on FPGA bank 16 and FMC bank A to 34, 35 and 36 so as to keep the symmetry at least for the FMC bank A? I'm imagining future application where FMC banks A and B are used for different purposes, it's more likely to be ok to separate A and B (the with no option to propagate clocks other than global buffer) than LA and HA. Do you agree?

2) Still about the distribution of I/O banks, I would like to suggest we put the first half of the LA bank (LA00-LA16) in between the banks accomplishing LA17-LA33 and HA. This way we have the LA clock-capable pins LA00 and LA01 at the center, and we can propagate it to adjacent banks.

FMC boards would have the possibility to use LA+HA as a single bank.

3) Following the same thinking in (2), we could keep HB adjacent to HA, not LA, since it will be more likely that HA will need a clock from LA than HB will eventually need a clock coming from LA.

4) It would be nicer to have primary and secondary _CC pins of a given half-bank routed to different types (SRCC and MRCC) of FPGA special clock pin. For example:

Title		
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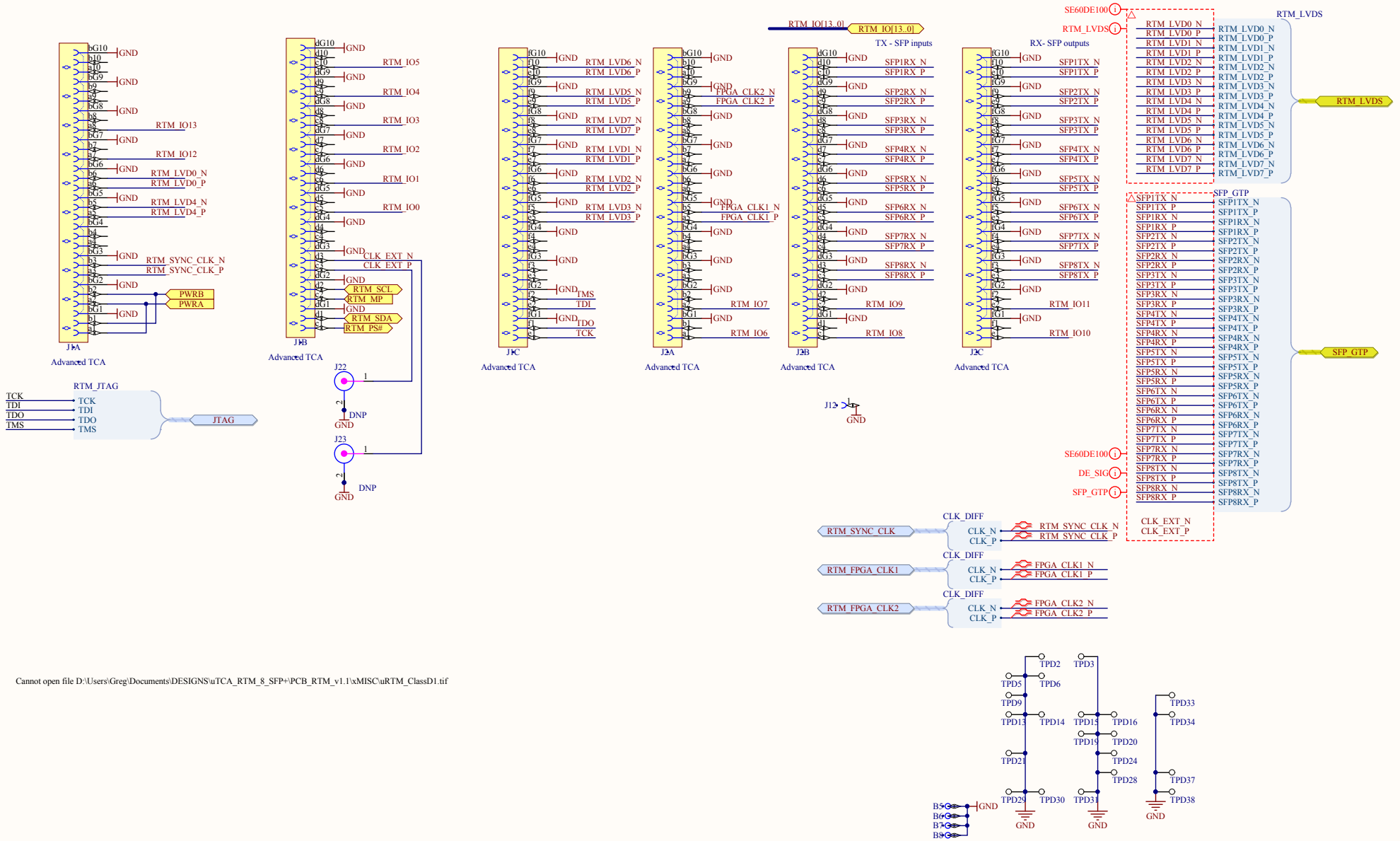

Cannot open file D:\Users\Greg\Documents\DESIGNS\uTCA_RTM_8_SFP+\PCB_RTM_v1.1\xMISC\uRTM_ClassD1.tif

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Size: A3	Number	Revision
Date: 2015-04-14		Sheet of
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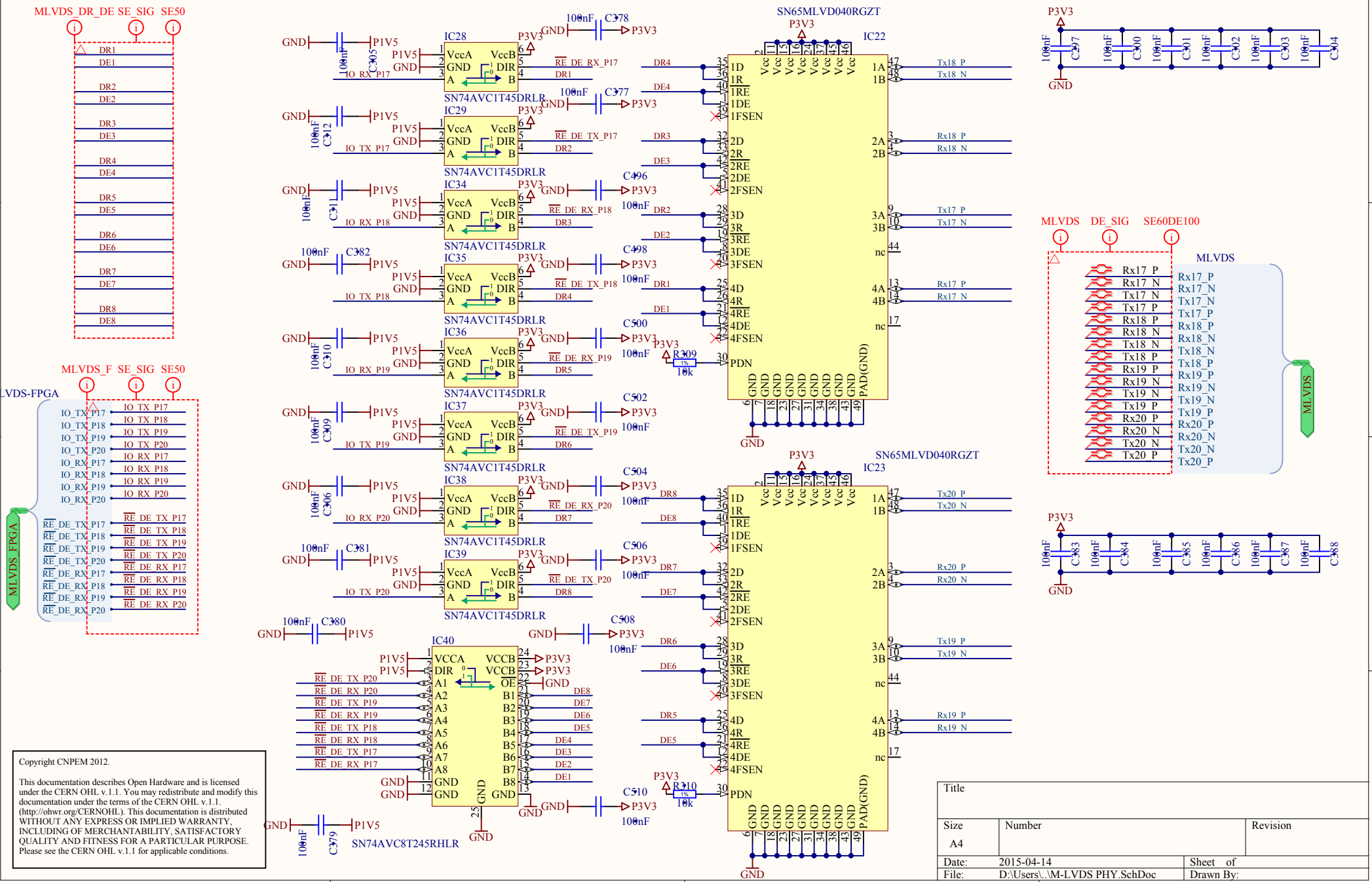

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Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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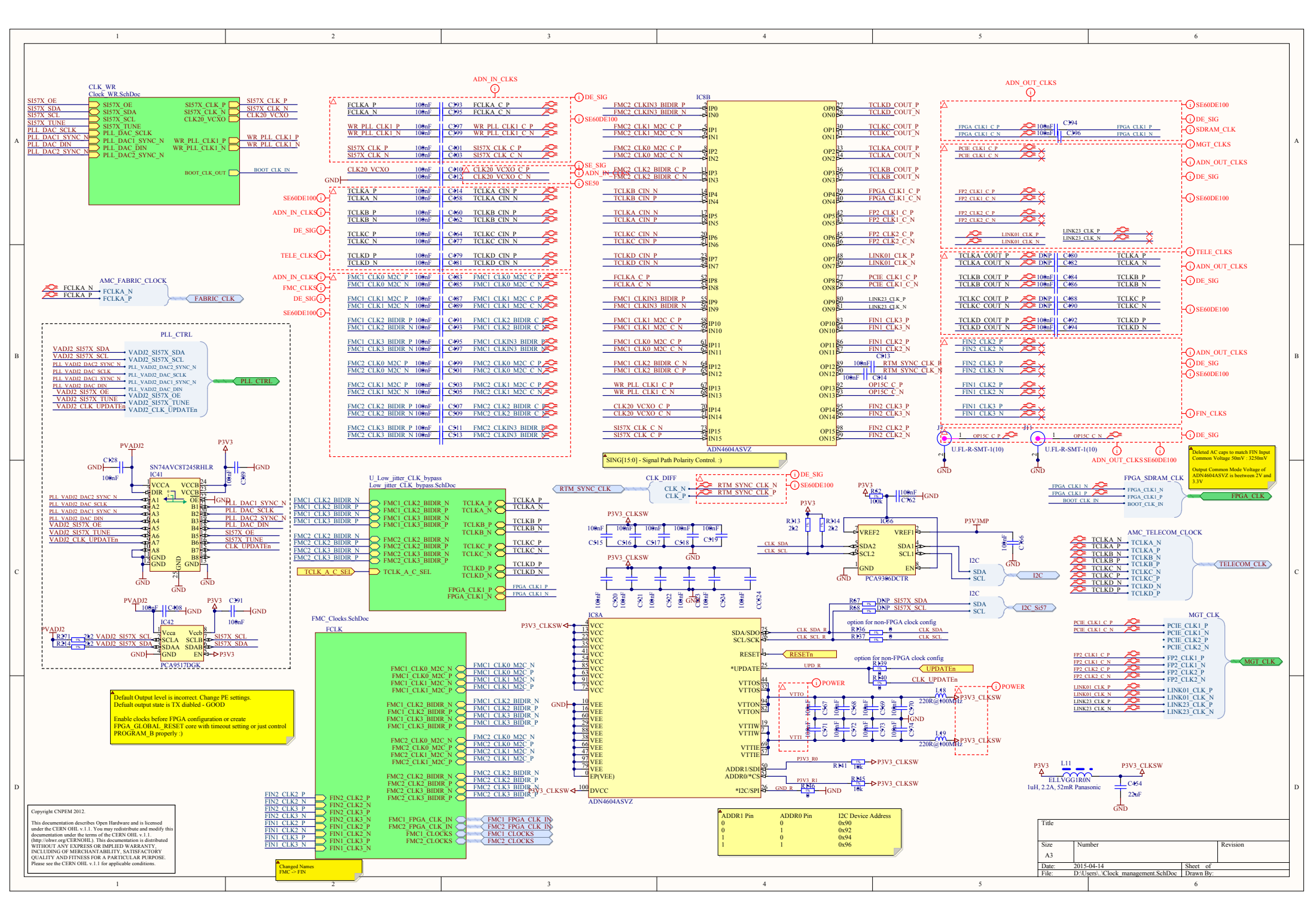
CLK_WR
Clock_WR.SchDoc
SI57X_OE
SI57X_SDA
SI57X_SCL
SI57X_TUNE
PLL_DAC_SCLK
PLL_DAC1_SYNC_N
PLL_DAC_DIN
PLL_DAC2_SYNC_N
SI57X_CLK_P
SI57X_CLK_N
CLK20_VCXO
WR_PLL_CLK1_P
WR_PLL_CLK1_N
BOOT_CLK_OUT
BOOT_CLK_IN
ADN_IN_CLKS
DE_SIG
SE60DE100
SE_SIG
ADN_IN_CLKS
SE50
IC8B
ADN4604ASVZ
ADN_OUT_CLKS
SDRAM_CLK
MGT_CLKS
TELE_CLKS
FIN_CLKS
AMC_FABRIC_CLOCK
FABRIC_CLK
PLL_CTRL
IC41
SN74AVC8T245RHLR
IC42
PCA9517DGK
U_Low_jitter_CLK_bypass
Low_jitter_CLK_bypass.SchDoc
TCLK_A_C_SEL
CLK_DIFF
RTM_SYNC_CLK
IC66
PCA9306DCTR
FPGA_SDRAM_CLK
FPGA_CLK
AMC_TELECOM_CLOCK
TELECOM_CLK
MGT_CLK
FMC_Clocks.SchDoc
FCLK
IC8A
ADN4604ASVZ
RESETn
UPDATEn
POWER
L48
L49
220R@100MHz
L11
ELLVGG1R0N
1uH, 2.2A, 52mR Panasonic
I2C
I2C_Si57
U.FL-SMT-1(10)
Default Output level is incorrect. Change PE settings.
Default output state is TX diabled - GOOD
Enable clocks before FPGA configuration or create
FPGA_GLOBAL_RESET core with timeout setting or just control
PROGRAM_B properly :)
Changed Names
FMC -> FIN
SING[15:0] - Signal Path Polarity Control. :)
Deleted AC caps to match FIN Input
Common Voltage 50mV - 3250mV
Output Common Mode Voltage of
ADN4604ASVZ is beetween 2V and
3.3V
ADDR1 Pin
ADDR0 Pin
I2C Device Address
0 0 0x90
0 1 0x92
1 0 0x94
1 1 0x96
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Size
A3
Number
Revision
Date: 2015-04-14
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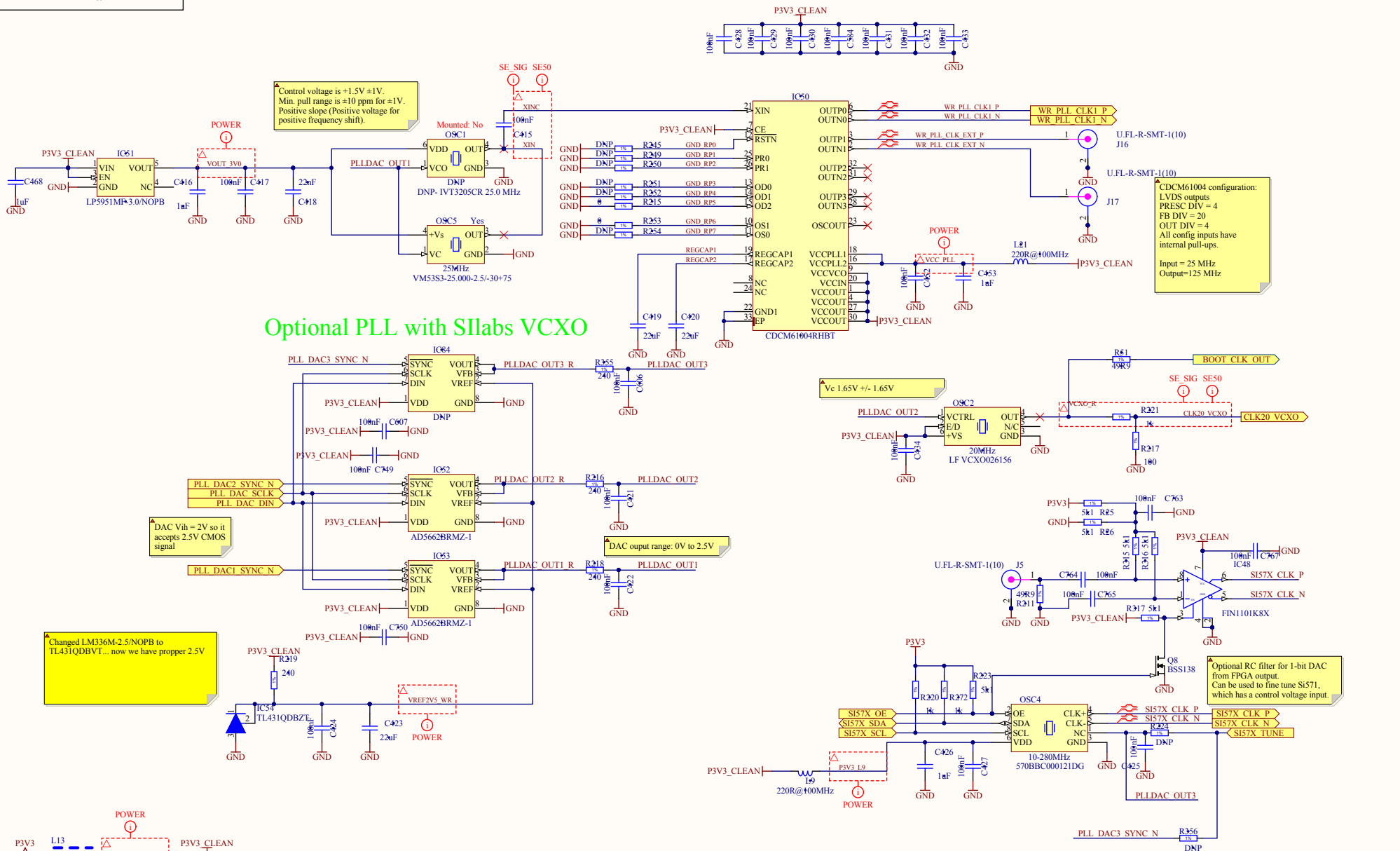


Title		
Size: A3	Number	Revision
Date: 2015-04-14		Sheet of
File: D:\Users\..\Clock_WR.SchDoc		Drawn By:

SATA naming is relative to HOST

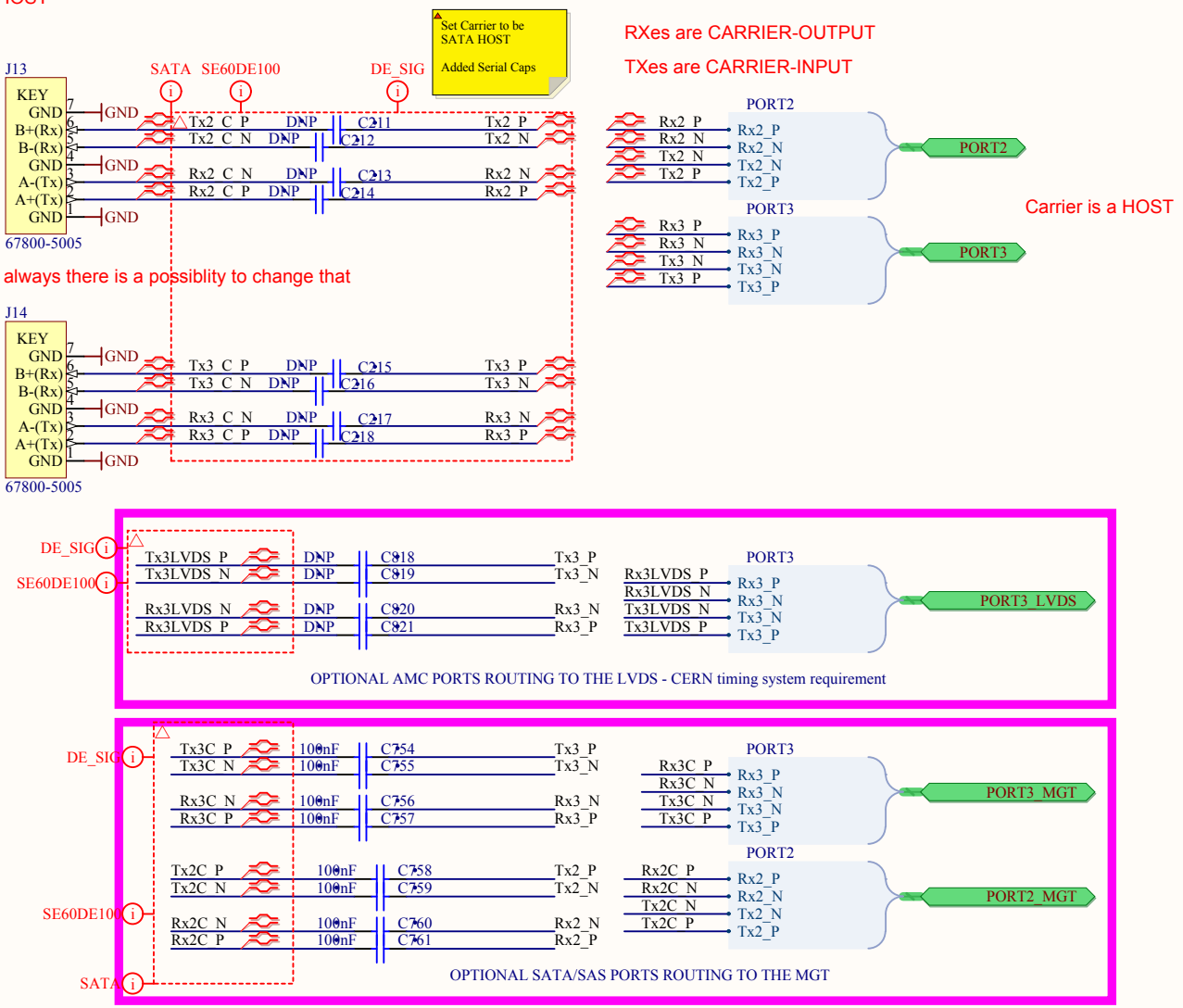
Apply to all AMC ports: see table 6-1 PICMG AMC.0 R2.0 1.5.11.2006

For normal SATA cables apply:

B = HOST SATA RX

A = HOST SATA TX

There also Exist a Cross-Over SATA Cable so always there is a possiblity to change that



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Date: 2015-04-14		Sheet of
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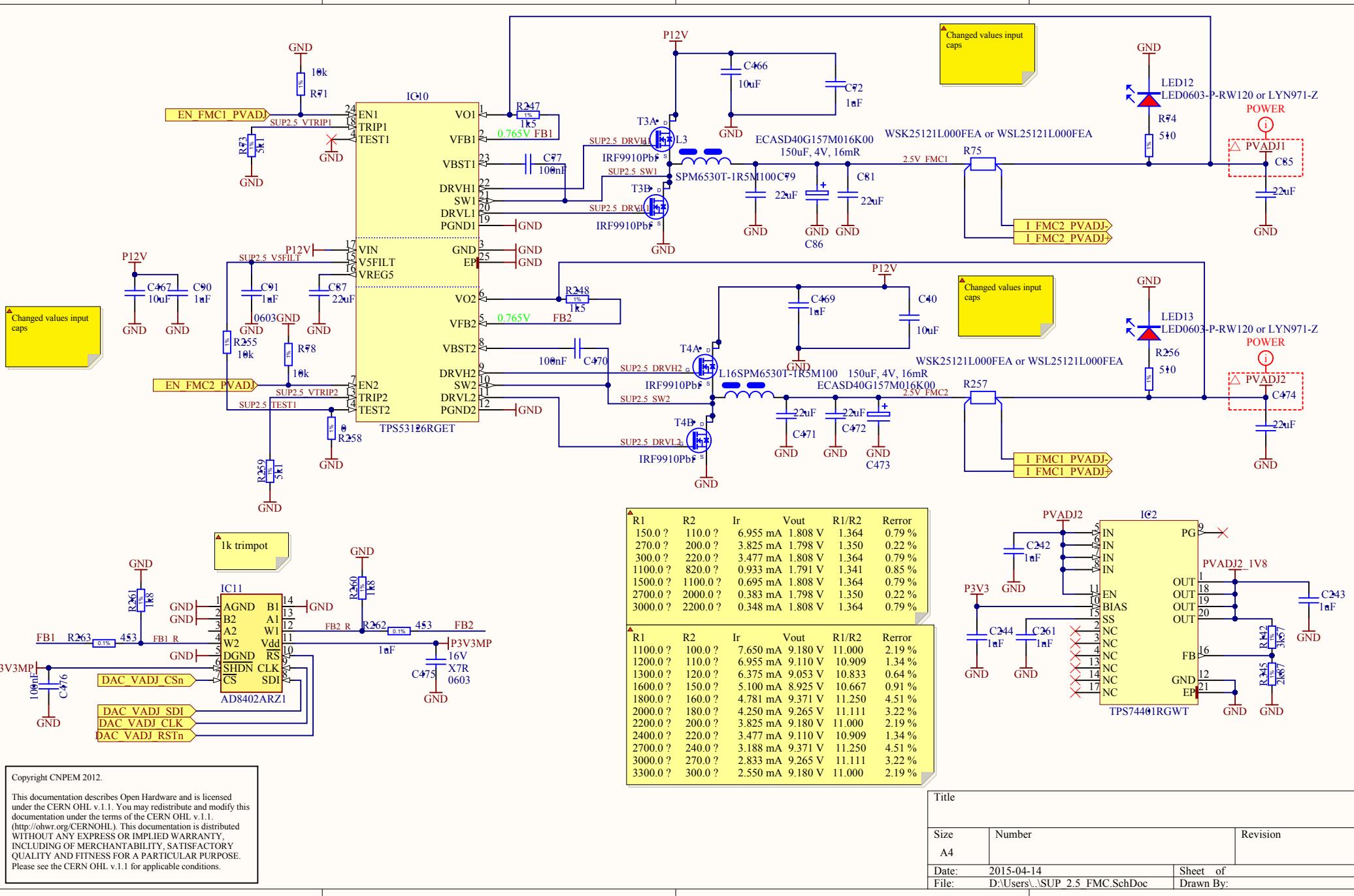

R1	R2	Ir	Vout	R1/R2	Rerror
150.0 ?	110.0 ?	6.955 mA	1.808 V	1.364	0.79 %
270.0 ?	200.0 ?	3.825 mA	1.798 V	1.350	0.22 %
300.0 ?	220.0 ?	3.477 mA	1.808 V	1.364	0.79 %
1100.0 ?	820.0 ?	0.933 mA	1.791 V	1.341	0.85 %
1500.0 ?	1100.0 ?	0.695 mA	1.808 V	1.364	0.79 %
2700.0 ?	2000.0 ?	0.383 mA	1.798 V	1.350	0.22 %
3000.0 ?	2200.0 ?	0.348 mA	1.808 V	1.364	0.79 %

R1	R2	Ir	Vout	R1/R2	Rerror
1100.0 ?	100.0 ?	7.650 mA	9.180 V	11.000	2.19 %
1200.0 ?	110.0 ?	6.955 mA	9.110 V	10.909	1.34 %
1300.0 ?	120.0 ?	6.375 mA	9.053 V	10.833	0.64 %
1600.0 ?	150.0 ?	5.100 mA	8.925 V	10.667	0.91 %
1800.0 ?	160.0 ?	4.781 mA	9.371 V	11.250	4.51 %
2000.0 ?	180.0 ?	4.250 mA	9.265 V	11.111	3.22 %
2200.0 ?	200.0 ?	3.825 mA	9.180 V	11.000	2.19 %
2400.0 ?	220.0 ?	3.477 mA	9.110 V	10.909	1.34 %
2700.0 ?	240.0 ?	3.188 mA	9.371 V	11.250	4.51 %
3000.0 ?	270.0 ?	2.833 mA	9.265 V	11.111	3.22 %
3300.0 ?	300.0 ?	2.550 mA	9.180 V	11.000	2.19 %

Title		
Size A4	Number	Revision
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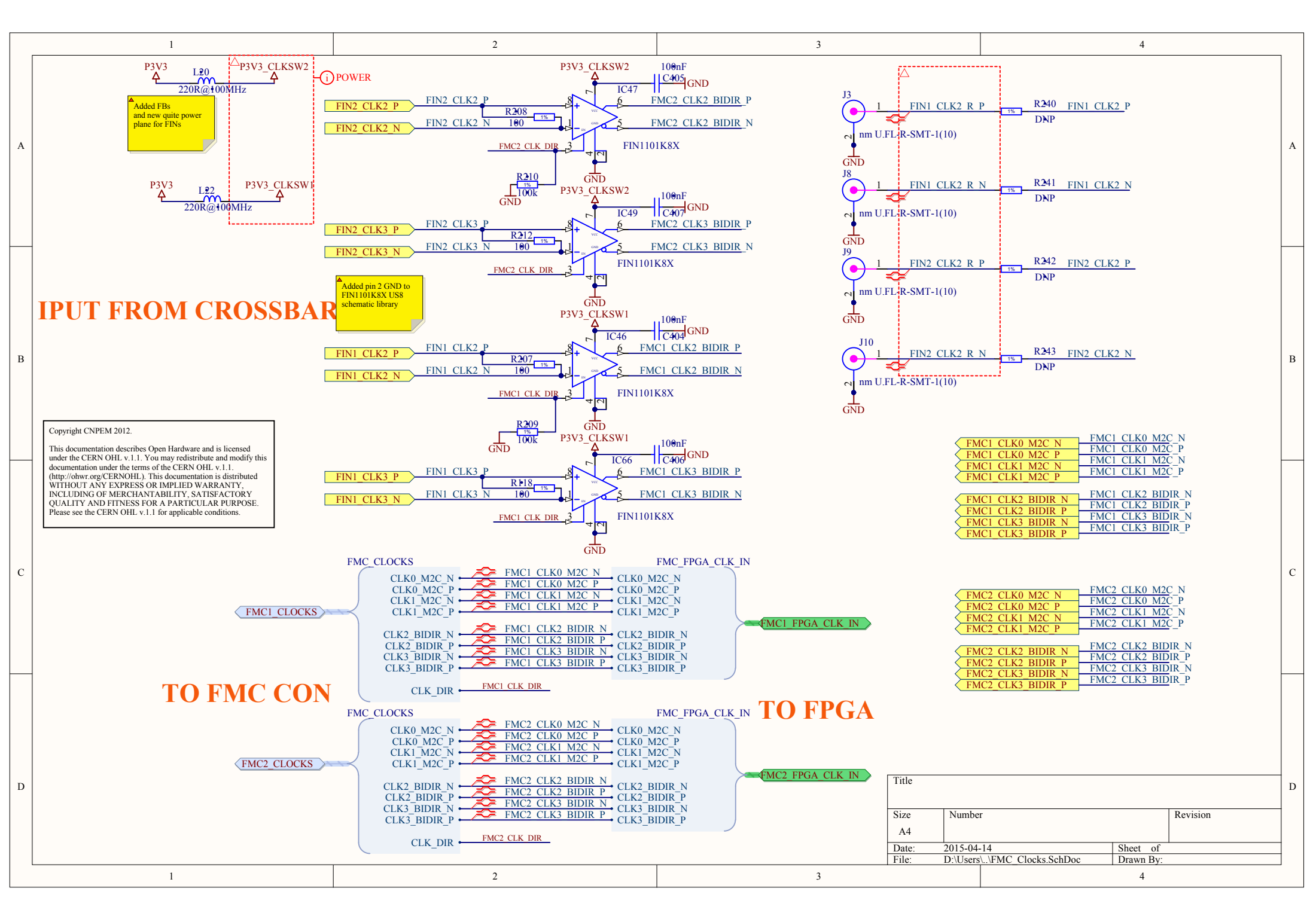
P3V3
L20
220R@100MHz
P3V3_CLKSW2
Added FBs
and new quite power
plane for FINs
POWER
P3V3
L22
220R@100MHz
P3V3_CLKSW1
IPUT FROM CROSSBAR
Added pin 2 GND to
FIN1101K8X US8
schematic library
FIN2_CLK2_P
FIN2_CLK2_N
FIN2_CLK3_P
FIN2_CLK3_N
FIN1_CLK2_P
FIN1_CLK2_N
FIN1_CLK3_P
FIN1_CLK3_N
FMC2_CLK_DIR
FMC1_CLK_DIR
R208
R210
R212
R207
R209
R218
100
100k
1%
GND
100nF
C405
C407
C404
C406
IC47
IC49
IC46
IC66
FIN1101K8X
FMC2_CLK2_BIDIR_P
FMC2_CLK2_BIDIR_N
FMC2_CLK3_BIDIR_P
FMC2_CLK3_BIDIR_N
FMC1_CLK2_BIDIR_P
FMC1_CLK2_BIDIR_N
FMC1_CLK3_BIDIR_P
FMC1_CLK3_BIDIR_N
J3
J8
J9
J10
FIN1_CLK2_R_P
FIN1_CLK2_R_N
FIN2_CLK2_R_P
FIN2_CLK2_R_N
R240
R241
R242
R243
DNP
nm U.FL-R-SMT-1(10)
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FMC_CLOCKS
FMC_FPGA_CLK_IN
FMC1_CLOCKS
FMC1_FPGA_CLK_IN
FMC2_CLOCKS
FMC2_FPGA_CLK_IN
CLK0_M2C_N
CLK0_M2C_P
CLK1_M2C_N
CLK1_M2C_P
CLK2_BIDIR_N
CLK2_BIDIR_P
CLK3_BIDIR_N
CLK3_BIDIR_P
CLK_DIR
TO FMC CON
TO FPGA
Title
Size
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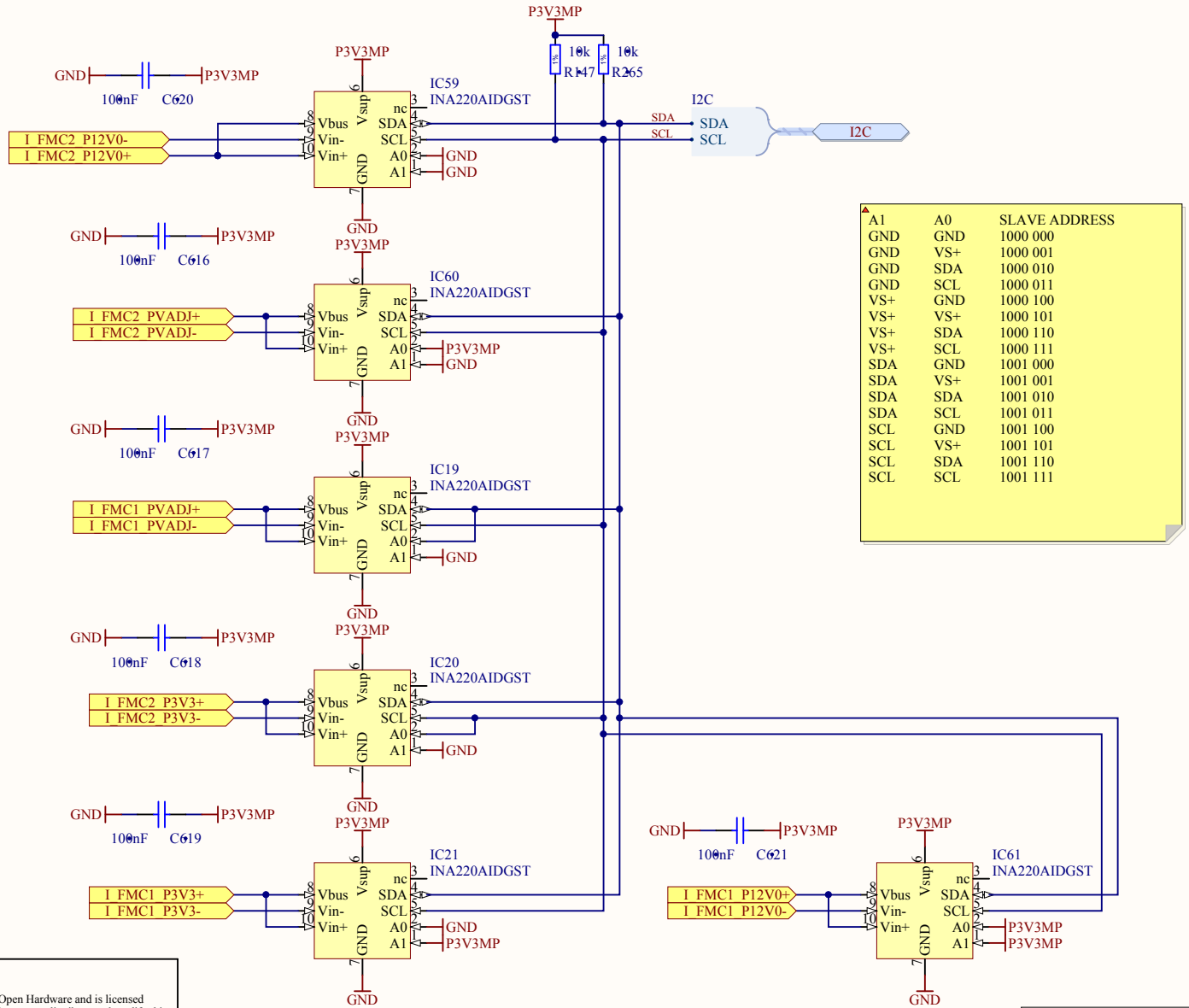
Number
Revision
Date:
2015-04-14
Sheet of
File:
D:\Users\..\FMC_Clocks.SchDoc
Drawn By:



A1	A0	SLAVE ADDRESS
GND	GND	1000 000
GND	VS+	1000 001
GND	SDA	1000 010
GND	SCL	1000 011
VS+	GND	1000 100
VS+	VS+	1000 101
VS+	SDA	1000 110
VS+	SCL	1000 111
SDA	GND	1001 000
SDA	VS+	1001 001
SDA	SDA	1001 010
SDA	SCL	1001 011
SCL	GND	1001 100
SCL	VS+	1001 101
SCL	SDA	1001 110
SCL	SCL	1001 111

Title		
Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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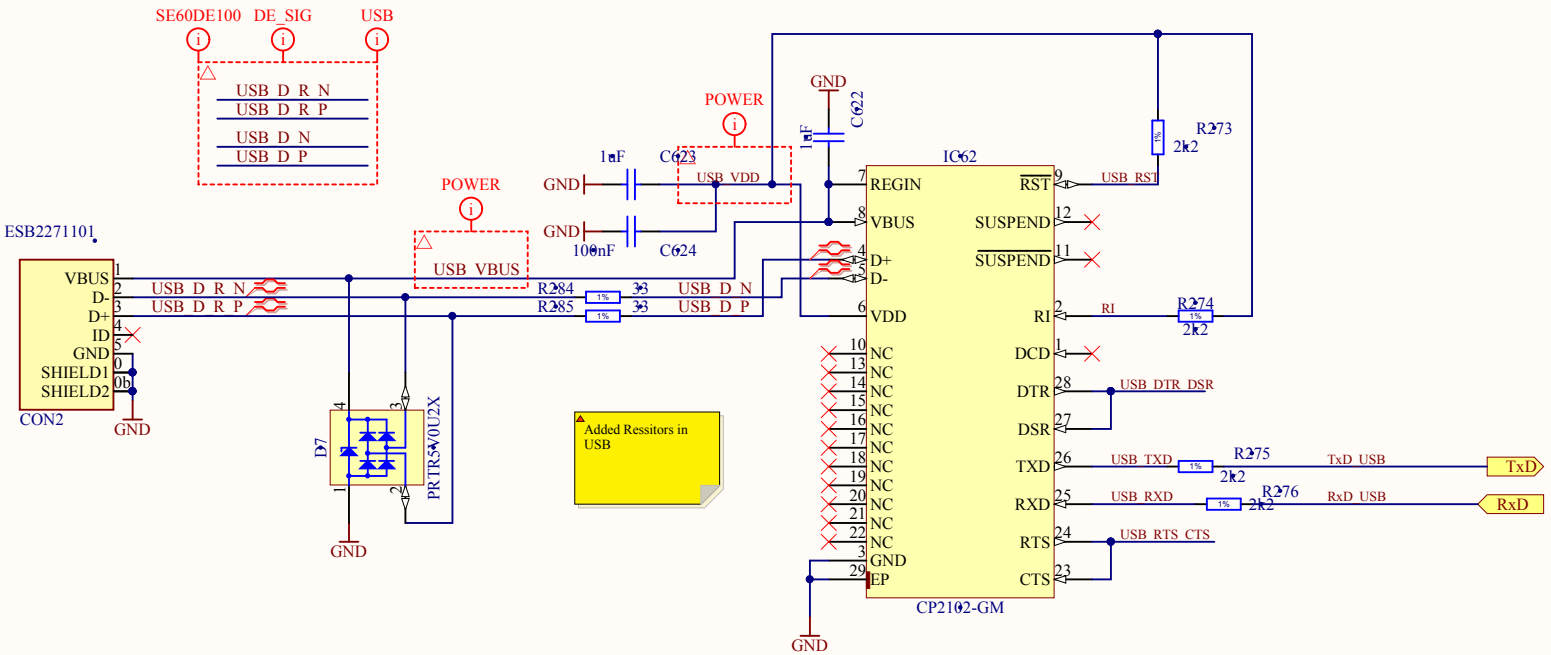

Title		
Size A4	Number	Revision
Date: 2015-04-14		Sheet of
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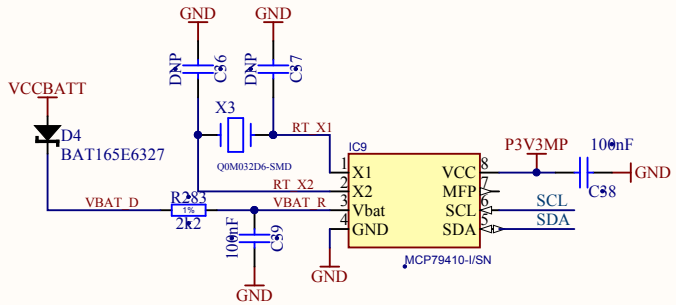
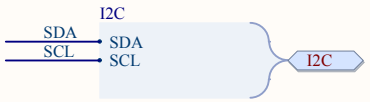
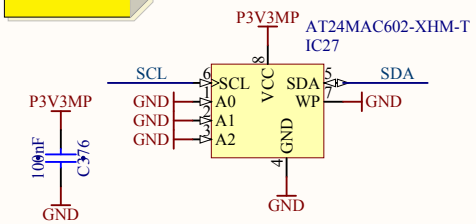




Added Ressitor and schotky to Vbat



Title		
Size: A4	Number	Revision
Date: 2015-04-14		Sheet of
File: D:\Users\..\RTCE.SchDoc		Drawn By:

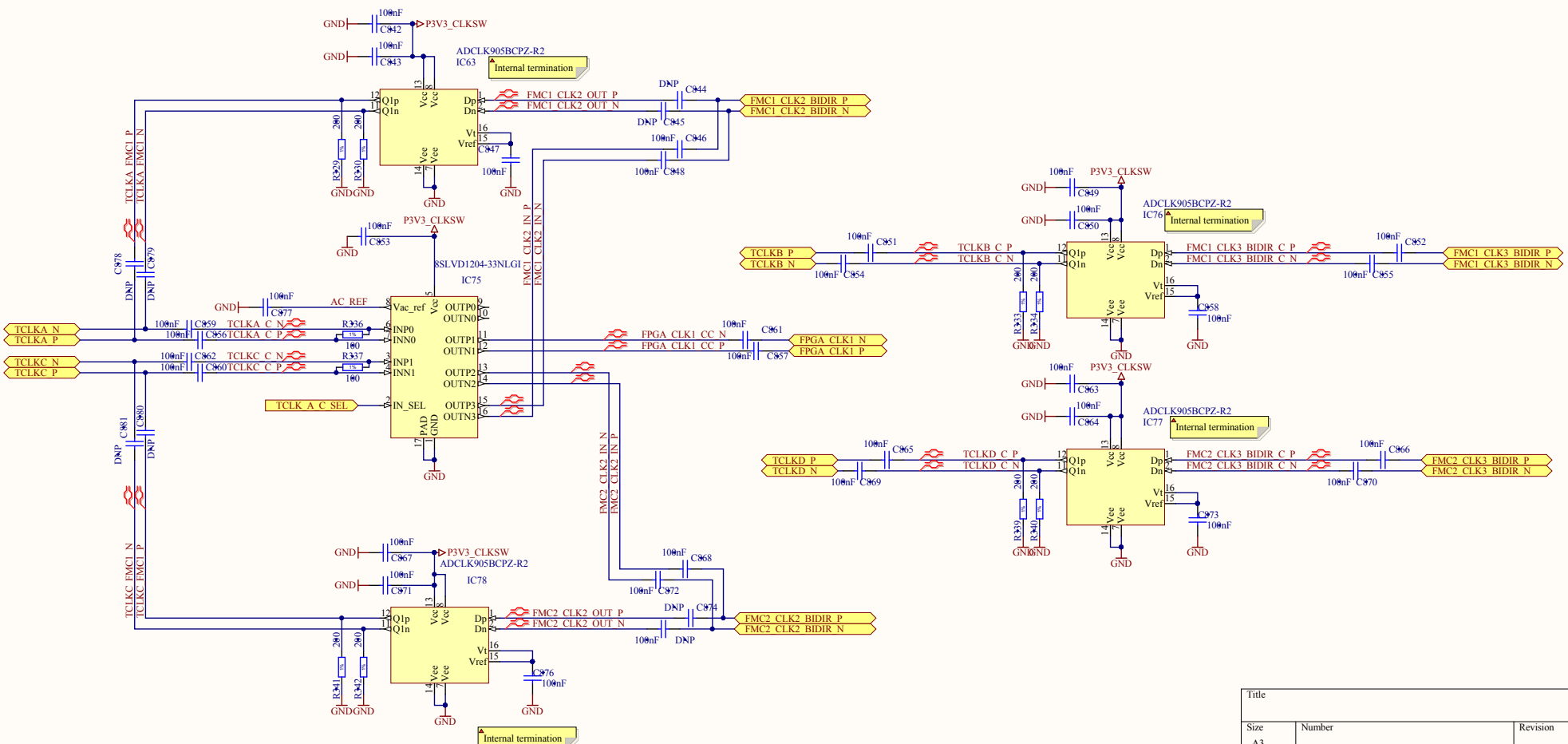
SE60DE100

TCLKB_C_P
TCLKB_C_N
TCLKD_C_P
TCLKD_C_N
TCLKA_C_P
TCLKA_C_N
TCLKC_C_P
TCLKC_C_N
TCLKC_FMC1_N
TCLKC_FMC1_P
TCLKA_FMC1_P
TCLKA_FMC1_N

FMC1_CLK3_BIDIR_C_P
FMC1_CLK3_BIDIR_C_N
FMC2_CLK3_BIDIR_C_P
FMC2_CLK3_BIDIR_C_N
FMC2_CLK2_IN_N
FMC2_CLK2_IN_P
FMC1_CLK2_IN_P
FMC1_CLK2_IN_N

FMC1_CLK2_OUT_P
FMC1_CLK2_OUT_N
FMC2_CLK2_OUT_P
FMC2_CLK2_OUT_N

File format (.png) not supported



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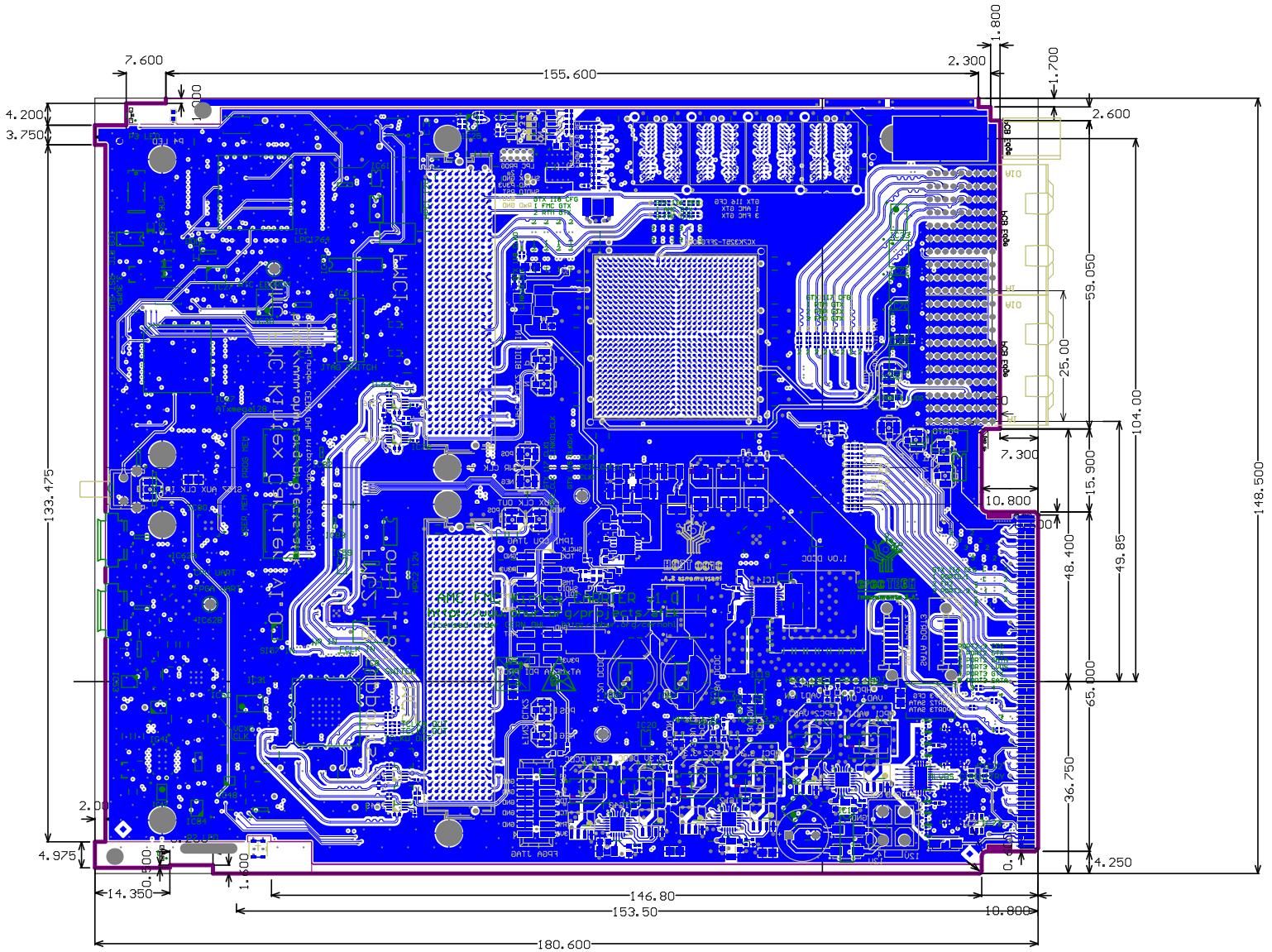

TOP = COMPONENT SIDE 2

BTM = COMPONENT SIDE 1