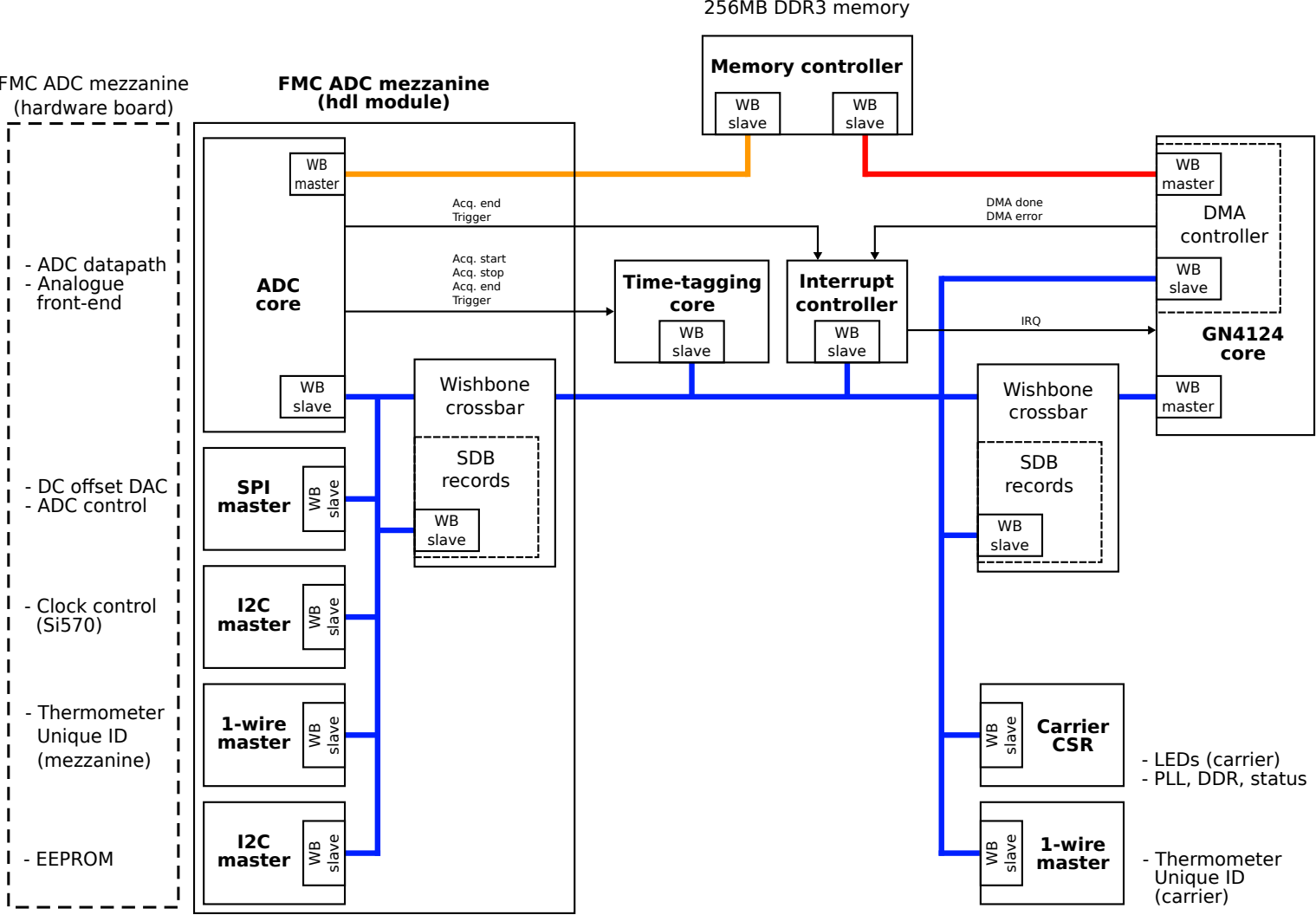
256MB DDR3 memory
Memory controller
WB slave
WB slave
FMC ADC mezzanine (hardware board)
FMC ADC mezzanine (hdl module)
- ADC datapath
- Analogue front-end
- DC offset DAC
- ADC control
- Clock control (Si570)
- Thermometer Unique ID (mezzanine)
- EEPROM
WB master
ADC core
WB slave
Acq. end
Trigger
Acq. start
Acq. stop
Acq. end
Trigger
Time-tagging core
WB slave
Interrupt controller
WB slave
DMA done
DMA error
IRQ
WB master
DMA controller
WB slave
GN4124 core
WB master
Wishbone crossbar
SDB records
WB slave
SPI master
WB slave
I2C master
WB slave
1-wire master
WB slave
I2C master
WB slave
Wishbone crossbar
SDB records
WB slave
Carrier CSR
WB slave
- LEDs (carrier)
- PLL, DDR, status
1-wire master
WB slave
- Thermometer Unique ID (carrier)