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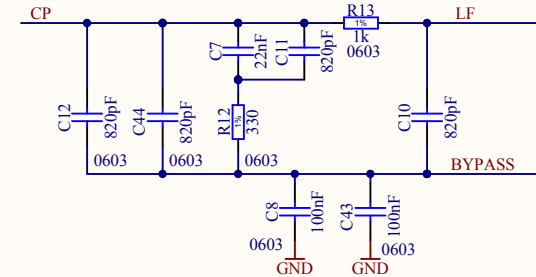
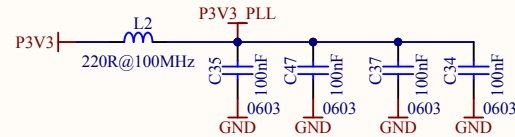
Default mode:  
TDC in I-Mode, 40MHz per channel. TDC driven by 125MHz/4 clock.  
START: 125/4 clock  
STOP: trigger inputs

Calibration mode:  
TBD

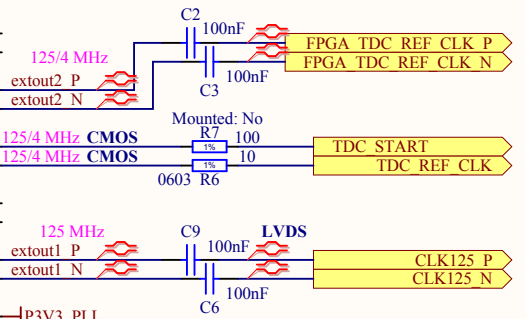
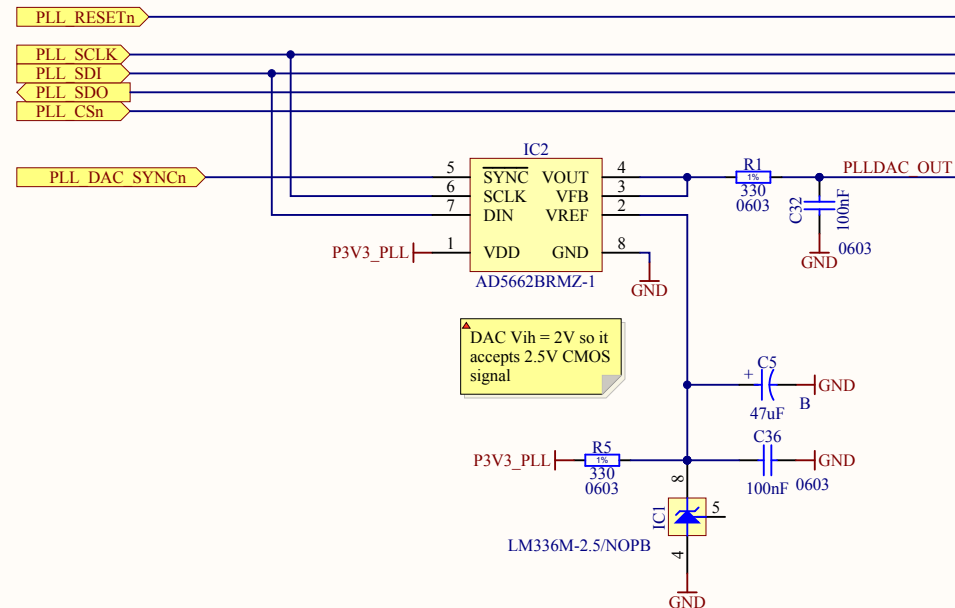
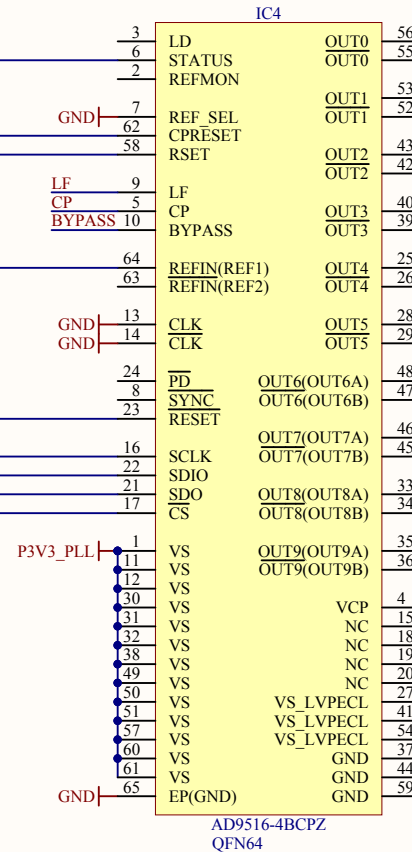
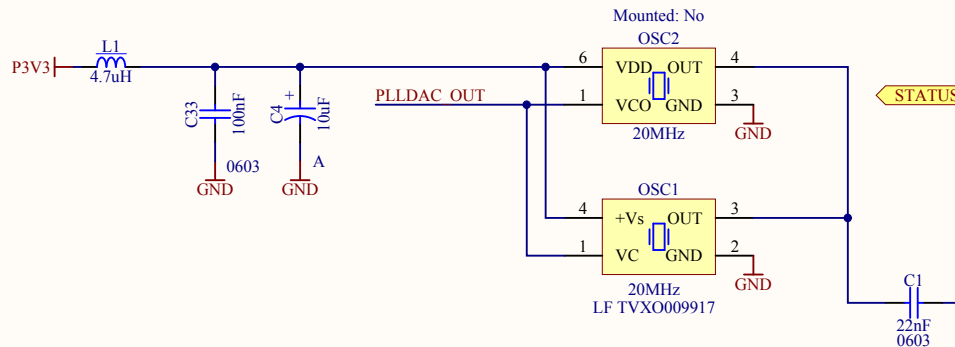
Project/Equipment		Fmc Tdc 1ns Scha	
Document		Designer: Nicolas Voumard	
		Drawn by: Nicolas Voumard	
		Check by: C.Andouillet	
		Last Mod: C.Andouillet	
		File: FMC TDC 1ns 5Cha SchDoe	
		Print Date: 26-04-2013 08:08:15	
		Sheet: 1 of 6	
		A3	



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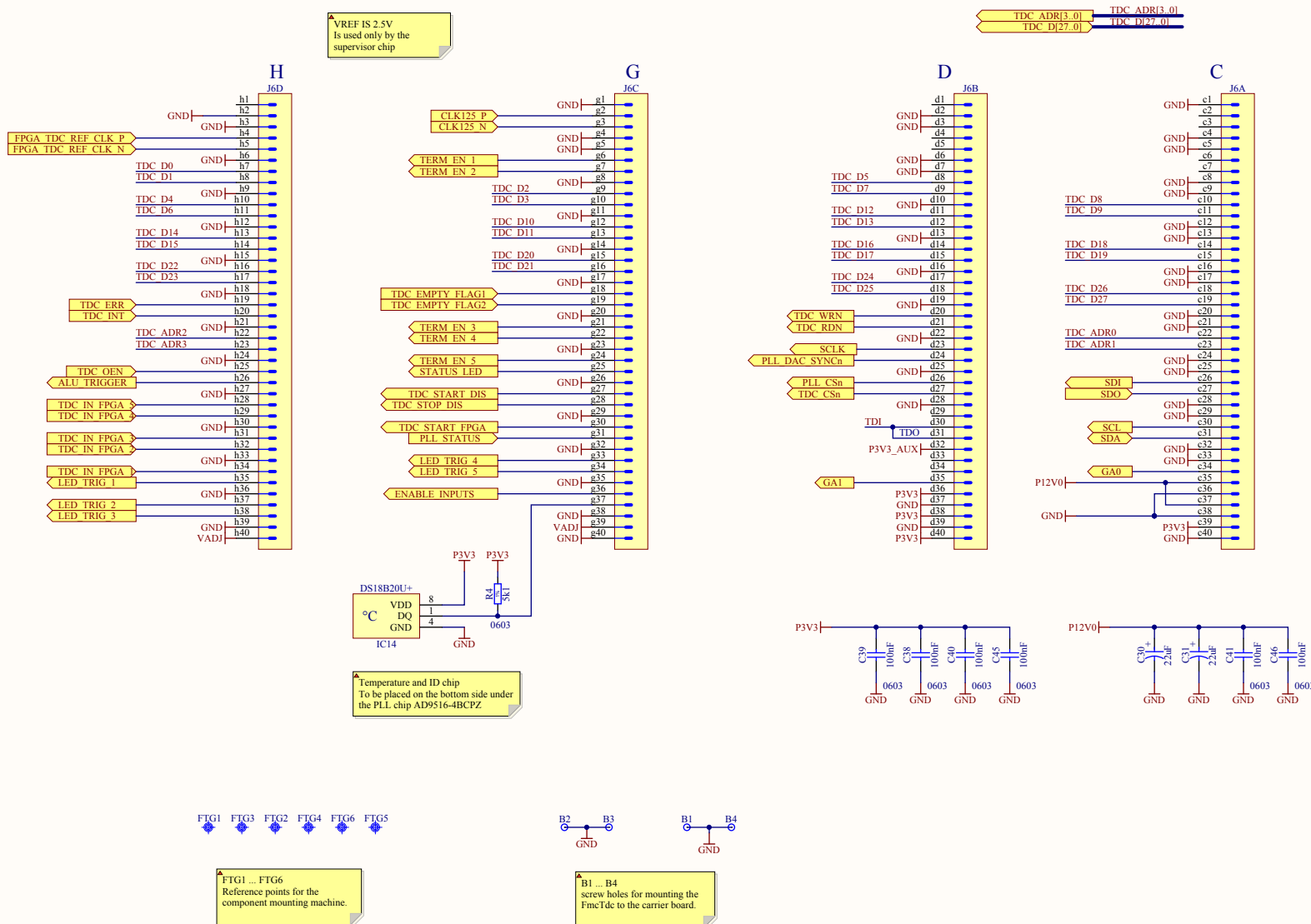
Loop filter components calculated using ADIsimCLK software.  
Loop BW=46.3kHz,  
Phase margin = 42.5deg  
Fvco=1.5GHz



Project/Equipment		Fmc Tdc Ins Scha	
Document		Designer	Nicolas Voumard
 		Drawn by	Nicolas Voumard
		Check by	C.Andouillet
		Last Mod.	C.Andouillet
		File	clock_generator.SchDoc
		Print Date	26-04-2013 08:08:16
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Sheet	2 of 6
EDA-02290-V3-1		Size	A4
		Rev	-

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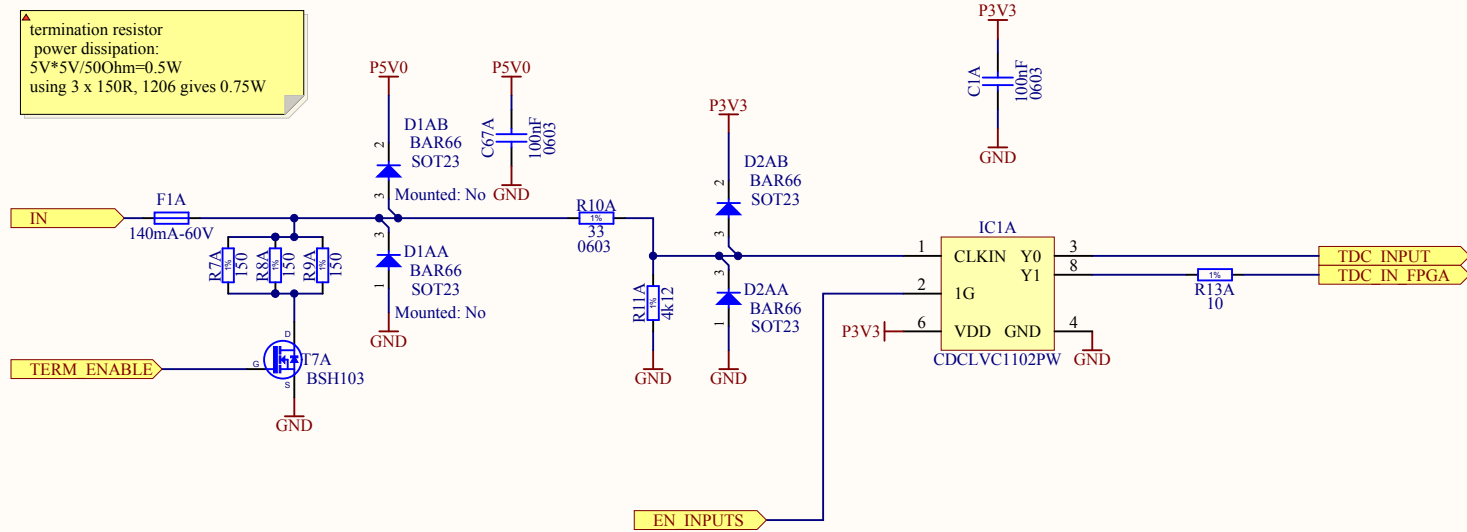
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Project/Equipment		Fmc Tdc Ins Scha	
Document		Designer: Nicolas Voumard	10-07-2010
		Drawn by: Nicolas Voumard	
		Check by: C.Andouillet	26-04-2013
		Last Mod: C.Andouillet	
		File: FMC connector SchDoc	
		Print Date: 26-04-2013 08:08:16	Sheet 3 of 6
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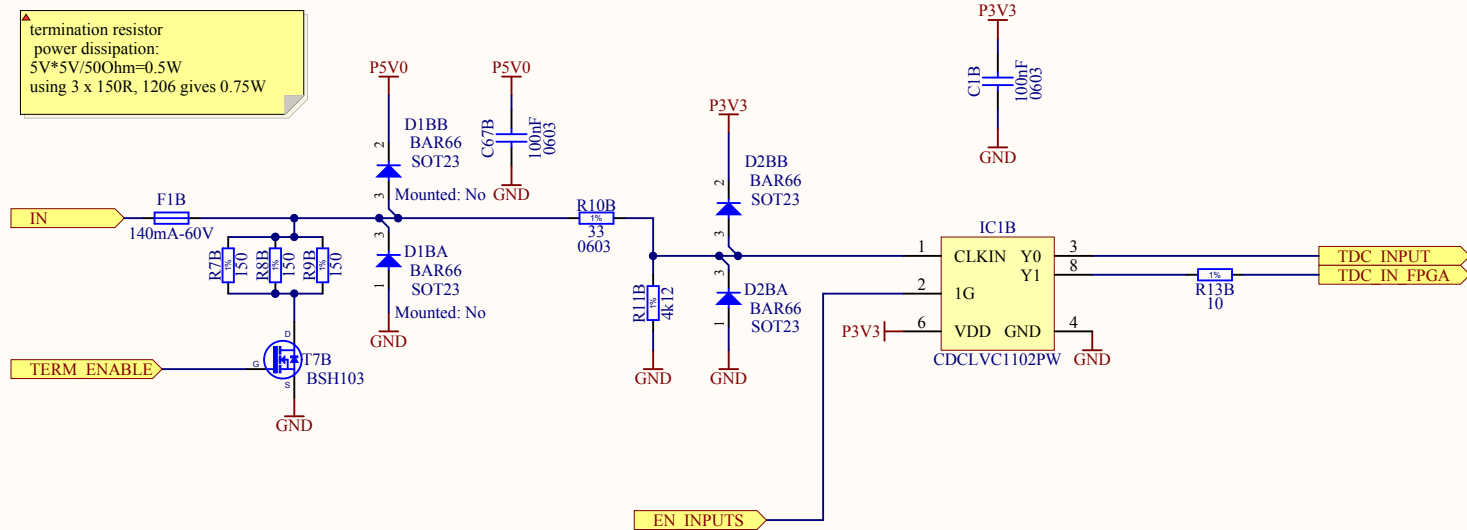
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Document		Designer Nicolas Voumard	
		Drawn by Nicolas Voumard	10-07-2010
		Check by C.Andouillet	
		Last Mod. C.Andouillet	25-04-2013
		File INPUT LOGIC.SchDoc	
		Print Date 26-04-2013 08:08:17	Sheet 4 of 6
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		Size A4	Rev -

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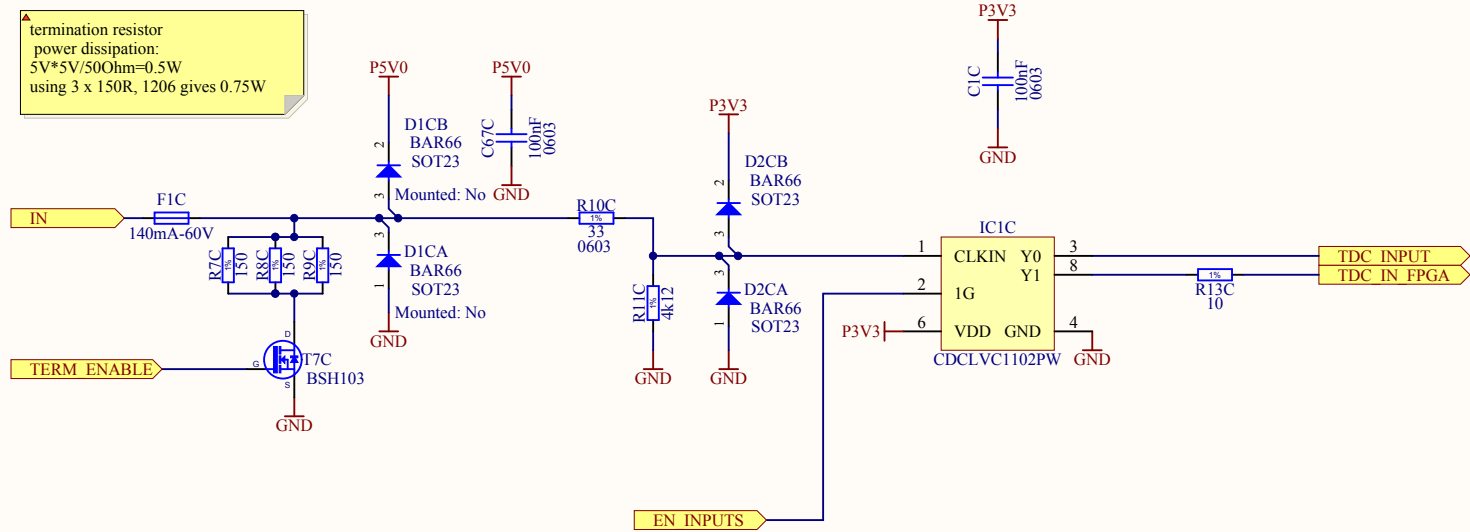
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		Drawn by Nicolas Voumard	10-07-2010
		Check by C.Andouillet	
		Last Mod. C.Andouillet	25-04-2013
		File INPUT LOGIC.SchDoc	
		Print Date 26-04-2013 08:08:17	Sheet 4 of 6
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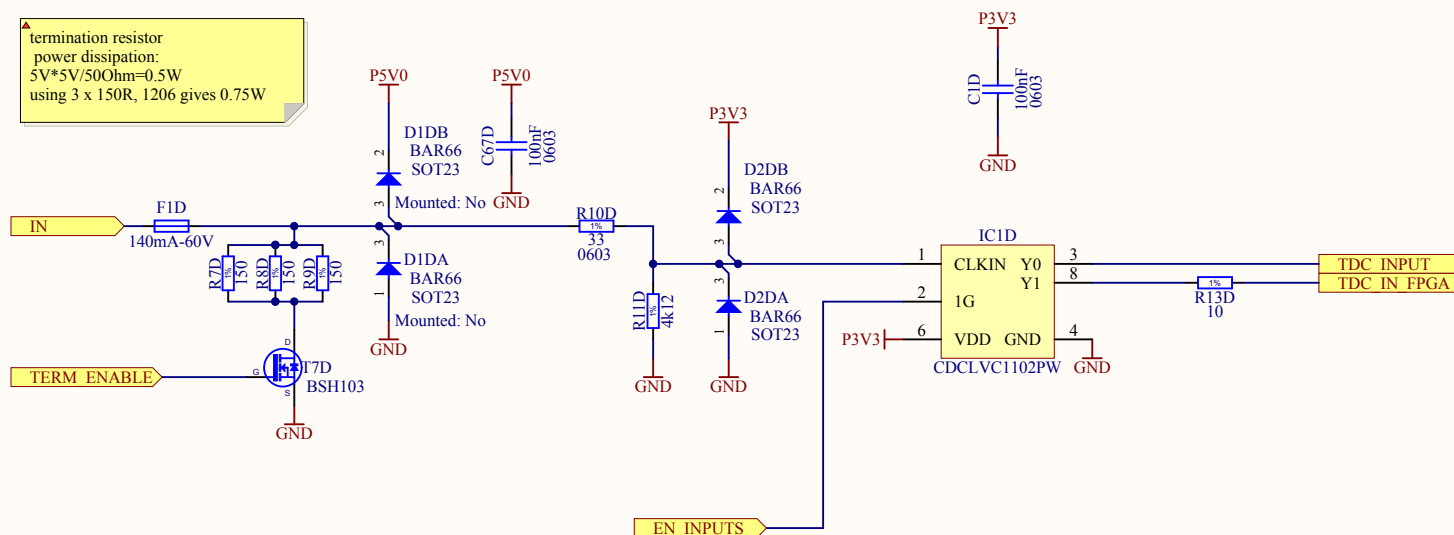
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Document		Designer Nicolas Voumard	
		Drawn by Nicolas Voumard	10-07-2010
		Check by C.Andouillet	
		Last Mod. C.Andouillet	25-04-2013
		File INPUT LOGIC.SchDoc	
		Print Date 26-04-2013 08:08:18	Sheet 4 of 6
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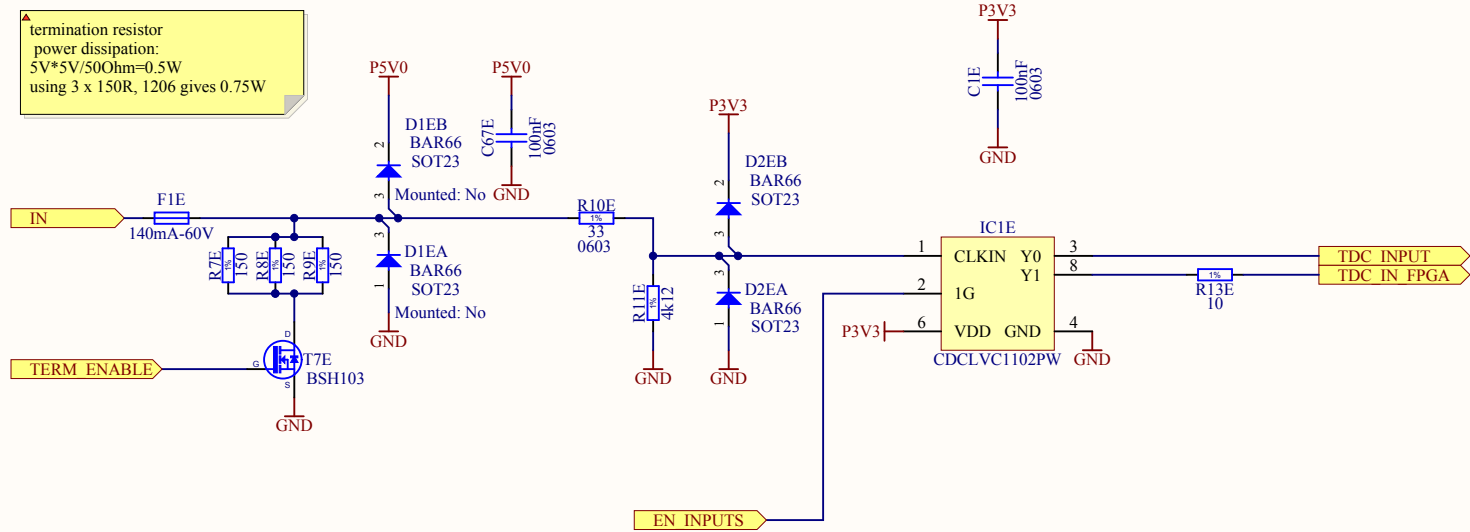
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Project/Equipment		Fmc Tdc Ins Scha			
<div>Document</div> <div>BE-CO</div> <div></div>	<div>Input logic</div>		Designer	Nicolas Voumard	
			Drawn by	Nicolas Voumard	10-07-2010
			Check by	C.Andouillet	
			Last Mod.	C.Andouillet	25-04-2013
			File	INPUT_LOGIC.SchDoc	
			Print Date	26-04-2013 08:08:18	Sheet
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Document		<b>Input logic</b>	
	Designer	Nicolas Voumard	
	Drawn by	Nicolas Voumard	10-07-2010
	Check by	C.Andouillet	
	Last Mod.	C.Andouillet	25-04-2013
	File	INPUT LOGIC.SchDoc	
Print Date		26-04-2013 08:08:19	Sheet 4 of 6
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland		EDA-02290-V3-1	
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		A4	-



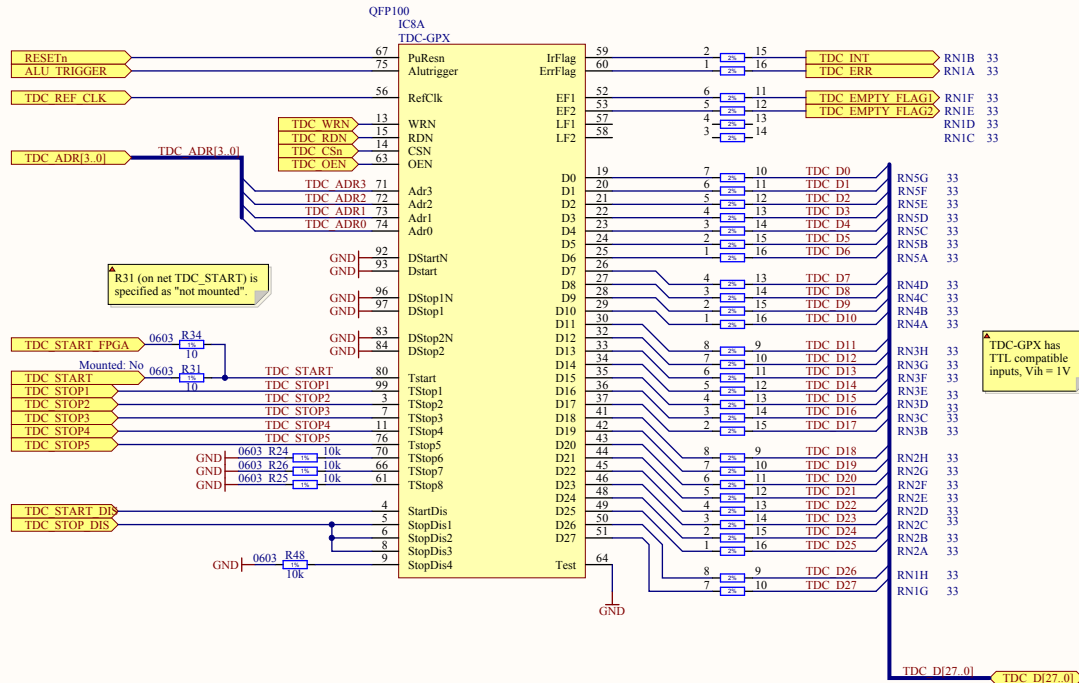
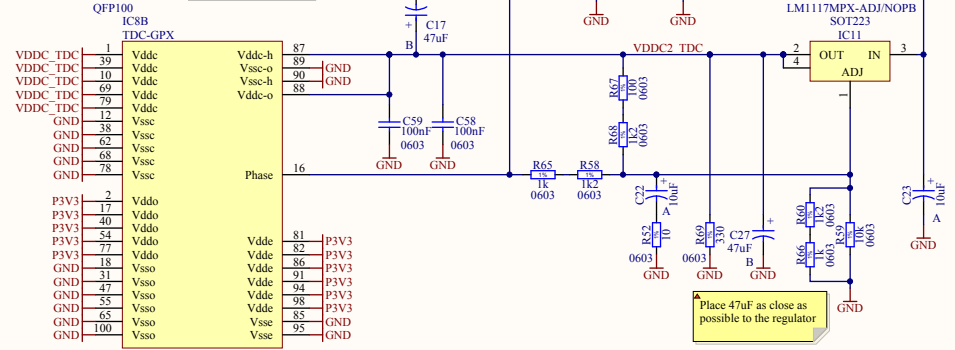
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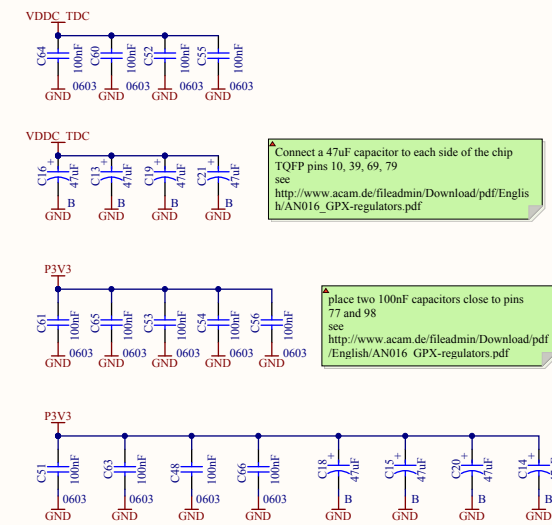
IC11 and IC12 are part of temperature compensation loop for TDC

V<sub>ddc-h</sub>, V<sub>ssc-o</sub> absolute maximum is 3.6V, nominal: 3.3V

V<sub>ddc</sub> should be close to 3.3V, absolute maximum is 3.6V



TDC-GPX has TTL compatible inputs, V<sub>ih</sub> = 1V



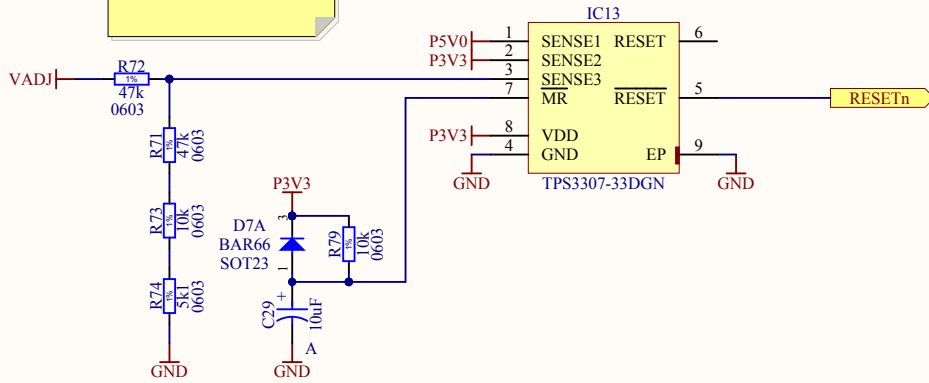
Connect a 47uF capacitor to each side of the chip TQFP pins 10, 39, 69, 79 see [http://www.acam.de/fileadmin/Download/pdf/English/AN016\\_GPX-regulators.pdf](http://www.acam.de/fileadmin/Download/pdf/English/AN016_GPX-regulators.pdf)

place two 100nF capacitors close to pins 77 and 98 see [http://www.acam.de/fileadmin/Download/pdf/English/AN016\\_GPX-regulators.pdf](http://www.acam.de/fileadmin/Download/pdf/English/AN016_GPX-regulators.pdf)

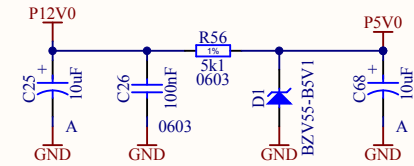
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▲ TPS3307-33D thresholds  
sense1 sense2 sense3  
4.55V 2.93V 1.25V



▲ +5V power supply only  
for input protection  
diodes biasing.



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CH-1211 Geneva 23 - Switzerland		File power_supply.SchDoc	
		Print Date 26-04-2013 08:08:20	
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**Power supplies**

EDA-02290-V3-1