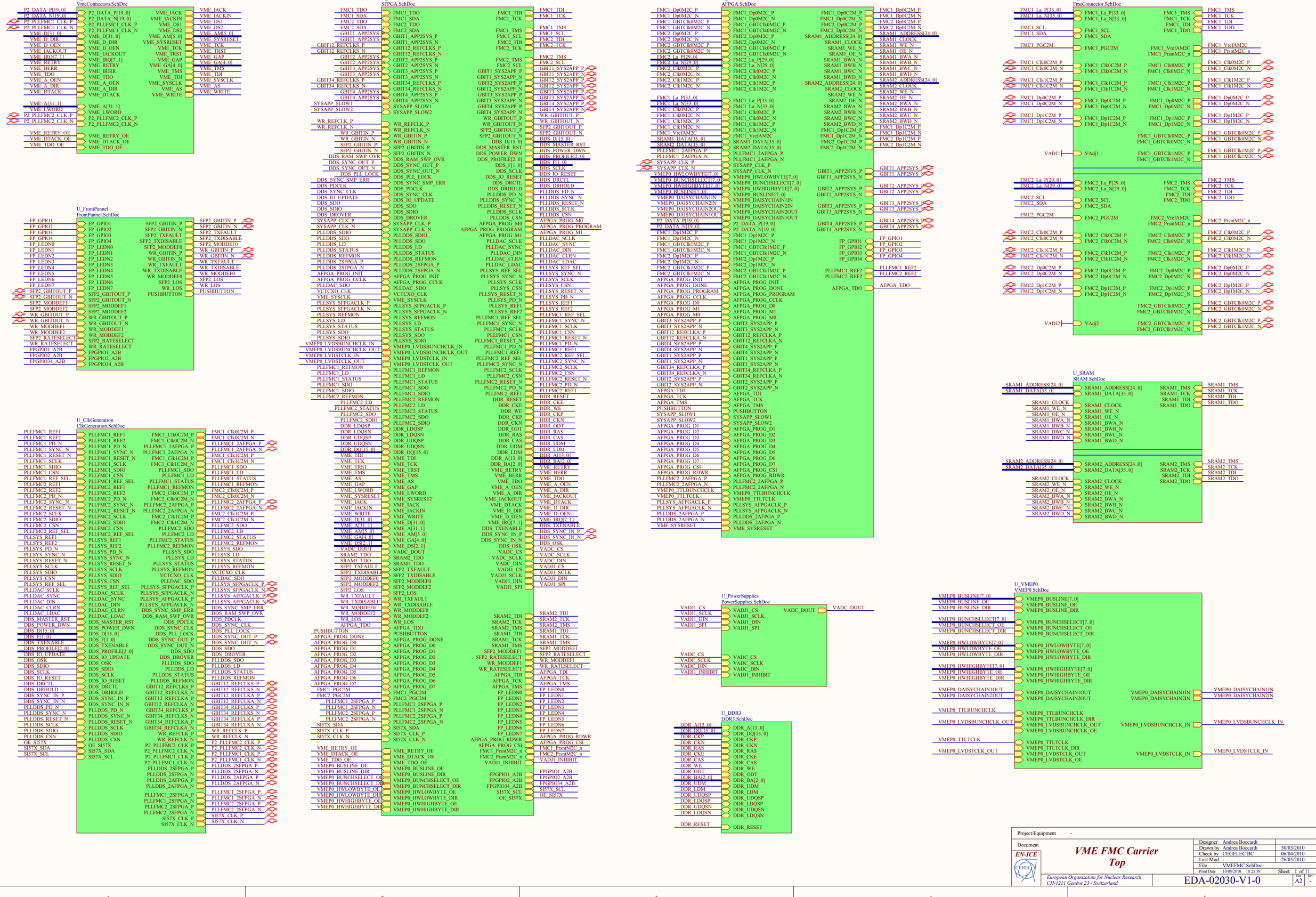


Project/Equipment	-
Document	

EN-ICE

VME FMC Carrier Top

Designer	Andrea Boccardi	
Drawn by	Andrea Boccardi	30/03/2010
Check by	CEGELEC BC	06/04/2010
Last Mod.	-	26/05/2010
File	VMEFMC.SchDoc	
Print Date	10/08/2010 18:25:39	Sheet 1 of 11

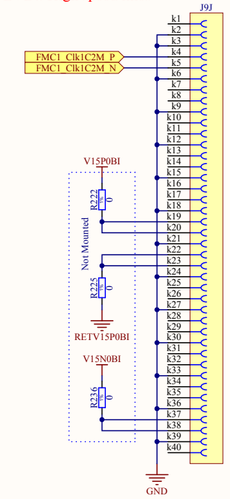
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02030-V1-0

Size A2 | Rev -

High Pin Count Rows

LVDS High speed lines



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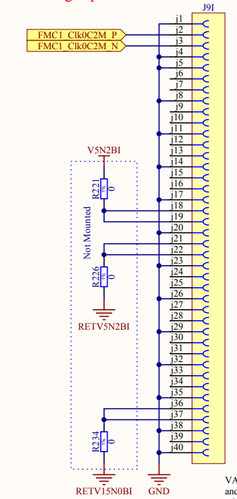
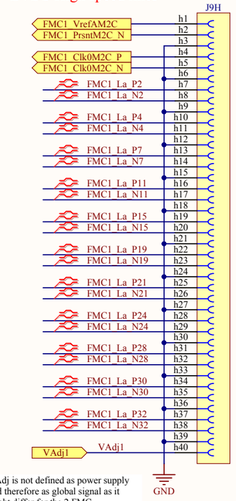


Low Pin Count Rows

LVDS High speed lines



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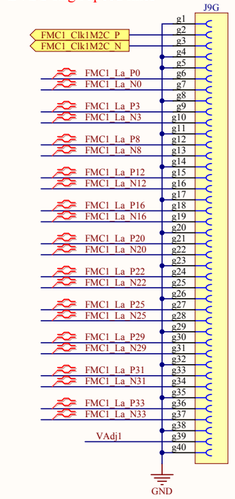
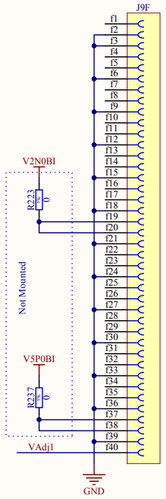
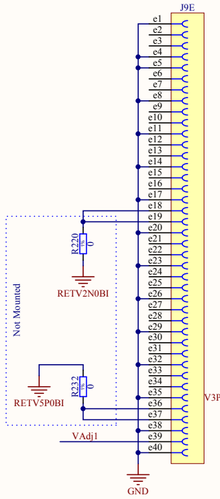


VAdj is not defined as power supply and therefore as global signal as it might differ for the 2 FMC

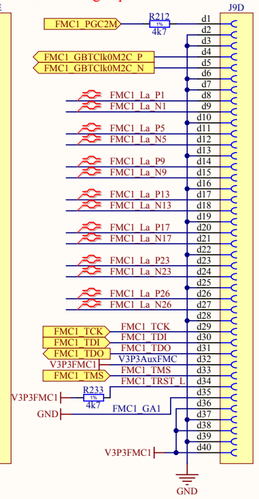
High Pin Count Rows





Low Pin Count Rows

LVDS High speed lines



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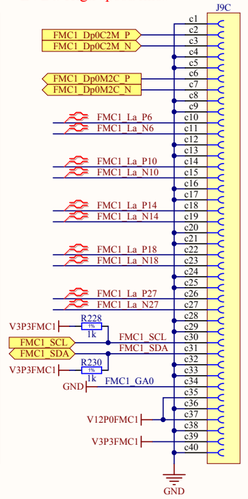

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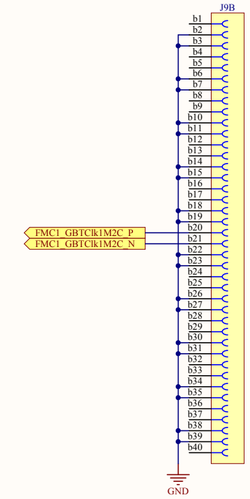
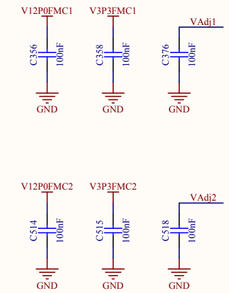




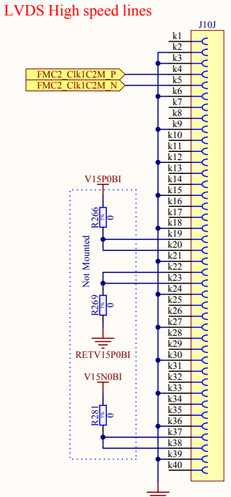
LaP and LaN are LVDS lines

NB: the LVDS pairs must have a differential impedence of 100 ohm and be routed with no skew between the P and the N lines.
The skew between the various La pairs should be kept as low as possible.

LaP and LaN are LVDS lines

High Pin Count Rows

LVDS High speed lines



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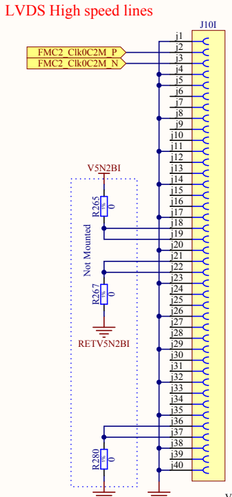

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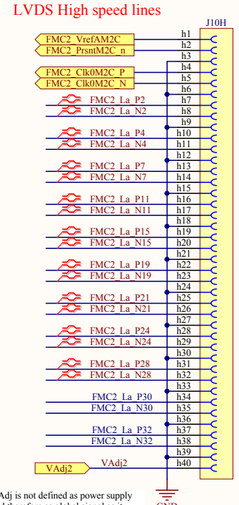

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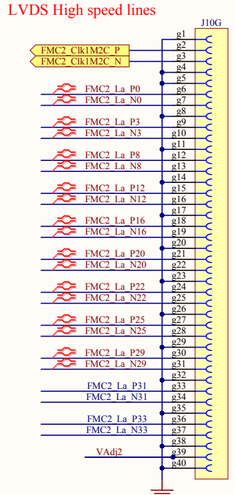
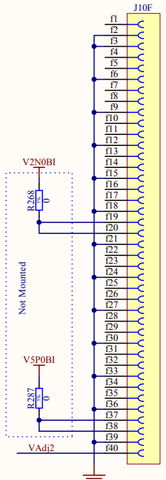
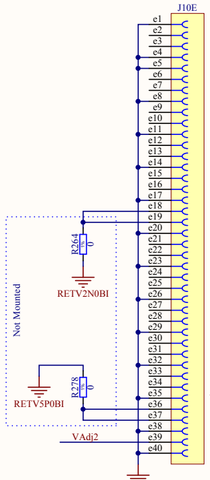


VAdj is not defined as power supply and therefore as global signal as it might differ for the 2 FMC

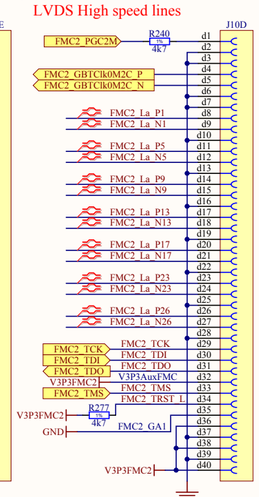
High Pin Count Rows





Low Pin Count Rows

LVDS High speed lines



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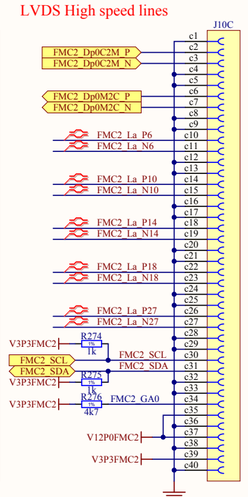

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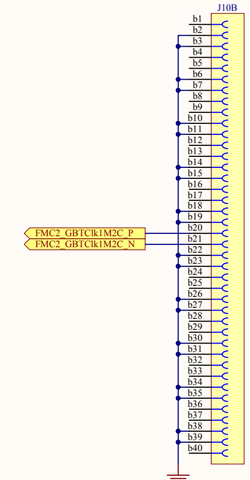

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		Drawn by Andrea Boccardi	30/03/2010
		Check.by CEGELEC BC	06/04/2010
		Last Mod. -	26/07/2010
		File FmcConnector.SchDoc	
		Print Date 10/08/2010 18:25:41	Sheet 2 of 11
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02030-V1-0	Size A2	Rev -

Project/Equipment -

Document

AB-BI

CERN

VME FMC Carrier
VME P1 & P2

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

Designer	Andrea Boccardi	
Drawn by	Andrea Boccardi	30/03/2010
Check by	CEGELEC BC	06/04/2010
Last Mod.		23/07/2010
File	VmeConnectors.SchDoc	
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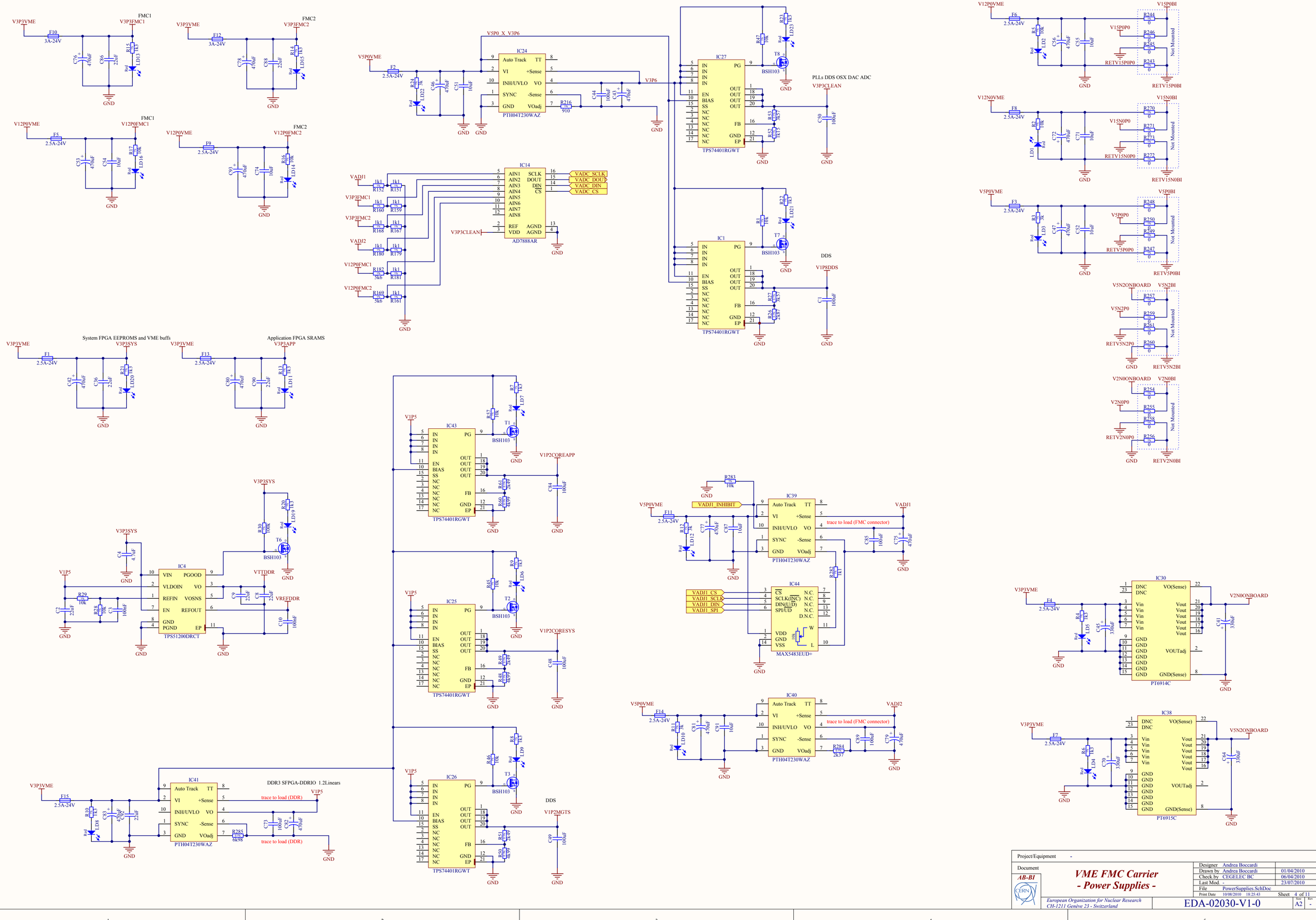
EDA-02030-V1-0

Size A2 | Rev -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V3P3FMC1
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FMC2
V3P3VME
V3P3FMC2
F12
3A-24V
C78 470uF
C88 22uF
R14 1K3
LD15 Red
GND
FMC1
V12P0VME
V12P0FMC1
F5
2.5A-24V
C53 470uF
C54 10uF
R17 10k
LD16 Red
GND
FMC2
V12P0VME
V12P0FMC2
F9
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C93 470uF
C74 10uF
R16 10k
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GND
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V3P3SYS
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C36 22uF
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LD20 Red
GND
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C90 22uF
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R30 10K
T6
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C2 22uF
R28 10k
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VLDOIN VO
REFIN VOSNS
EN REFOUT
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PGND EP
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GND
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INH/UVLO VO
SYNC -Sense
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- Power Supplies -
Designer Andrea Boccardi
Drawn by Andrea Boccardi 01/04/2010
Check.by CEGELEC BC 06/04/2010
Last Mod. - 23/07/2010
File PowerSupplies.SchDoc
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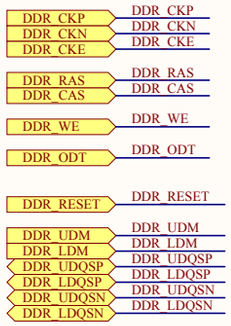
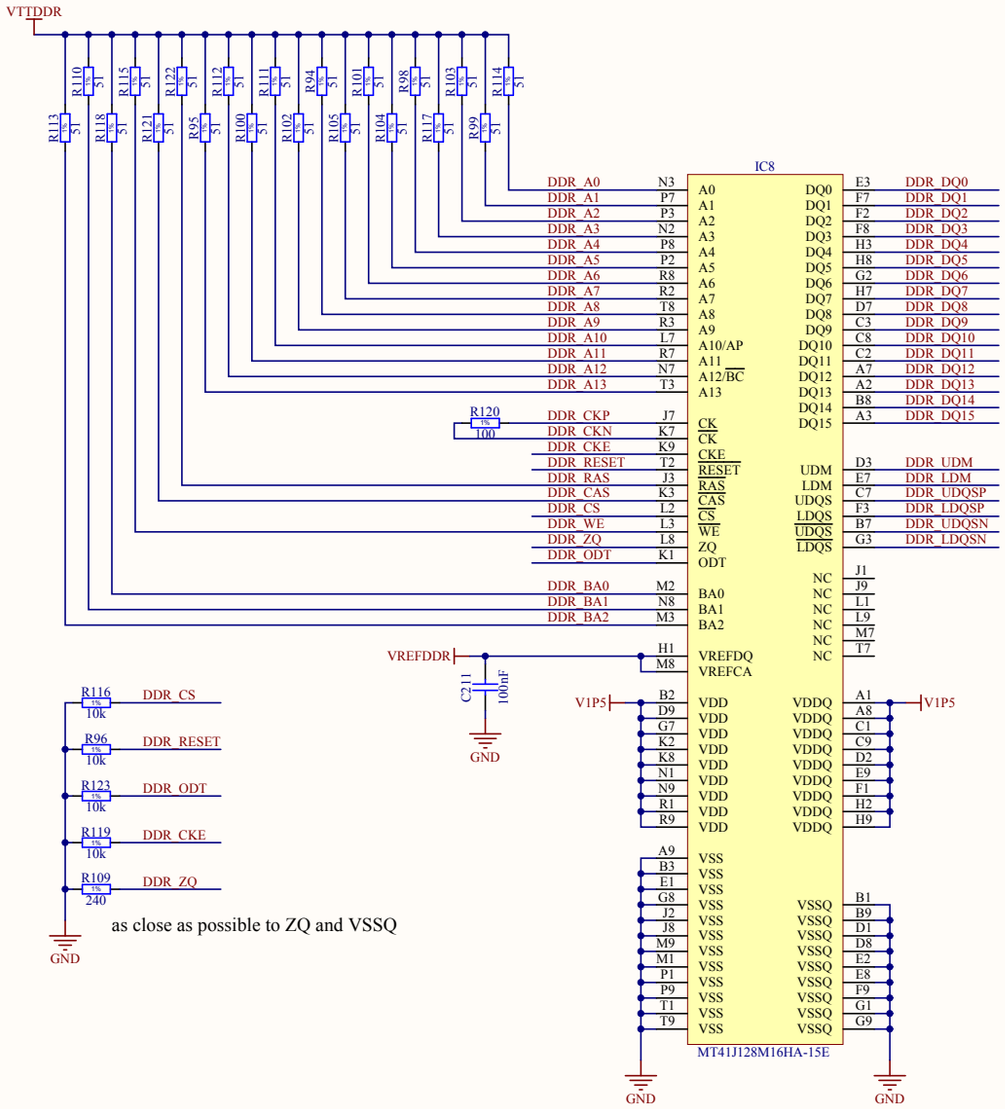
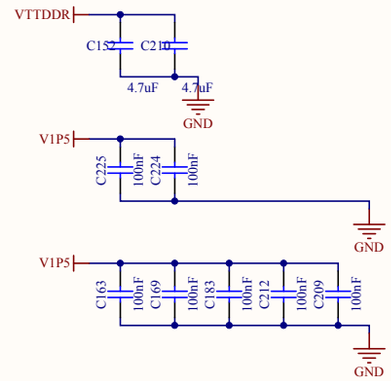
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
EDA-02030-V1-0
Size A2
Rev -







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		Check.by CEGELEC BC	06/04/2010
		Last Mod. -	23/07/2010
		File DDR3.SchDoc	
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European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02030-V1-0	Size A3	Rev -

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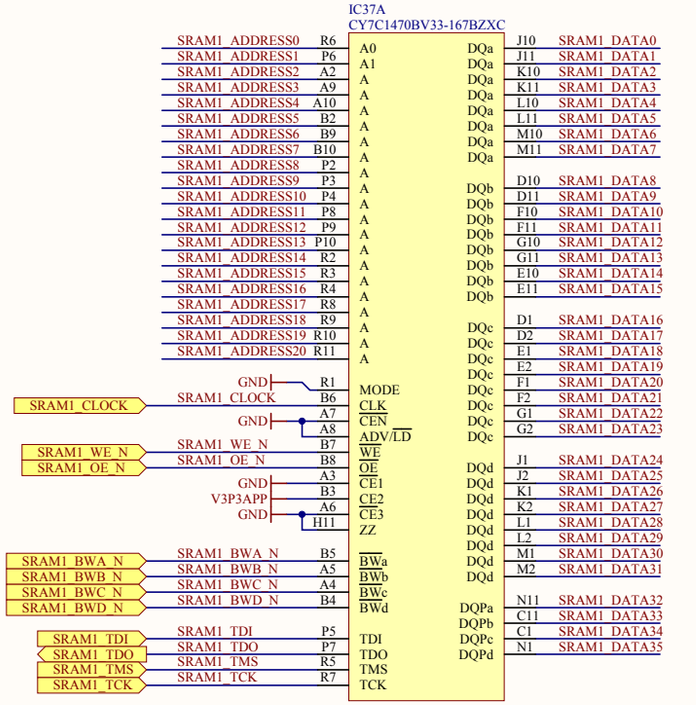

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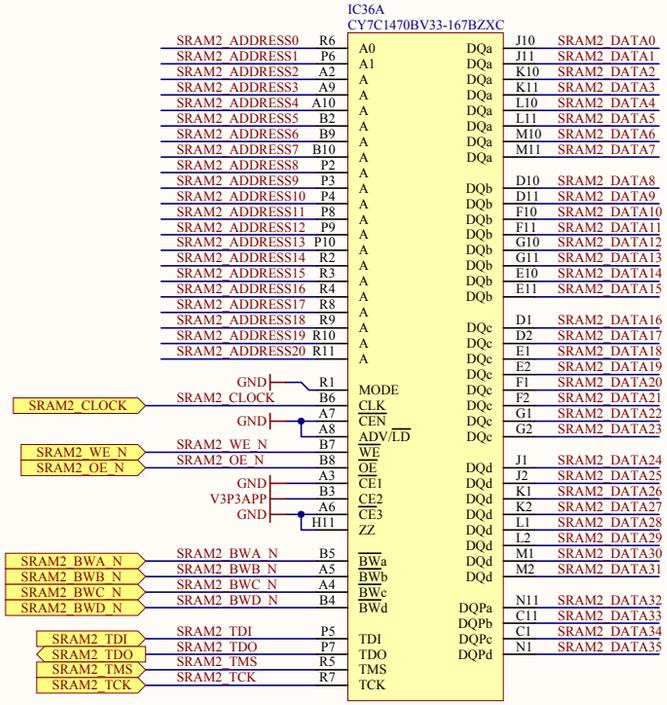
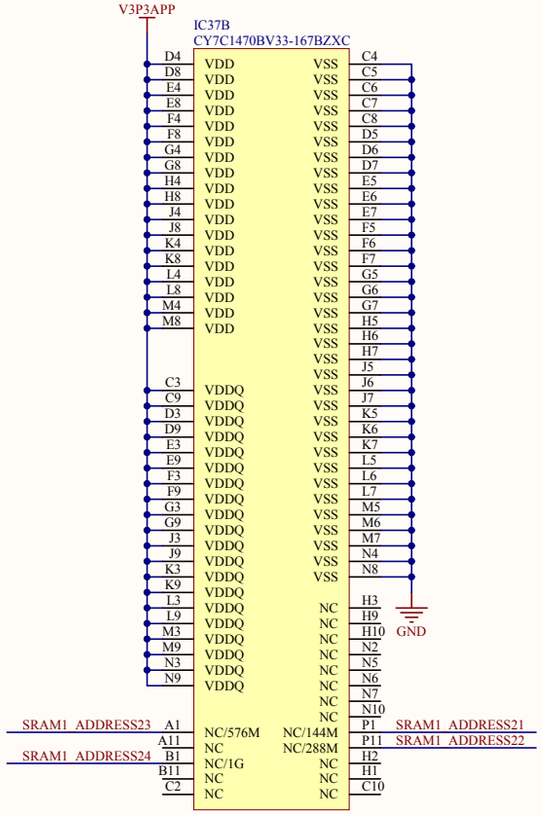
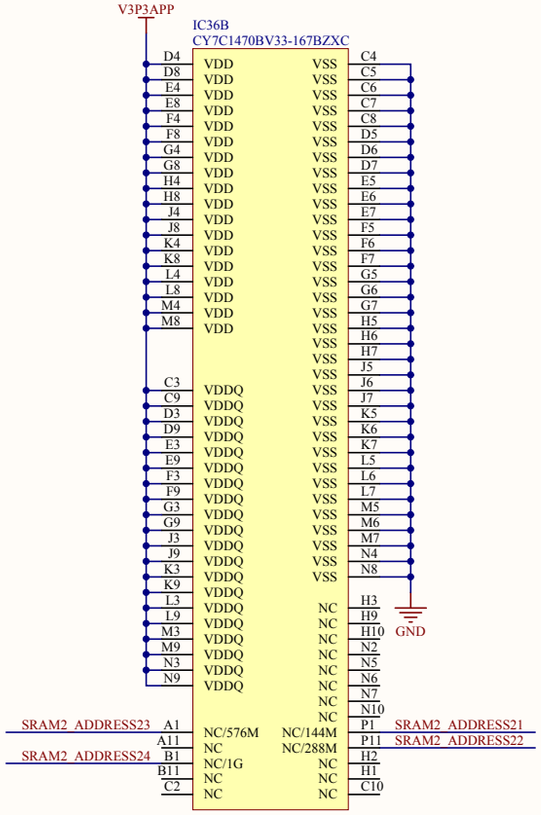
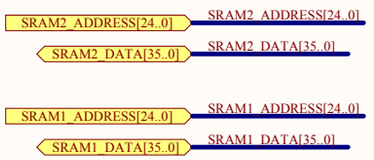
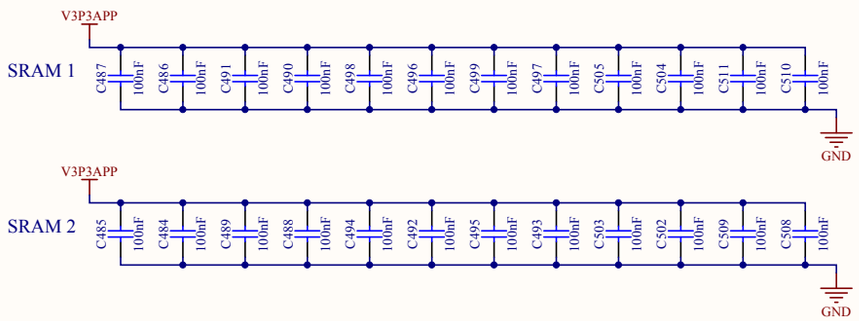


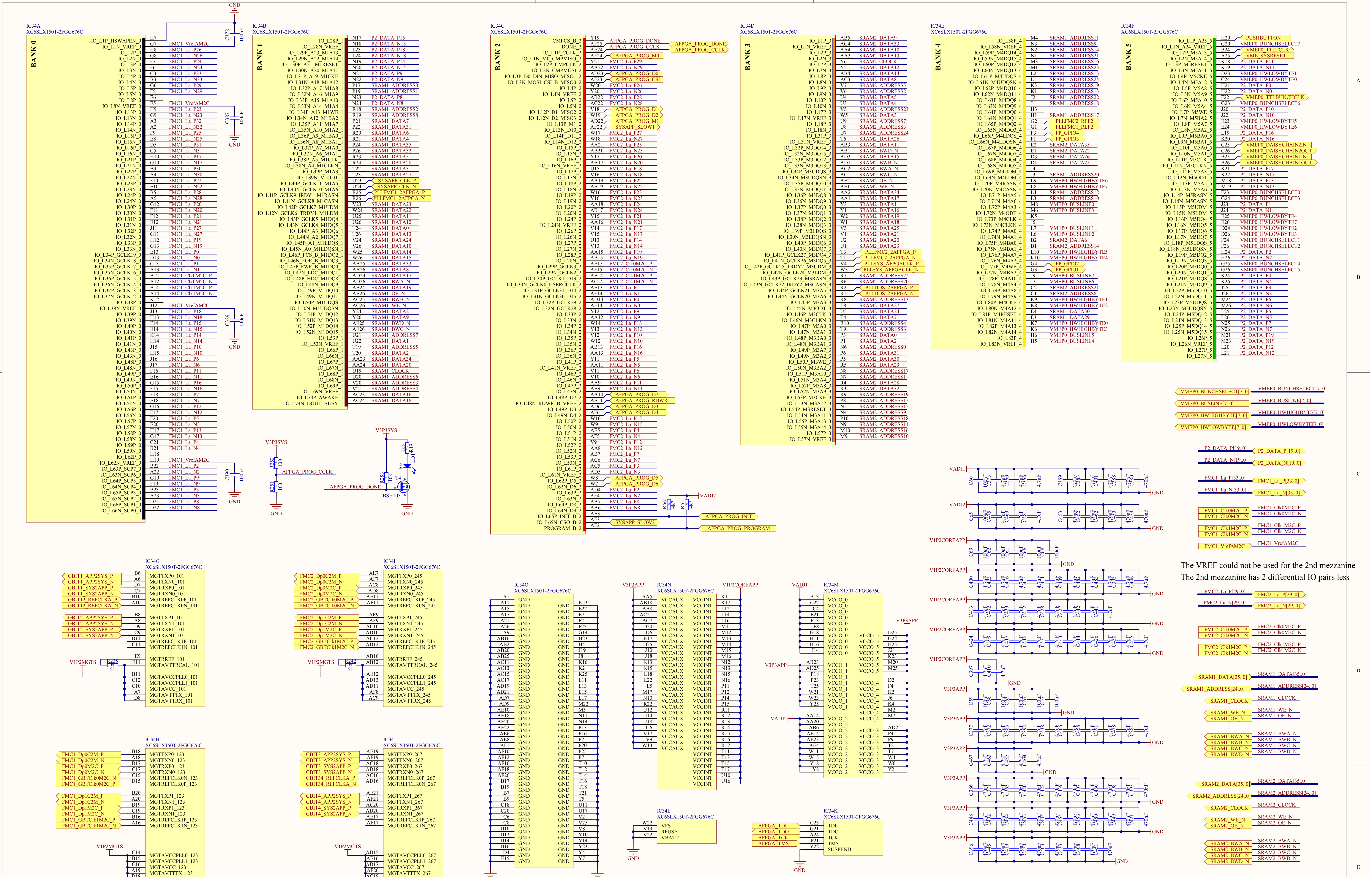








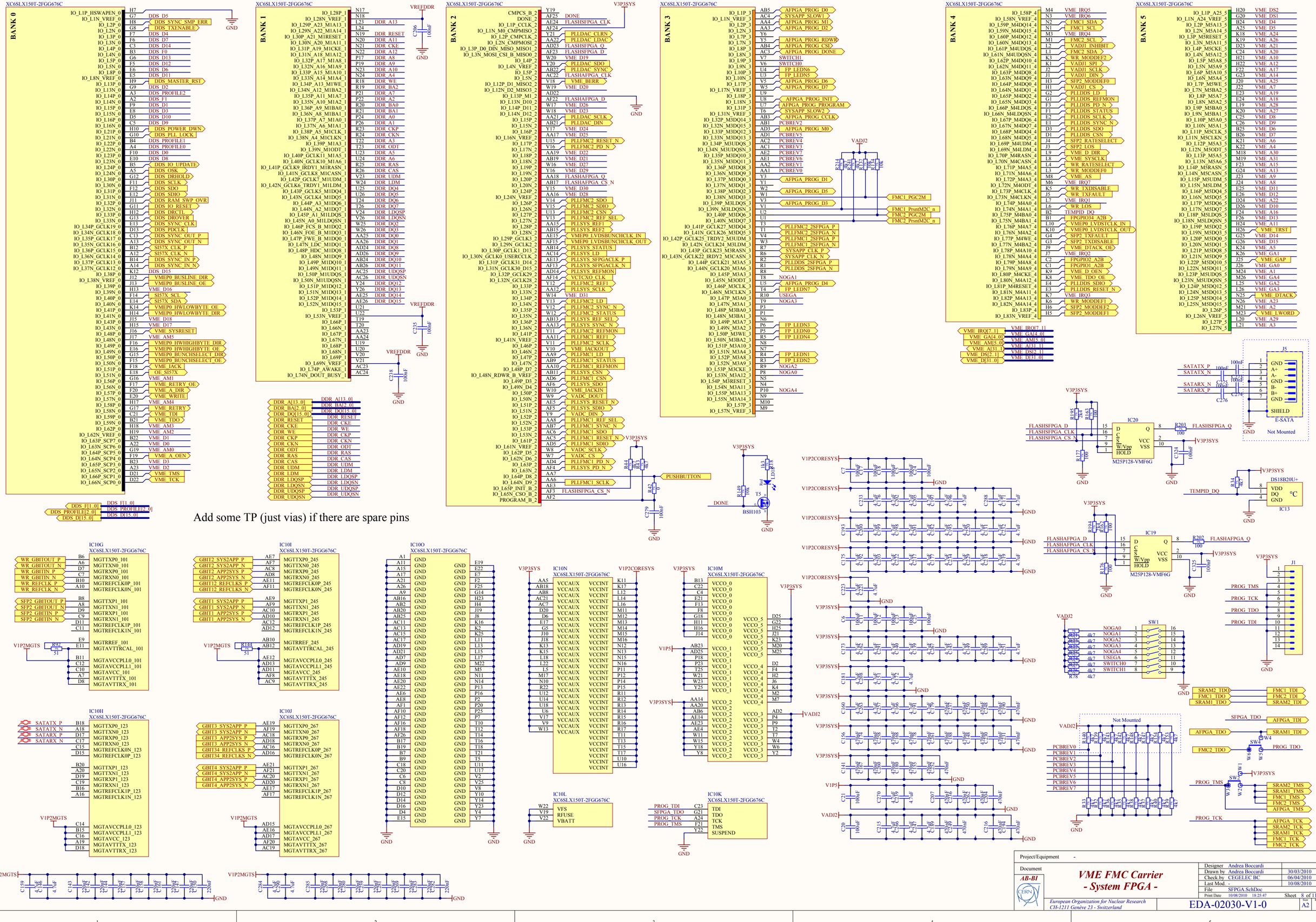
Project/Equipment	-		
Document	VME FMC Carrier - SRAM -	Designer	Andrea Boccardi
		Drawn by	Andrea Boccardi 30/03/2010
		Check.by	CEGELEC BC 06/04/2010
		Last Mod.	- 23/07/2010
		File	SRAM.SchDoc
		Print Date	10/08/2010 18:25:44 Sheet 6 of 11
EN-ICE	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	EDA-02030-V1-0	Size A3 Rev -

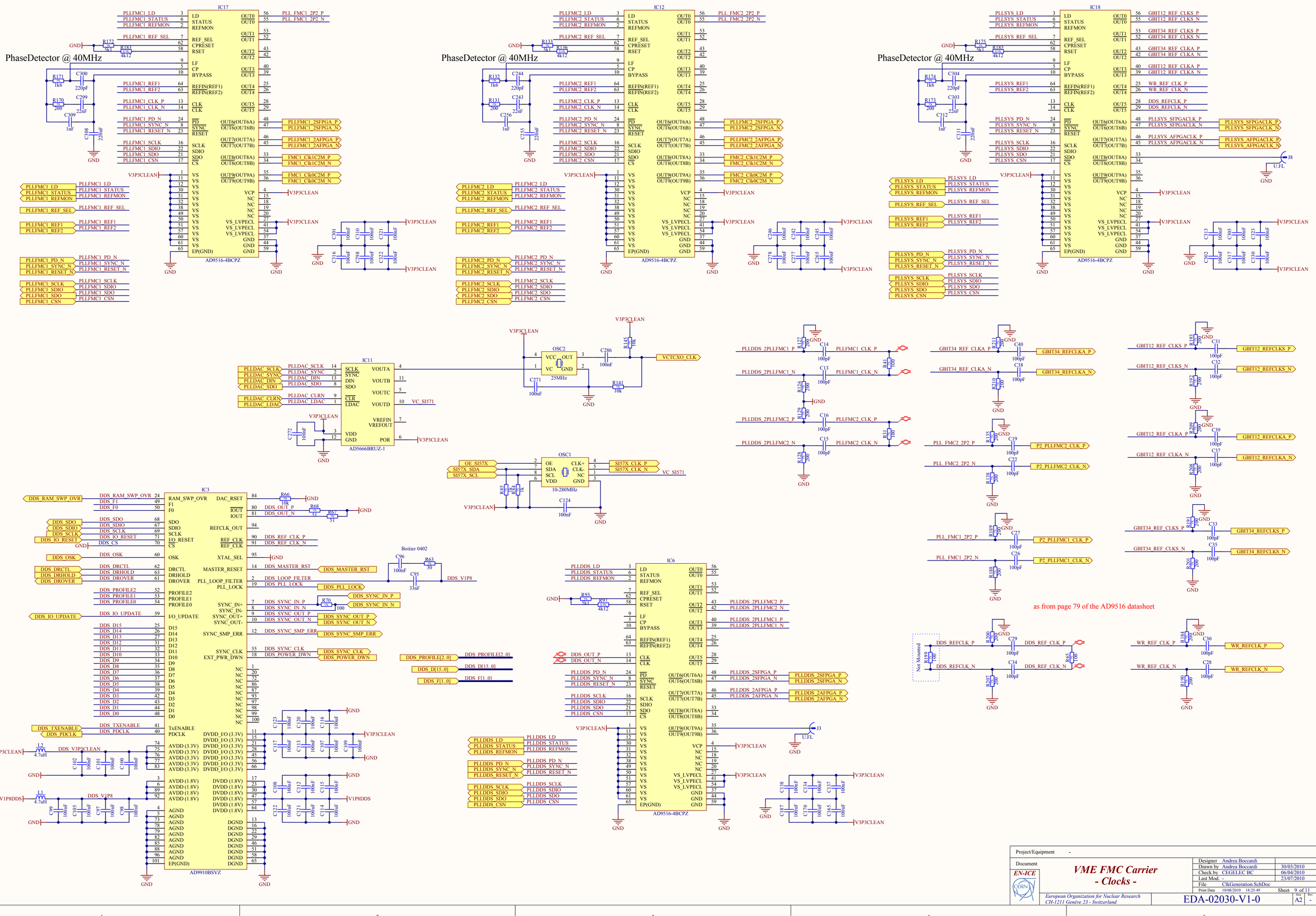


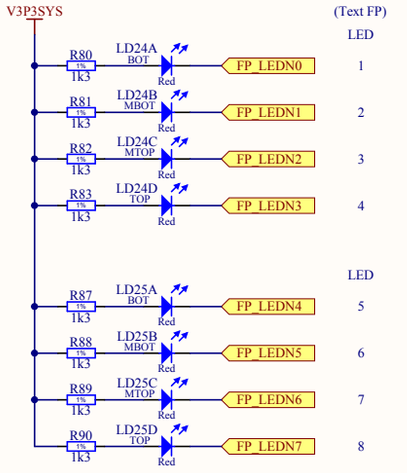
The VREF could not be used for the 2nd mezzanine
The 2nd mezzanine has 2 differential IO pairs less

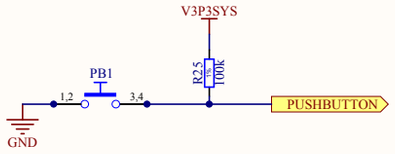
Project/Equipment	-		
Document	**VME FMC Carrier - Application FPGA -**	Designer	Andrea Boccardi
AB-BI		Drawn by	Andrea Boccardi 30/03/2010
		Check by	CEGELEC CB 06/04/2010
		Last Mod.	- 06/08/2010
		File	AFPGA.SchDoc
		Print Date	10/08/2010 18:25:46 Sheet 7 of 11
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02030-V1-0	Size A2	Rev -

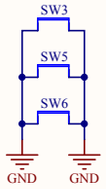
Add some TP (just vias) if there are spare pins

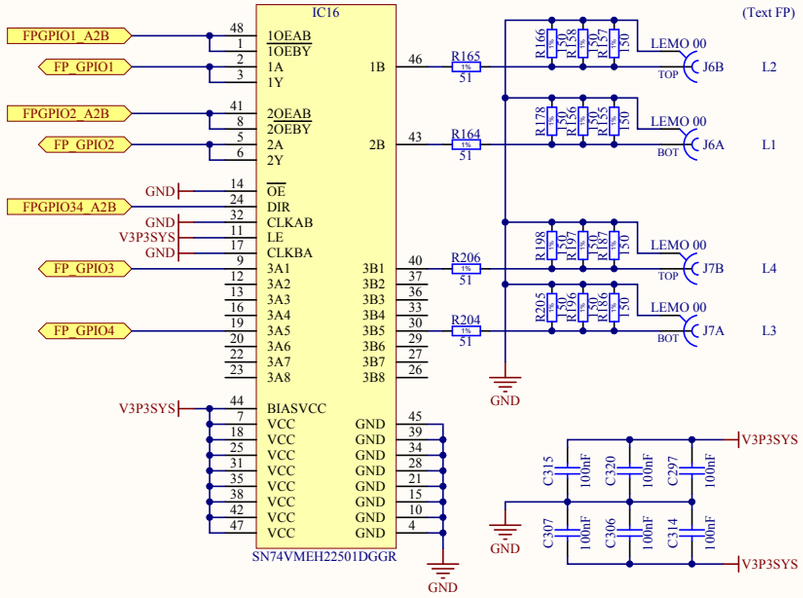


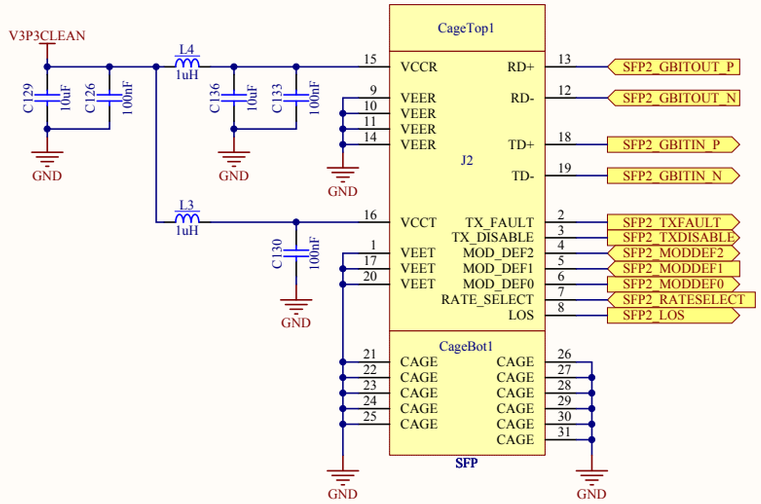

IC17
AD9516-4BCPZ
PhaseDetector @ 40MHz
PLLFMC1_LD
PLLFMC1_STATUS
PLLFMC1_REFMON
PLLFMC1_REF_SEL
PLLFMC1_REF1
PLLFMC1_REF2
PLLFMC1_CLK_P
PLLFMC1_CLK_N
PLLFMC1_PD_N
PLLFMC1_SYNC_N
PLLFMC1_RESET_N
PLLFMC1_SCLK
PLLFMC1_SDIO
PLLFMC1_SDO
PLLFMC1_CSN
PLL_FMC1_2P2_P
PLL_FMC1_2P2_N
PLLFMC1_2SFPGA_P
PLLFMC1_2SFPGA_N
PLLFMC1_2AFPGA_P
PLLFMC1_2AFPGA_N
FMC1_Clk1C2M_P
FMC1_Clk1C2M_N
FMC1_Clk0C2M_P
FMC1_Clk0C2M_N
V3P3CLEAN
GND
IC12
AD9516-4BCPZ
PhaseDetector @ 40MHz
PLLFMC2_LD
PLLFMC2_STATUS
PLLFMC2_REFMON
PLLFMC2_REF_SEL
PLLFMC2_REF1
PLLFMC2_REF2
PLLFMC2_CLK_P
PLLFMC2_CLK_N
PLLFMC2_PD_N
PLLFMC2_SYNC_N
PLLFMC2_RESET_N
PLLFMC2_SCLK
PLLFMC2_SDIO
PLLFMC2_SDO
PLLFMC2_CSN
PLL_FMC2_2P2_P
PLL_FMC2_2P2_N
PLLFMC2_2SFPGA_P
PLLFMC2_2SFPGA_N
PLLFMC2_2AFPGA_P
PLLFMC2_2AFPGA_N
FMC2_Clk1C2M_P
FMC2_Clk1C2M_N
FMC2_Clk0C2M_P
FMC2_Clk0C2M_N
V3P3CLEAN
GND
IC18
AD9516-4BCPZ
PhaseDetector @ 40MHz
PLLSYS_LD
PLLSYS_STATUS
PLLSYS_REFMON
PLLSYS_REF_SEL
PLLSYS_REF1
PLLSYS_REF2
PLLSYS_PD_N
PLLSYS_SYNC_N
PLLSYS_RESET_N
PLLSYS_SCLK
PLLSYS_SDIO
PLLSYS_SDO
PLLSYS_CSN
GBIT12_REF_CLKS_P
GBIT12_REF_CLKS_N
GBIT34_REF_CLKS_P
GBIT34_REF_CLKS_N
GBIT34_REF_CLKA_P
GBIT34_REF_CLKA_N
GBIT12_REF_CLKA_P
GBIT12_REF_CLKA_N
WR_REF_CLK_P
WR_REF_CLK_N
DDS_REFCLK_P
DDS_REFCLK_N
PLLSYS_SFPGACLK_P
PLLSYS_SFPGACLK_N
PLLSYS_AFPGACLK_P
PLLSYS_AFPGACLK_N
J8
U.FL
V3P3CLEAN
GND
IC11
AD5666BRUZ-1
PLLDAC_SCLK
PLLDAC_SYNC
PLLDAC_DIN
PLLDAC_SDO
PLLDAC_CLRN
PLLDAC_LDAC
VC_SI571
VCTCXO_CLK
OSC2
25MHz
OSC1
10-280MHz
OE_SI57X
SI57X_SDA
SI57X_SCL
SI57X_CLK_P
SI57X_CLK_N
IC3
AD9910BSVZ
DDS_RAM_SWP_OVR
DDS_F1
DDS_F0
DDS_SDO
DDS_SDIO
DDS_SCLK
DDS_IO_RESET
DDS_CS
DDS_OSK
DDS_DRCTL
DDS_DRHOLD
DDS_DROVER
DDS_PROFILE2
DDS_PROFILE1
DDS_PROFILE0
DDS_IO_UPDATE
DDS_D15
DDS_D14
DDS_D13
DDS_D12
DDS_D11
DDS_D10
DDS_D9
DDS_D8
DDS_D7
DDS_D6
DDS_D5
DDS_D4
DDS_D3
DDS_D2
DDS_D1
DDS_D0
DDS_TXENABLE
DDS_PDCLK
DDS_V3P3CLEAN
DDS_V1P8
V1P8DDS
DDS_MASTER_RST
DDS_PLL_LOCK
DDS_SYNC_IN_P
DDS_SYNC_IN_N
DDS_SYNC_OUT_P
DDS_SYNC_OUT_N
DDS_SYNC_SMP_ERR
DDS_SYNC_CLK
DDS_POWER_DWN
DDS_REF_CLK_P
DDS_REF_CLK_N
DDS_OUT_P
DDS_OUT_N
Boitier 0402
DDS_V1P8
DDS_PROFILE[2..0]
DDS_D[15..0]
DDS_F[1..0]
IC6
PLLDDS_2PLLFMC2_P
PLLDDS_2PLLFMC2_N
PLLDDS_2PLLFMC1_P
PLLDDS_2PLLFMC1_N
PLLDDS_2SFPGA_P
PLLDDS_2SFPGA_N
PLLDDS_2AFPGA_P
PLLDDS_2AFPGA_N
U.FL
as from page 79 of the AD9516 datasheet
Not Mounted
Project/Equipment -
Document
EN-ICE
VME FMC Carrier
- Clocks -
Designer Andrea Boccardi
Drawn by Andrea Boccardi 30/03/2010
Check.by CEGELEC BC 06/04/2010
Last Mod. - 23/07/2010
File ClkGeneration.SchDoc
Print Date 10/08/2010 18:25:49
Sheet 9 of 11
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
EDA-02030-V1-0
Size A2
Rev -

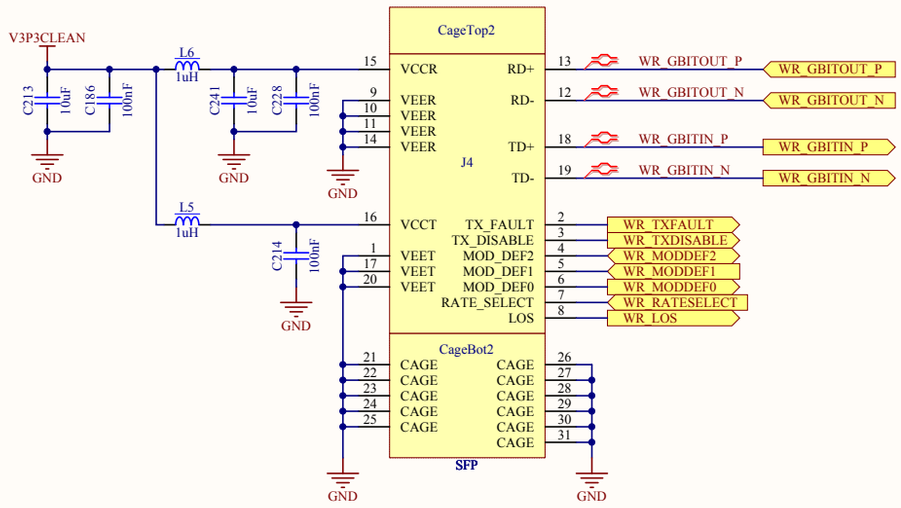


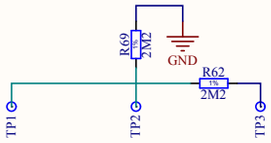


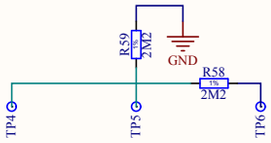












Project/Equipment -

Document

EN-ICE

VME FMC Carrier - Front Panel -

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Drawn by	Andrea Boccardi	30/03/2010
Check.by	CEGELEC BC	06/04/2010
Last Mod.	-	23/07/2010
File	FrontPannel.SchDoc	
Print Date	10/08/2010 18:25:49	Sheet 10 of 11

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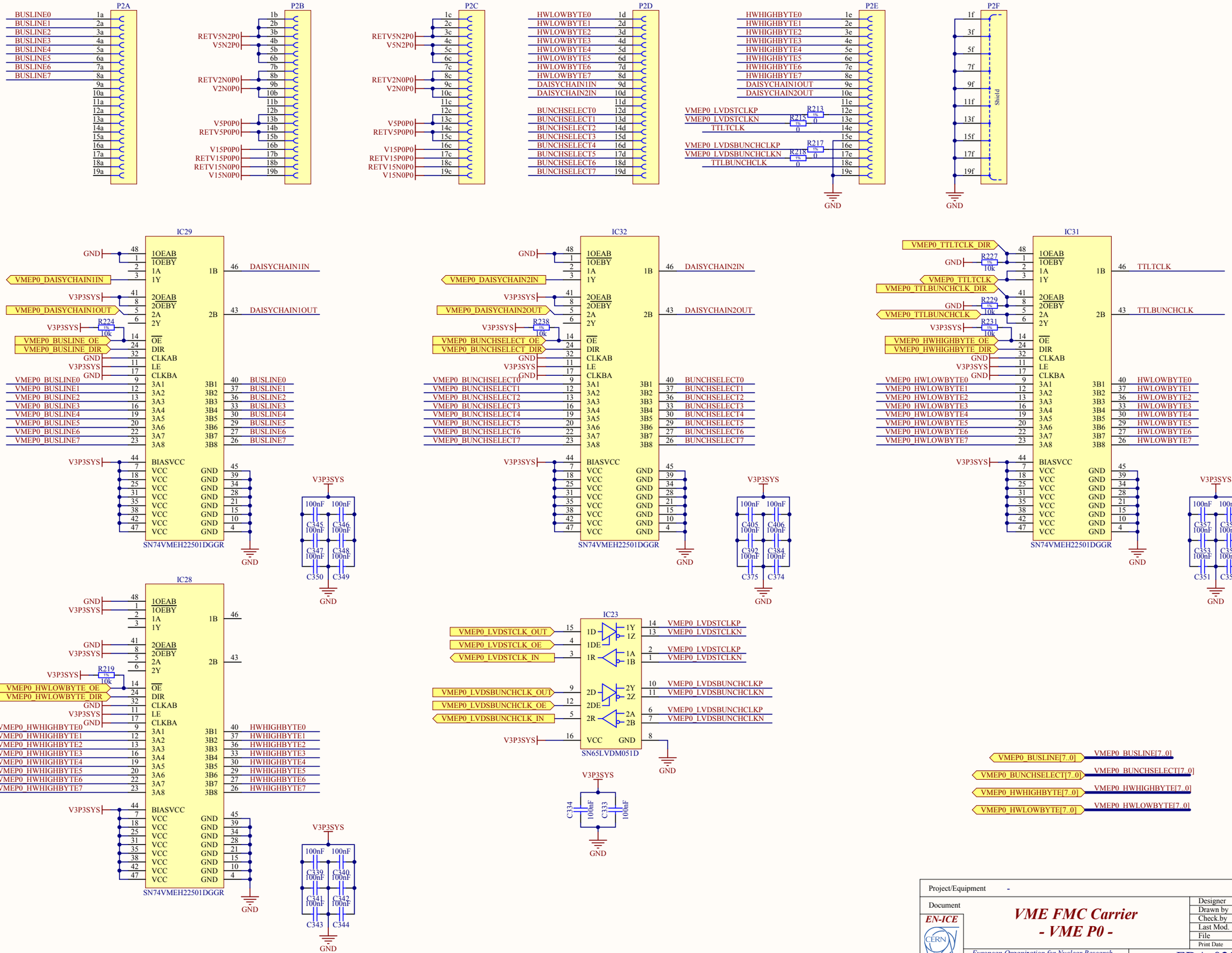

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Document	VME FMC Carrier - VME P0 -
EN-ICE	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland
Designer	Andrea Boccardi
Drawn by	Andrea Boccardi 30/03/2010
Check.by	CEGELEC BC 06/04/2010
Last Mod.	- 23/07/2010
File	VMEP0.SchDoc
Print Date	10/08/2010 18:25:50
Sheet	11 of 11
EDA-02030-V1-0	Size A3, Rev -