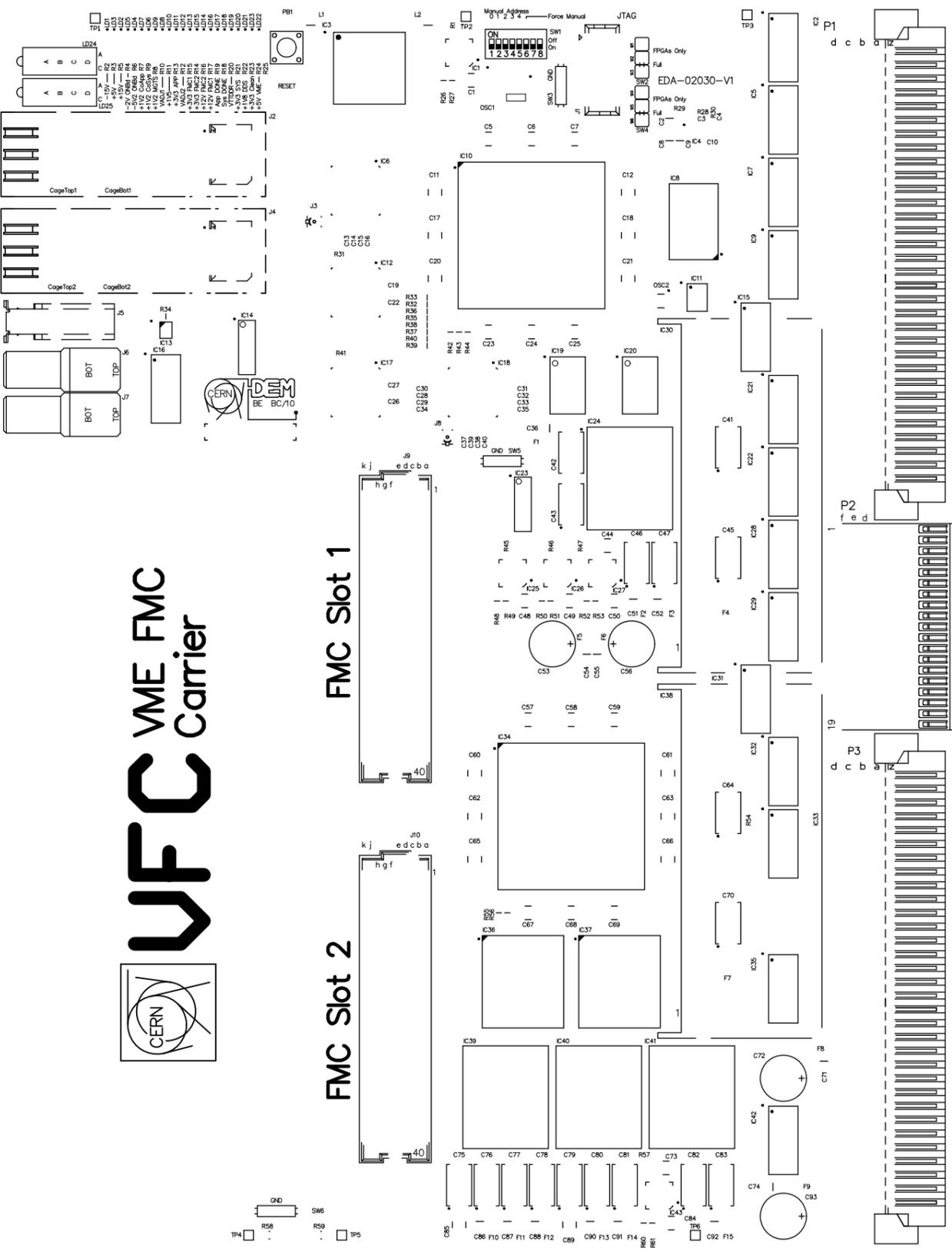


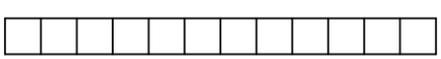
VFC VME FMC Carrier

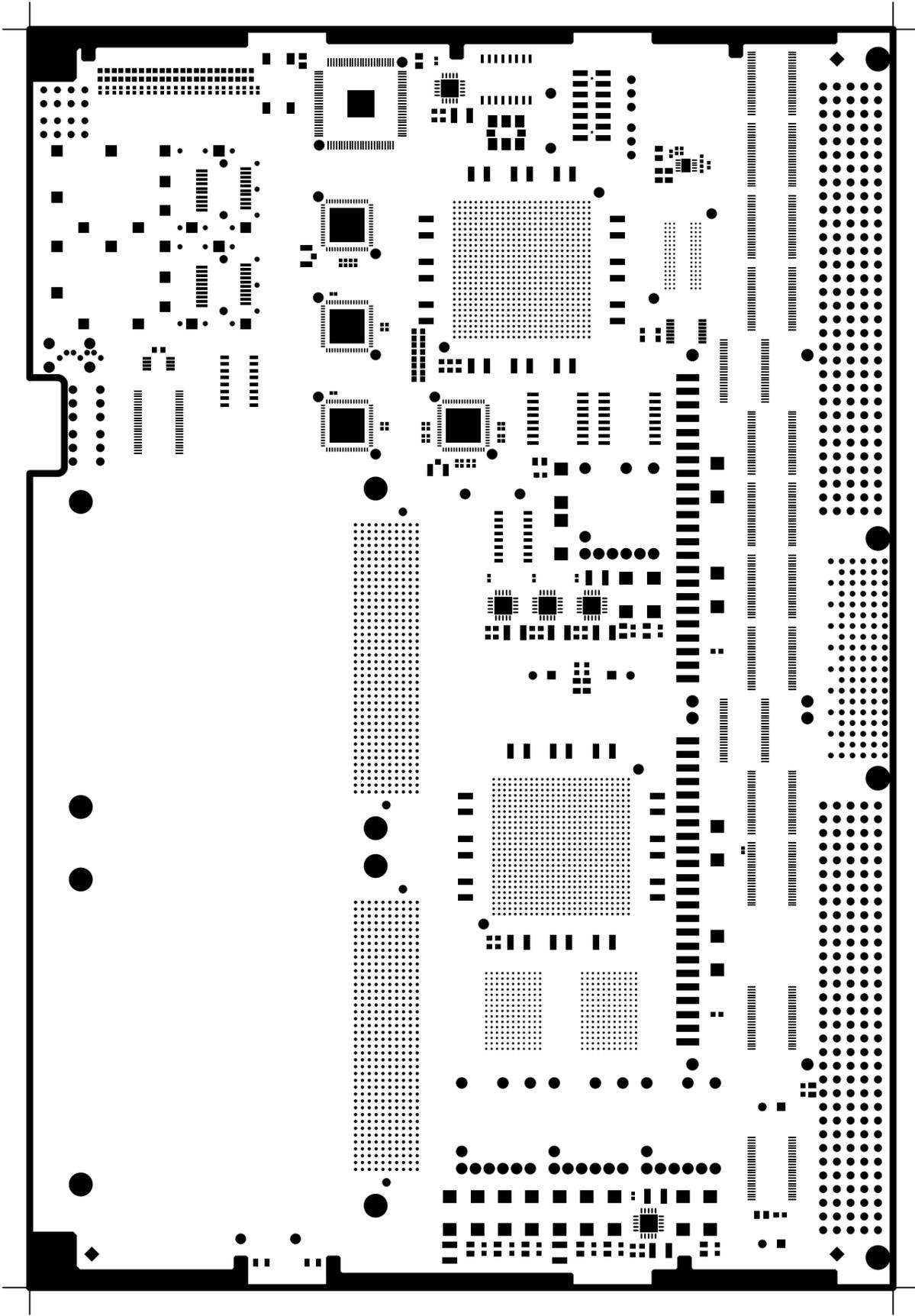


Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

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Top Overlay

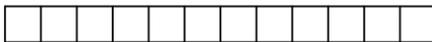


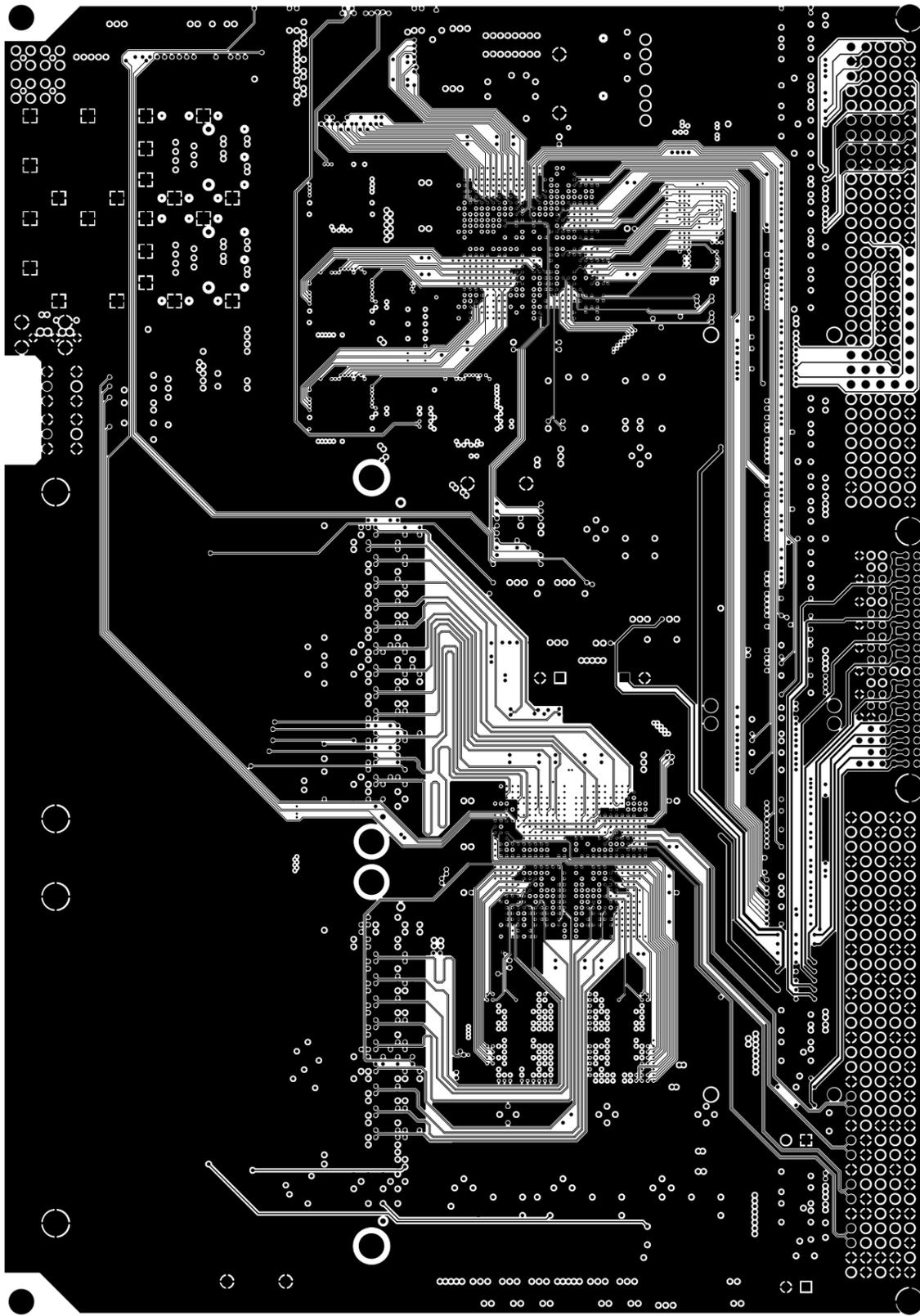


Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

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Top Solder

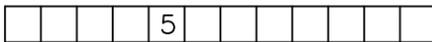


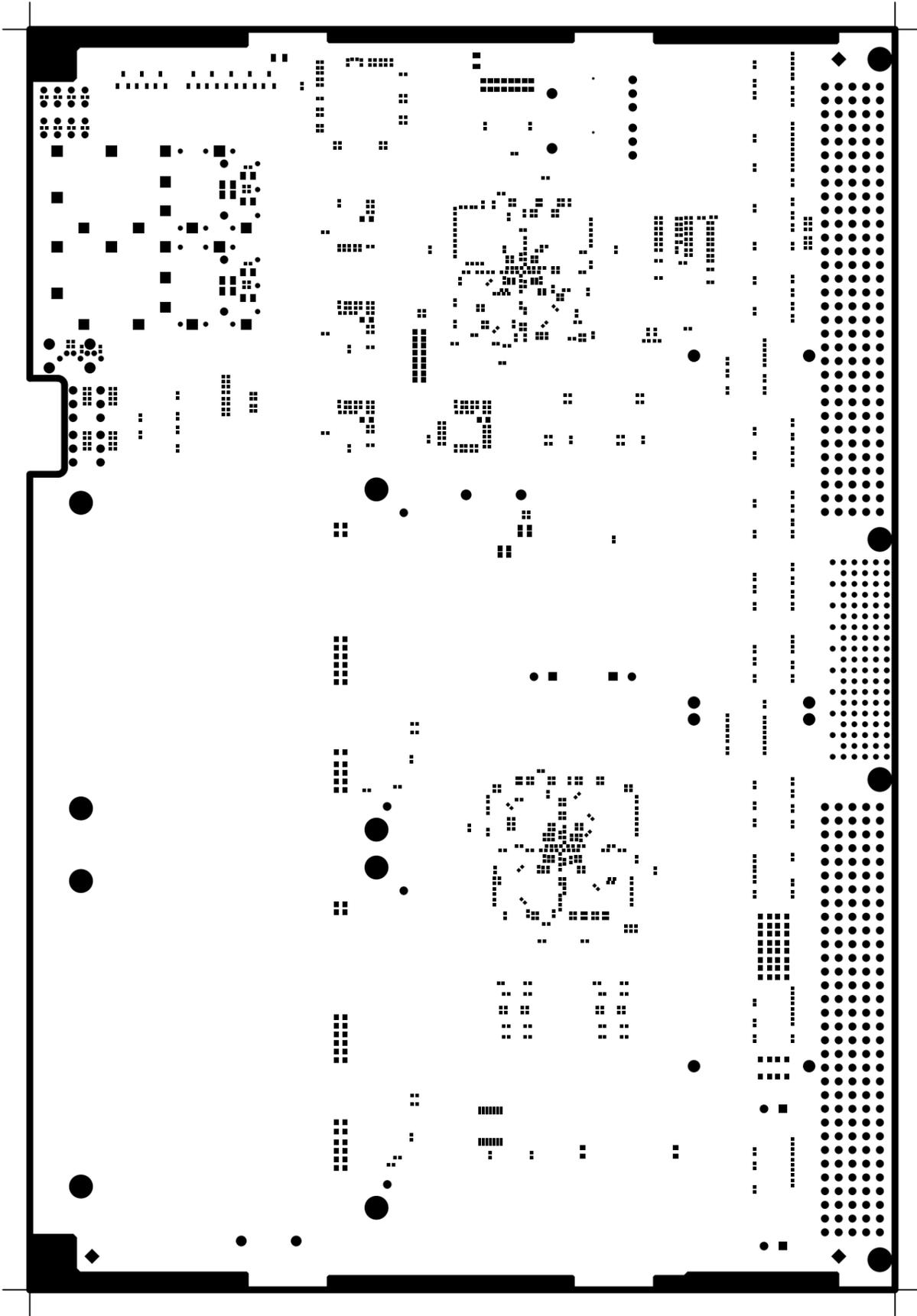


Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

Print Date 13/08/2010 17:28:17
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L5

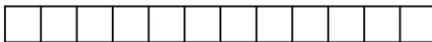


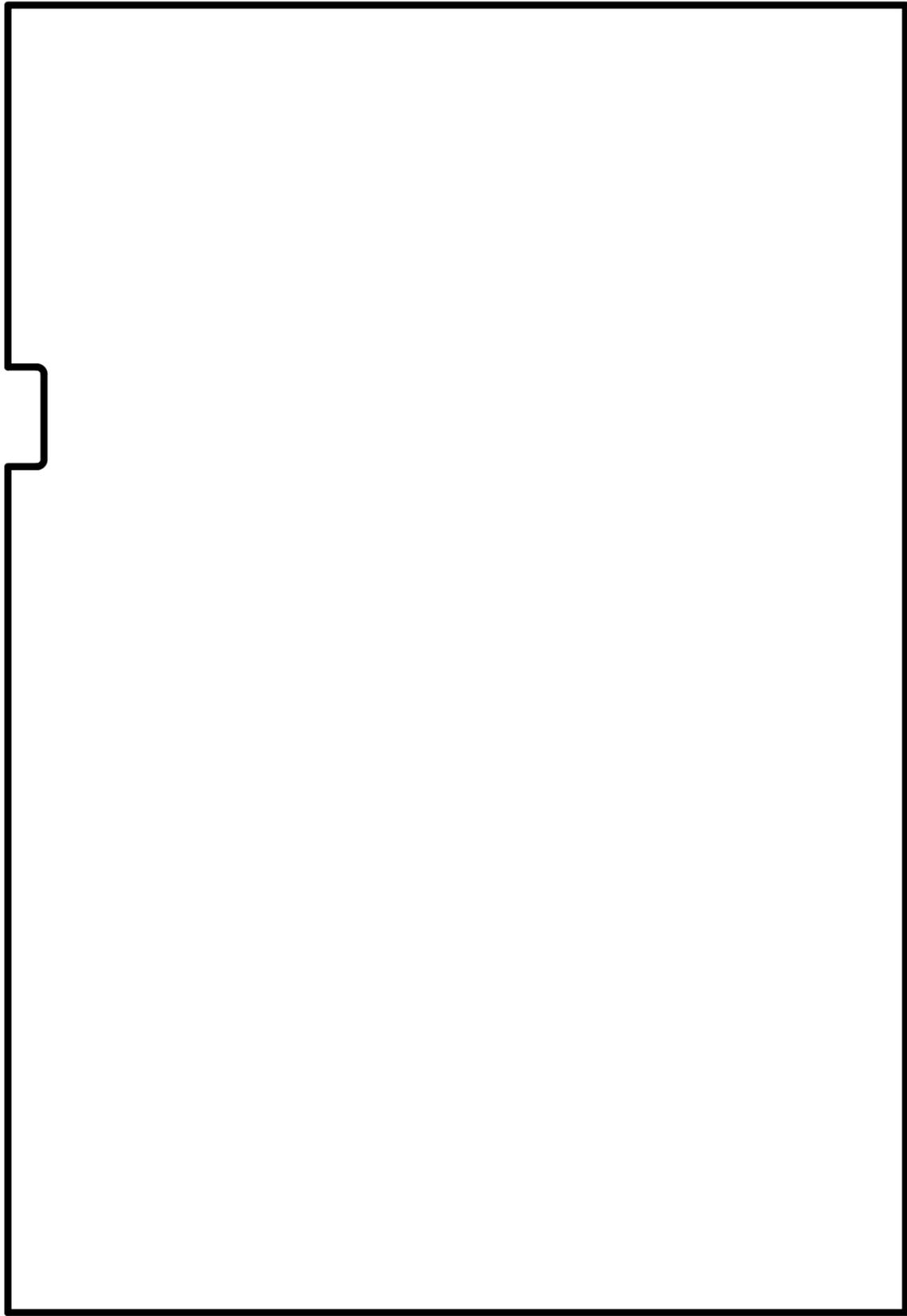


Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

Print Date 13/08/2010 17:31:32
SCALE: 1.00

Bottom solder

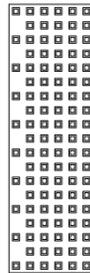
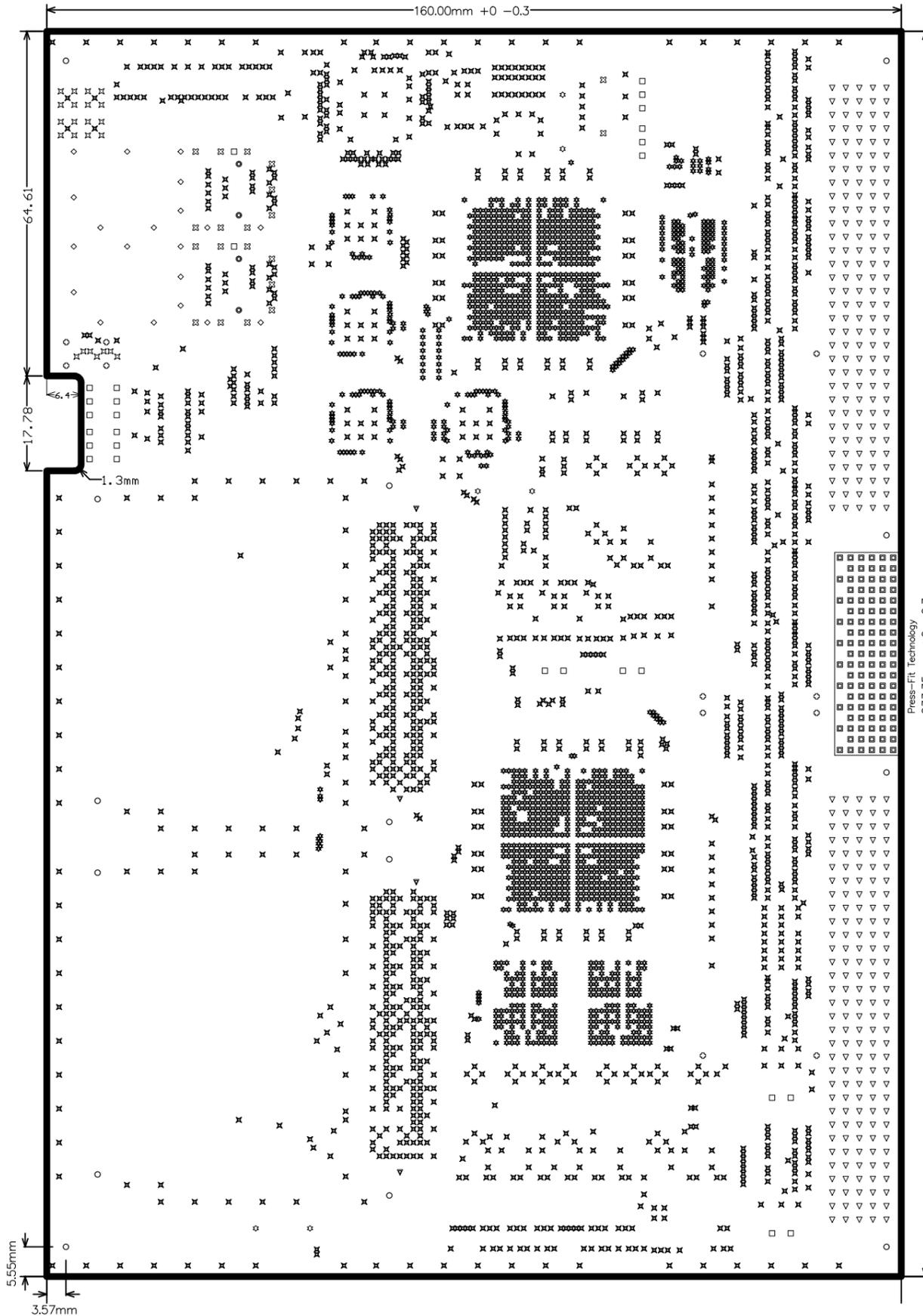




Symbol	Hit Count	Tool Size	Plated	Hole Type
★	1663	7.874mil (0.2mm)	PTH	Round
✕	1903	11.811mil (0.3mm)	PTH	Round
⊠	105	23.622mil (0.6mm)	PTH	Round
✕	23	31.496mil (0.8mm)	PTH	Round
□	28	35.433mil (0.9mm)	PTH	Round
⊠	20	39.37mil (1mm)	NPTH	Round
▽	320	39.37mil (1mm)	PTH	Round
◇	20	43.307mil (1.1mm)	PTH	Round
▽	4	51.181mil (1.3mm)	NPTH	Round
☆	6	51.181mil (1.3mm)	PTH	Round
⊙	4	62.992mil (1.6mm)	NPTH	Round
⊙	12	70.866mil (1.8mm)	PTH	Round
○	14	106.299mil (2.7mm)	PTH	Round
	4122 Total			

LAYER IDENTIFICATION		LINE WIDTH/GAP (Mils)	FINISHED COPPER THICKNESS	CONTROLLED IMPEDANCE +/-10%	DIELECTRIC THICKNESS
TOP LAYER	SIGNAL LAYER	9 / 12	35 um	50/*100 Ohms	*=CRITICAL
LAYER 2	POWER PLANE	-	35 um		* 0.150mm
LAYER 3	SIGNAL LAYER	4 / 5	35 um	50/*100 Ohms	* 0.100mm
LAYER 4	POWER PLANE	-	35 um		0.100mm
LAYER 5	SIGNAL LAYER	4 / 5	35 um	50/*100 Ohms	* 0.100mm
LAYER 6	POWER PLANE	-	35 um		0.100mm
LAYER 7	POWER PLANE	-	35 um		0.100mm
LAYER 8	SIGNAL LAYER	4 / 5	35 um	50/*100 Ohms	* 0.100mm
LAYER 9	POWER PLANE	-	35 um		0.100mm
LAYER 10	SIGNAL LAYER	4 / 5	35 um	50/*100 Ohms	* 0.100mm
LAYER 11	GND PLANE	-	35 um		* 0.150mm
BOTTOM LAYER	SIGNAL LAYER	9 / 12	35 um	50/*100 Ohms	* 0.150mm
FINISHED BOARD THICKNESS +/-10%					1.6 mm

*100 Ohms = Differential Impedance



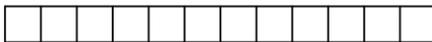
Press-Fit Technology
233.35mm +/- 0.3

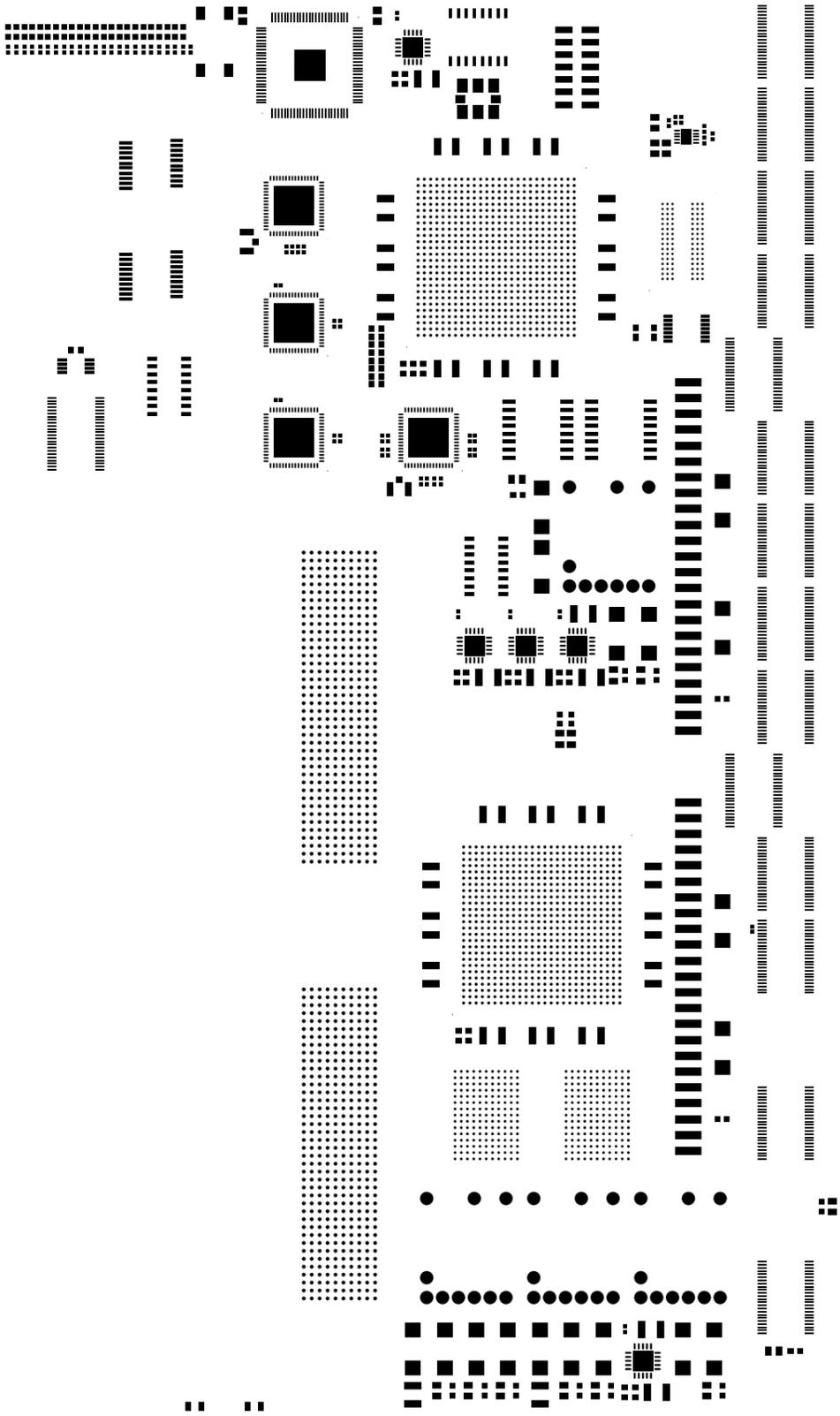


Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

Print Date 13/08/2010 17:31:33
SCALE: 1.00

Components 951
Pins 6361
Vias 3566
Holes 4122
Nets 1210

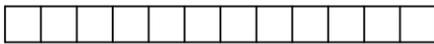


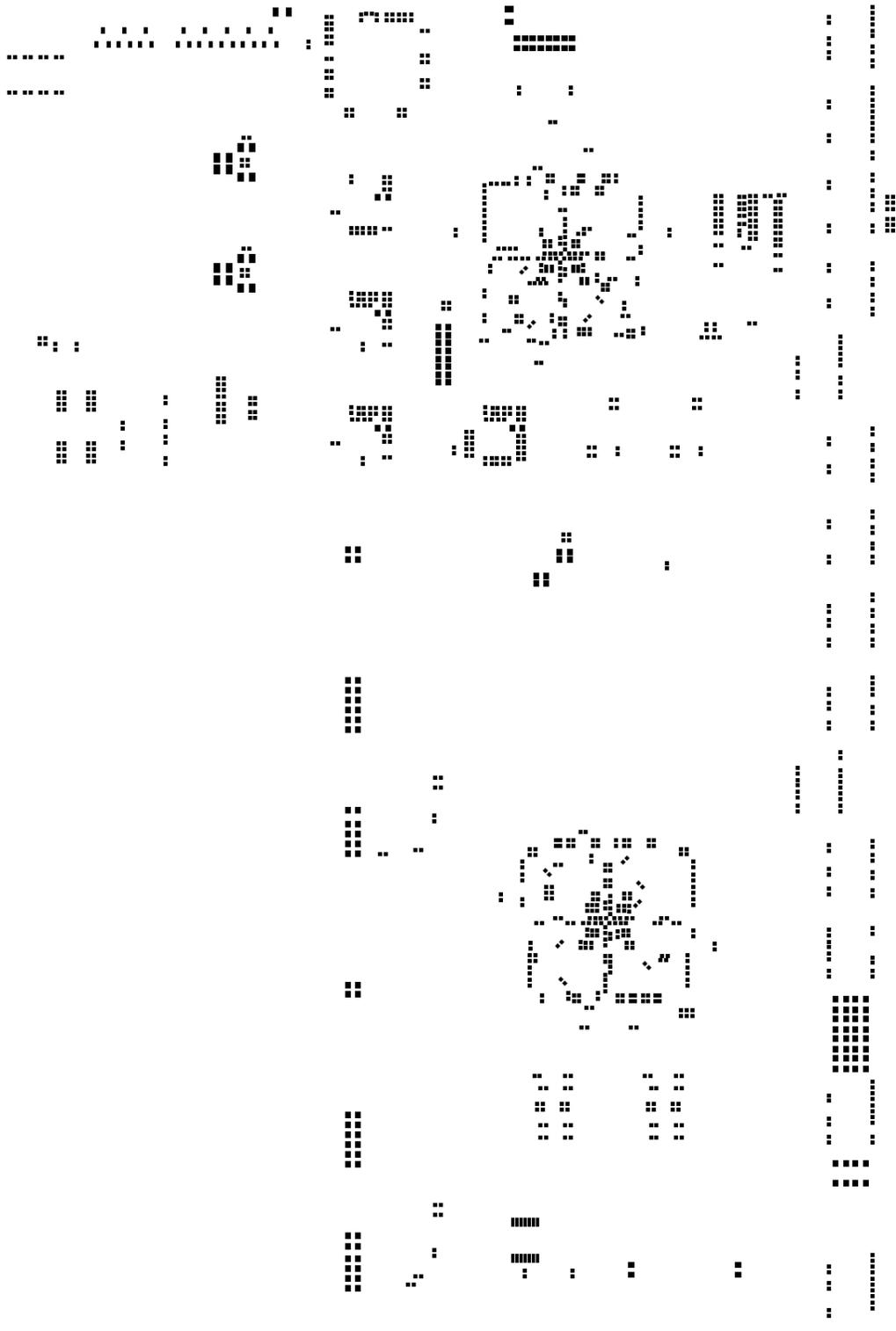


Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

Print Date 13/08/2010 17:31:22
SCALE: 1.00

Top Paste





Number	EDA-02030-V1
Drawn By	CEGELEC BC
DATE	19-04-2010
MOD.	-

Print Date 13/08/2010 17:31:23
SCALE: 1.00

Bottom Paste

