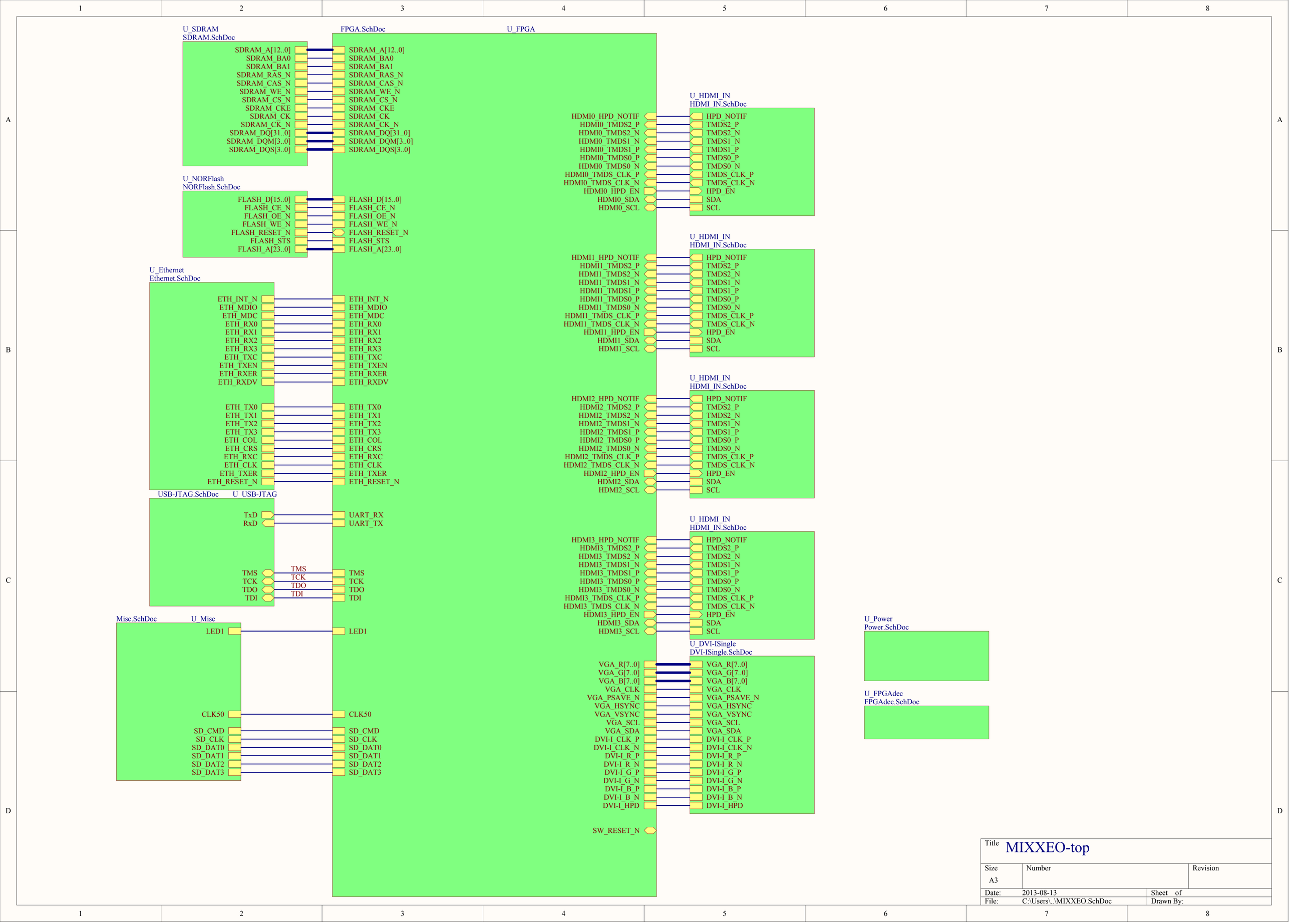

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Number	
Revision	
Date:	2013-08-13
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File:	C:\Users\..\MIXXEO.SchDoc
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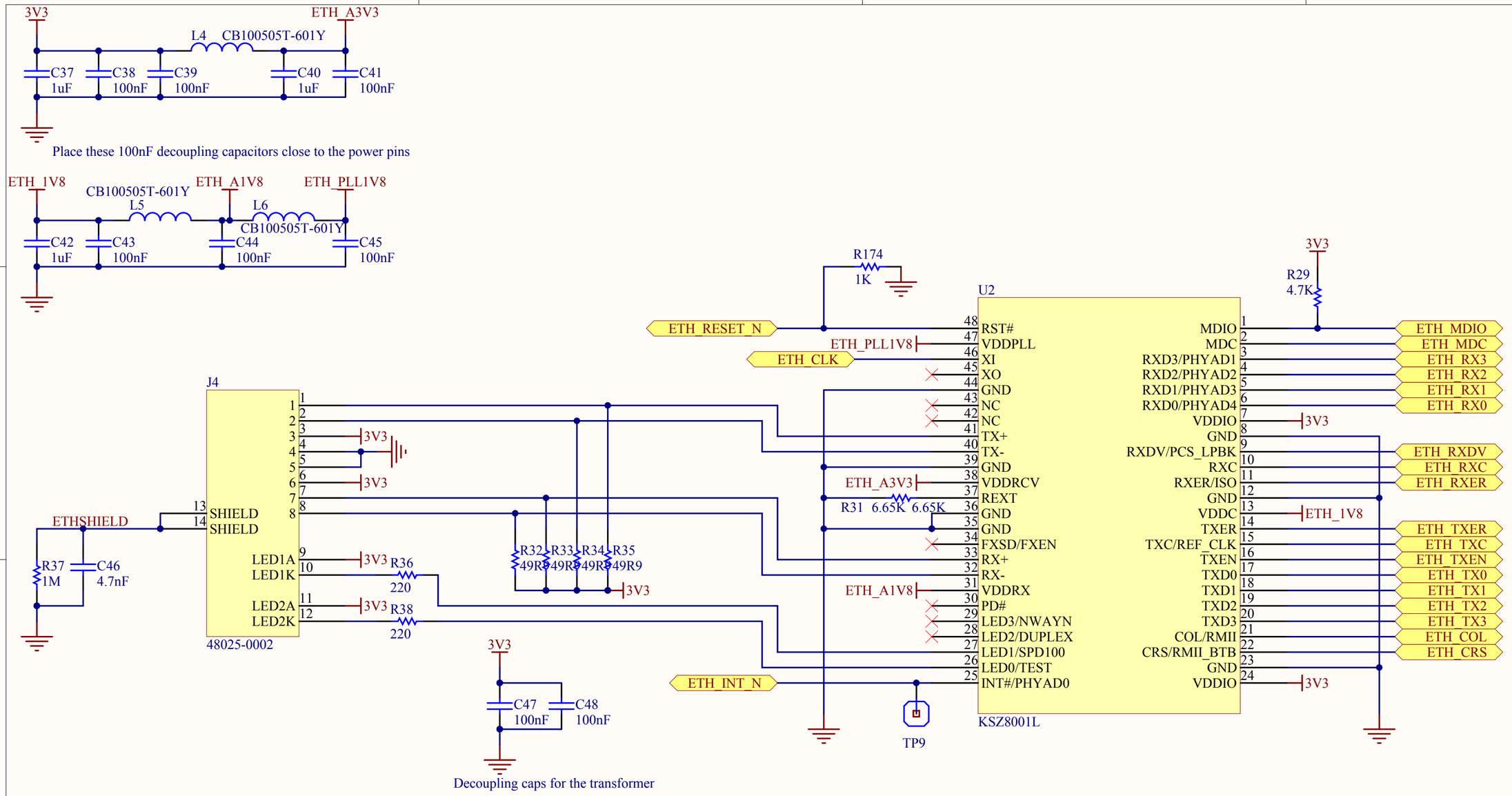

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Date: 2013-08-13		Sheet of
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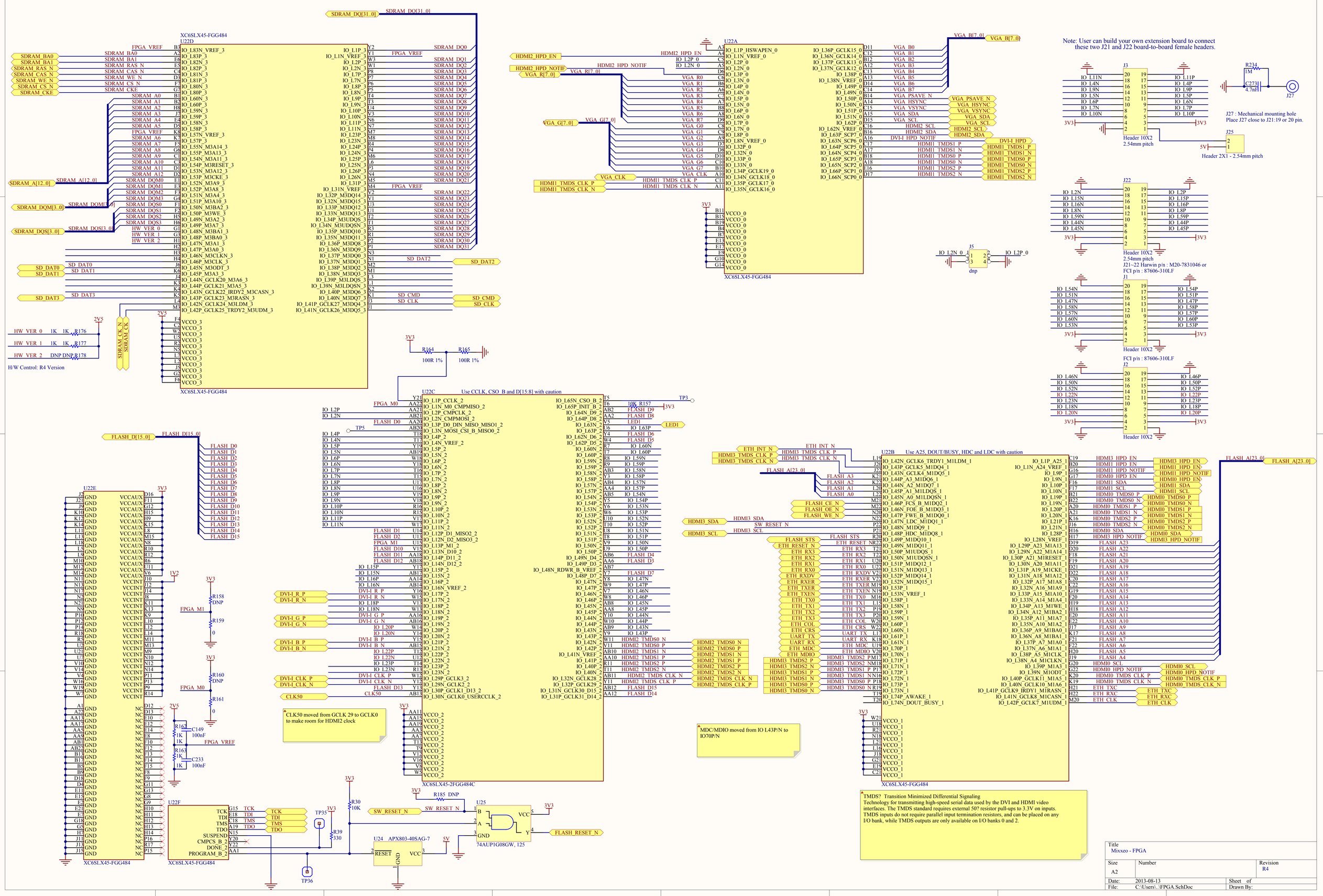
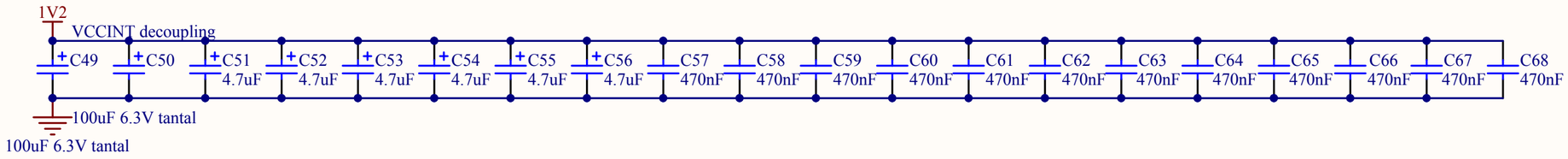
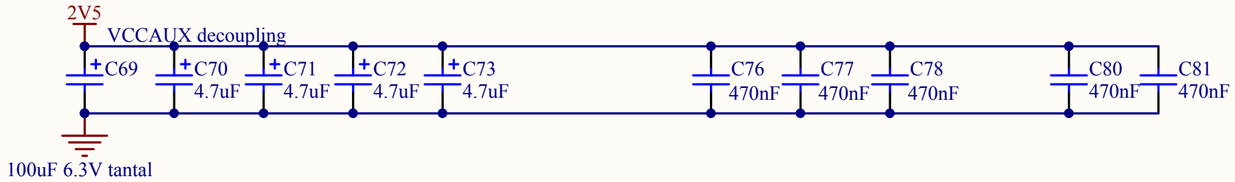
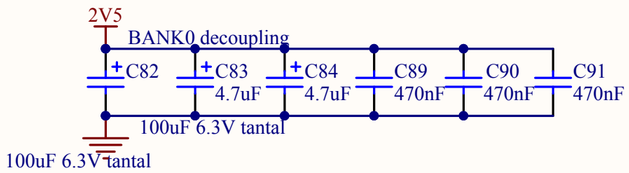
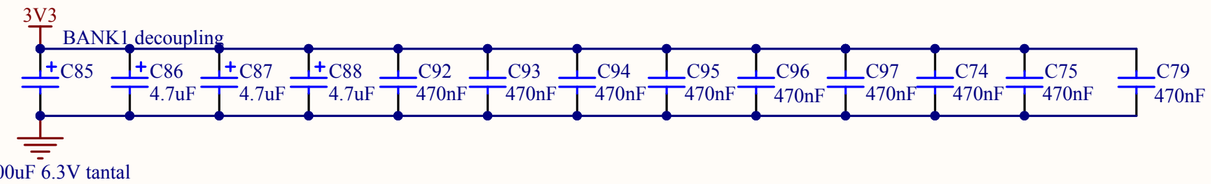
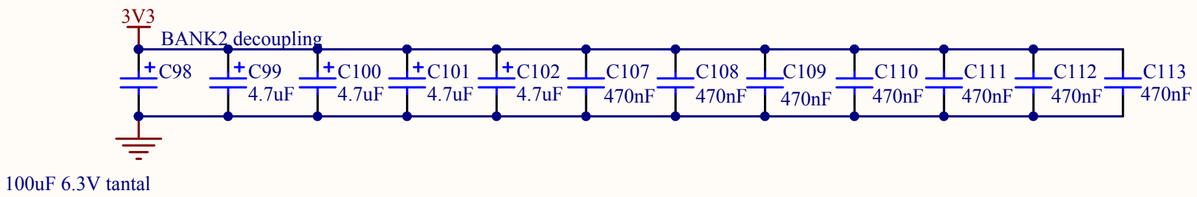

XC6LX45-FGG484
U22D
SDRAM_DQ[31..0]
SDRAM_DQ[31..0]
SDRAM_BA0
SDRAM_BA1
SDRAM_RAS_N
SDRAM_CAS_N
SDRAM_WE_N
SDRAM_CS_N
SDRAM_CKE
SDRAM_A[12..0]
SDRAM_DQM[3..0]
SDRAM_DQS[3..0]
SD_DAT0
SD_DAT1
SD_DAT3
SD_DAT2
SD_CMD
SD_CLK
HW_VER_0
HW_VER_1
HW_VER_2
SDRAM_CK_N
SDRAM_CK
H/W Control: R4 Version
R176 1K
R177 1K
R178 DNP
2V5
3V3
1V2
FPGA_VREF
FPGA_M1
FPGA_M0
R158 DNP
R159 0
R160 DNP
R161 0
R162 1K
R163 1K
C149 100nF
C233 100nF
U22E
U22F
U22C
Use CCLK, CSO_B and D[15:8] with caution
FPGA_M0
TP5
FLASH_D[15..0]
FLASH_D[15..0]
FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4
FLASH_D5
FLASH_D6
FLASH_D7
FLASH_D8
FLASH_D9
FLASH_D10
FLASH_D11
FLASH_D12
FLASH_D13
FLASH_D14
FLASH_D15
TCK
TDI
TMS
TDO
TP35
TP36
R30 10K
R39 330
SW_RESET_N
R185 DNP
U24 APX803-40SAG-7
RESET
GND
VCC
5V
U25
74AUP1G08GW, 125
FLASH_RESET_N
TP3
10K R157
FLASH_D9
FLASH_D8
LED1
FLASH_D6
FLASH_D5
FLASH_D4
FLASH_D3
FLASH_D2
FLASH_D1
FLASH_D0
XC6SLX45-2FGG484C
CLK50 moved from GCLK 29 to GCLK0 to make room for HDMI2 clock
U22A
HDMI2_HPD_EN
HDMI2_HPD_NOTIF
VGA_R[7..0]
VGA_G[7..0]
VGA_CLK
HDMI1_TMDS_CLK_P
HDMI1_TMDS_CLK_N
HDMI2_TMDS0_N
HDMI2_TMDS0_P
HDMI2_TMDS1_N
HDMI2_TMDS1_P
HDMI2_TMDS2_P
HDMI2_TMDS2_N
HDMI2_TMDS_CLK_N
HDMI2_TMDS_CLK_P
VGA_B[7..0]
VGA_B0
VGA_B1
VGA_B2
VGA_B3
VGA_B4
VGA_B5
VGA_B6
VGA_B7
VGA_PSAVE_N
VGA_HSYNC
VGA_VSYNC
VGA_SDA
VGA_SCL
HDMI2_SCL
HDMI2_SDA
DVI-I_HPD
HDMI1_TMDS1_P
HDMI1_TMDS1_N
HDMI1_TMDS0_P
HDMI1_TMDS0_N
HDMI1_TMDS2_P
HDMI1_TMDS2_N
J5
dnp
Note: User can build your own extension board to connect these two J21 and J22 board-to-board female headers.
J3
Header 10X2
2.54mm pitch
R234 1M
C273 4.7nF
J27
J27 : Mechanical mounting hole
Place J27 close to J21:19 or 20 pin.
J25
Header 2X1 - 2.54mm pitch
J22
Header 10X2
2.54mm pitch
J21~22 Harwin p/n : M20-7831046 or
FCI p/n : 87606-310LF
J1
Header 10X2
FCI p/n : 87606-310LF
J2
Header 10X2
U22B
Use A25, DOUT/BUSY, HDC and LDC with caution
ETH_INT_N
FLASH_A[23..0]
FLASH_CE_N
FLASH_OE_N
FLASH_WE_N
HDMI3_SDA
HDMI3_SCL
SW_RESET_N
FLASH_STS
ETH_RESET_N
ETH_RX3
ETH_RX2
ETH_RX1
ETH_RX0
ETH_RXDV
ETH_RXER
ETH_TXER
ETH_TXEN
ETH_TX0
ETH_TX1
ETH_TX2
ETH_TX3
ETH_COL
ETH_CRS
UART_TX
UART_RX
ETH_MDC
ETH_MDIO
HDMI3_TMDS2_P
HDMI3_TMDS2_N
HDMI3_TMDS1_P
HDMI3_TMDS1_N
HDMI3_TMDS0_P
HDMI3_TMDS0_N
HDMI3_HPD_EN
HDMI1_HPD_EN
HDMI1_HPD_NOTIF
HDMI0_HPD_EN
HDMI1_SDA
HDMI1_SCL
HDMI0_TMDS0_P
HDMI0_TMDS0_N
HDMI0_TMDS1_P
HDMI0_TMDS1_N
HDMI0_TMDS2_P
HDMI0_TMDS2_N
HDMI0_SDA
HDMI3_HPD_NOTIF
HDMI0_SCL
HDMI0_HPD_NOTIF
HDMI0_TMDS_CLK_P
HDMI0_TMDS_CLK_N
ETH_TXC
ETH_RXC
ETH_CLK
MDC/MDIO moved from IO L43P/N to IO70P/N
TMDS? Transition Minimized Differential Signaling
Technology for transmitting high-speed serial data used by the DVI and HDMI video interfaces. The TMDS standard requires external 50? resistor pull-ups to 3.3V on inputs. TMDS inputs do not require parallel input termination resistors, and can be placed on any I/O bank, while TMDS outputs are only available on I/O banks 0 and 2.
Title
Mixxeo - FPGA
Size
A2
Number
Revision
R4
Date: 2013-08-13
File: C:\Users\..\FPGA.SchDoc
Sheet of
Drawn By:

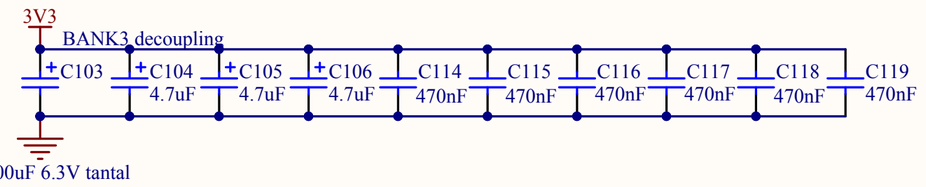












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Size: A4	Number:	Revision:
Date: 2013-08-13		Sheet of
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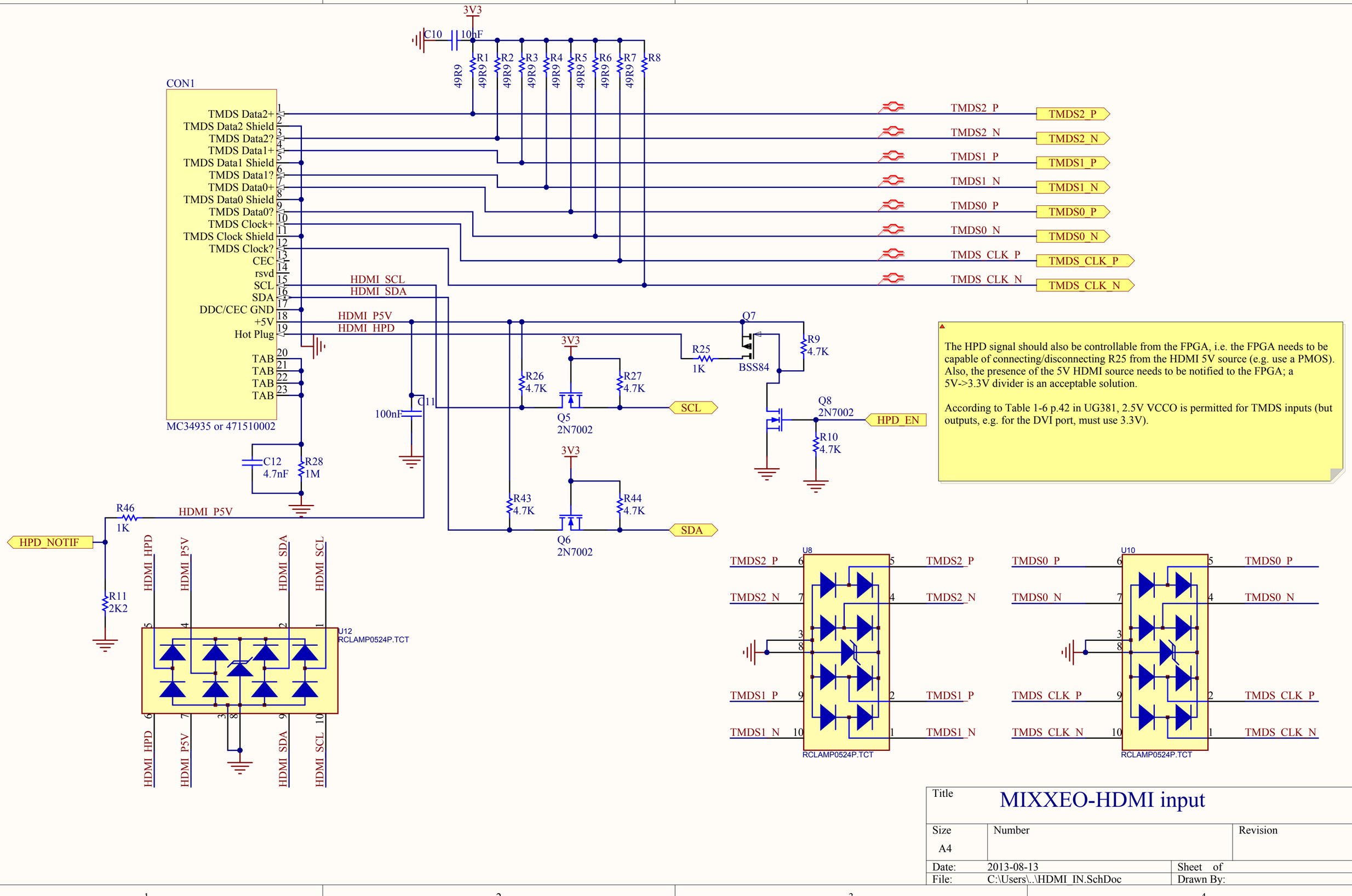
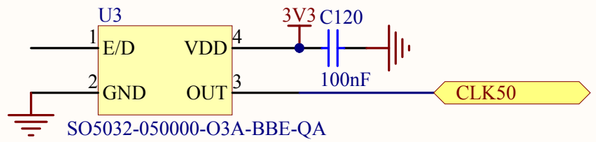
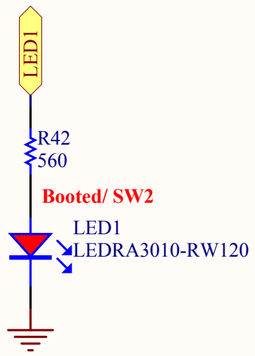


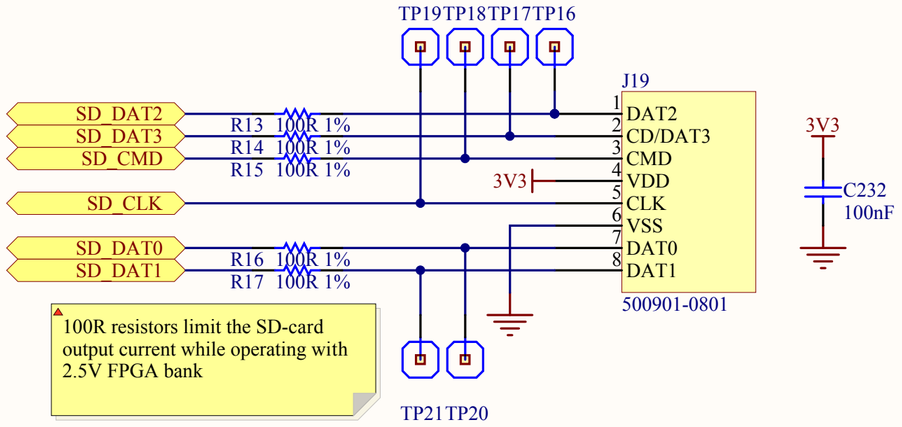
The HPD signal should also be controllable from the FPGA, i.e. the FPGA needs to be capable of connecting/disconnecting R25 from the HDMI 5V source (e.g. use a PMOS). Also, the presence of the 5V HDMI source needs to be notified to the FPGA; a 5V->3.3V divider is an acceptable solution.

According to Table 1-6 p.42 in UG381, 2.5V VCCO is permitted for TMDS inputs (but outputs, e.g. for the DVI port, must use 3.3V).

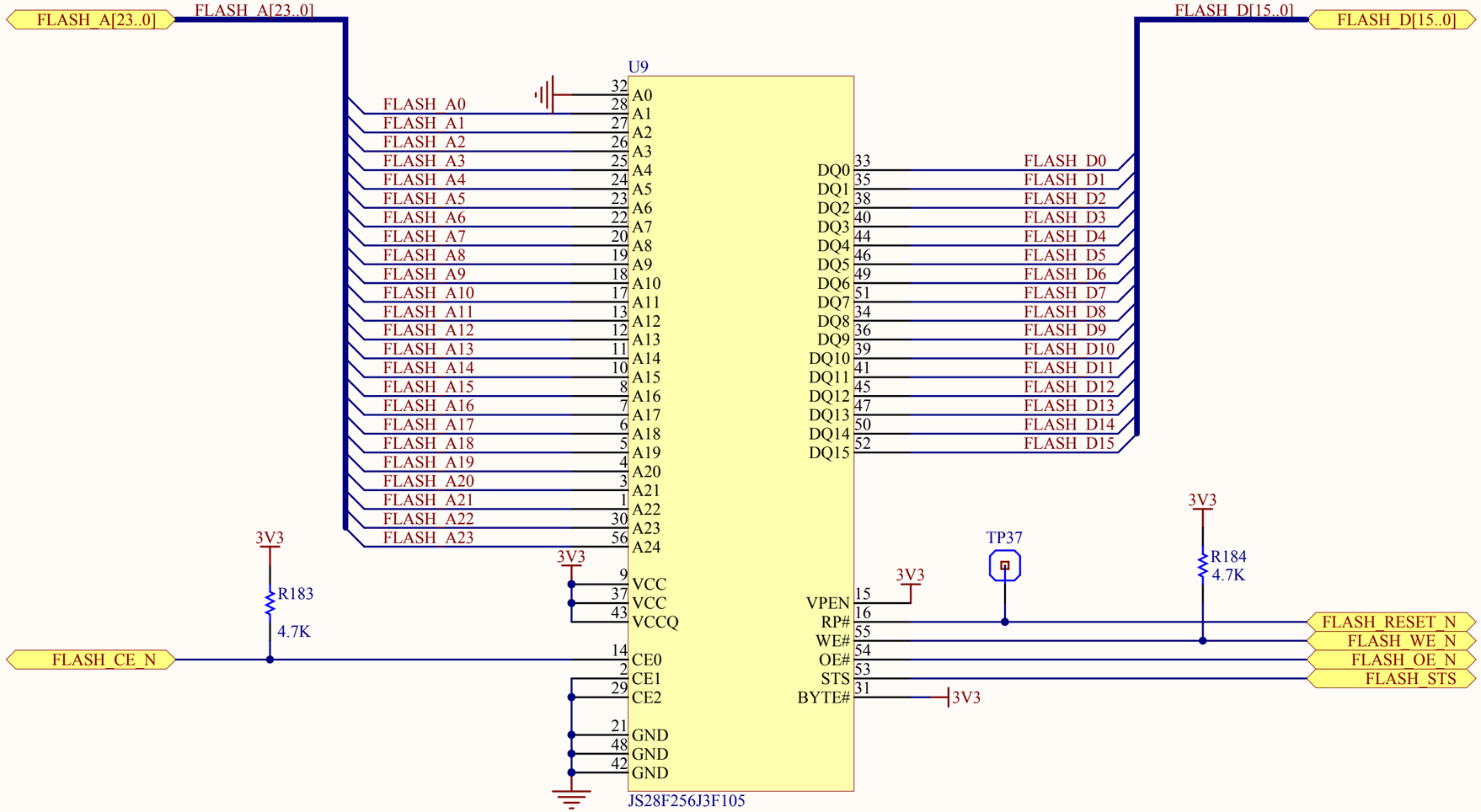
Title	MIXXEO-HDMI input	
Size: A4	Number:	Revision:
Date: 2013-08-13		Sheet of
File: C:\Users\..\HDMI_IN.SchDoc		Drawn By:

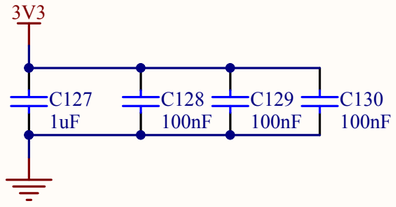






Title: Mixxeo - Misc.		
Size: A4	Number:	Revision: R4
Date: 2013-08-13		Sheet of
File: C:\Users\..\Misc.SchDoc		Drawn By:





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Size: A4	Number:	Revision: R4
Date: 2013-08-13		Sheet of
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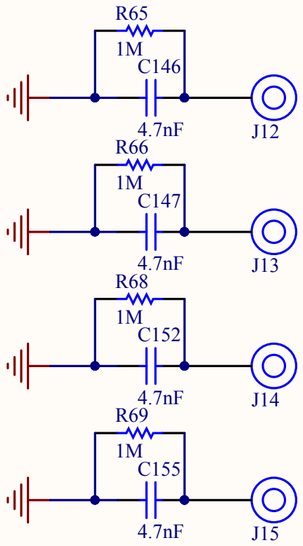
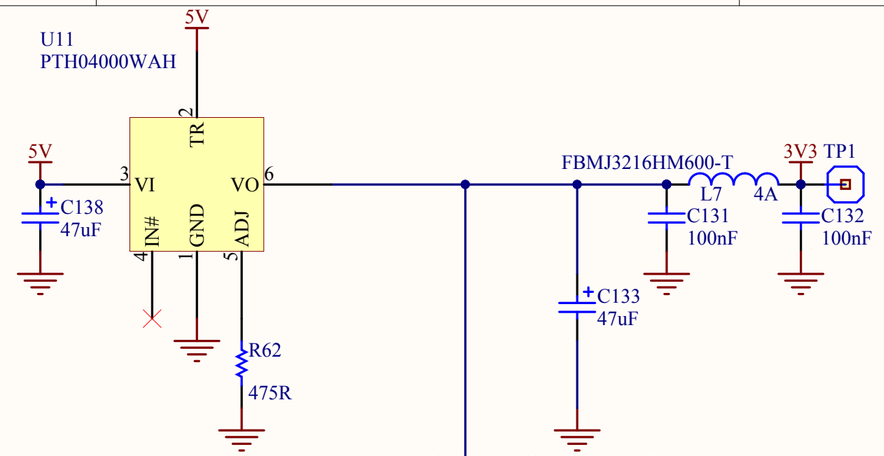
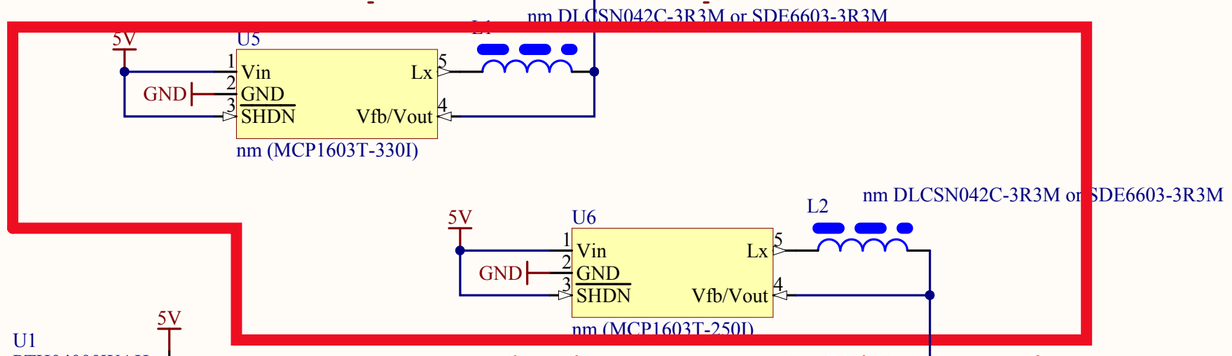
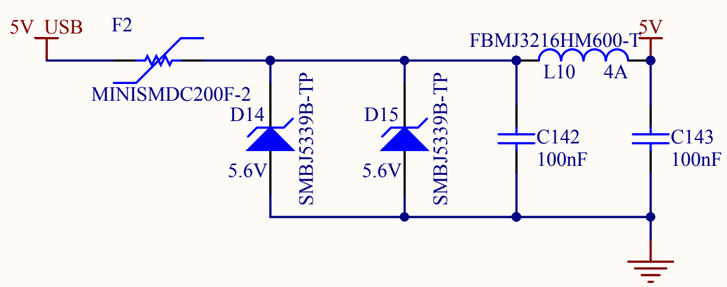


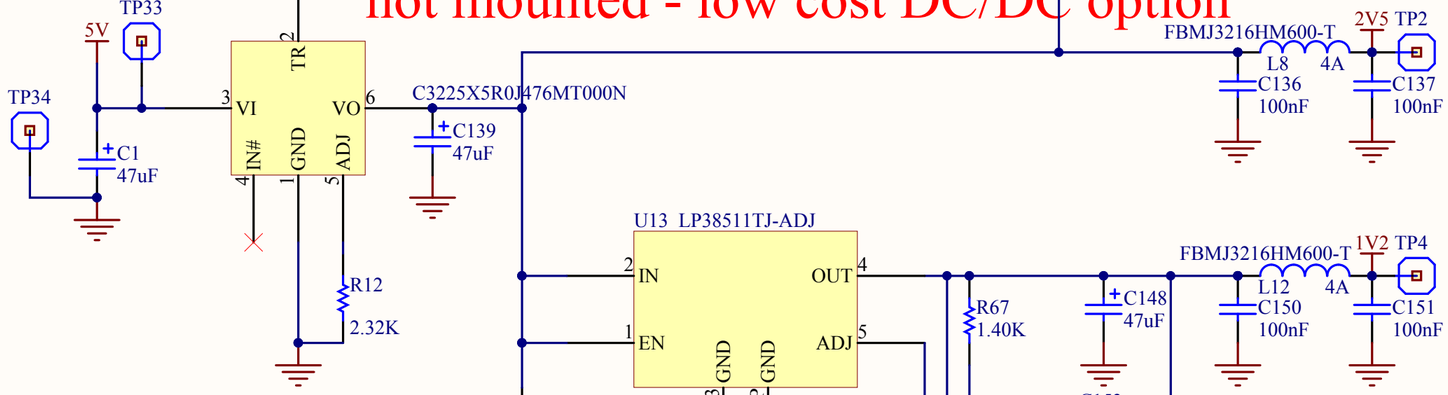
J12~15 are the mechanical mounting holes at each corner of PCB.



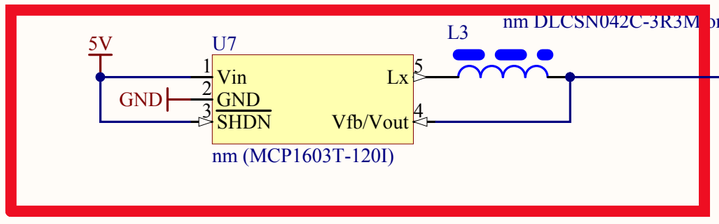


not mounted - low cost DC/DC option

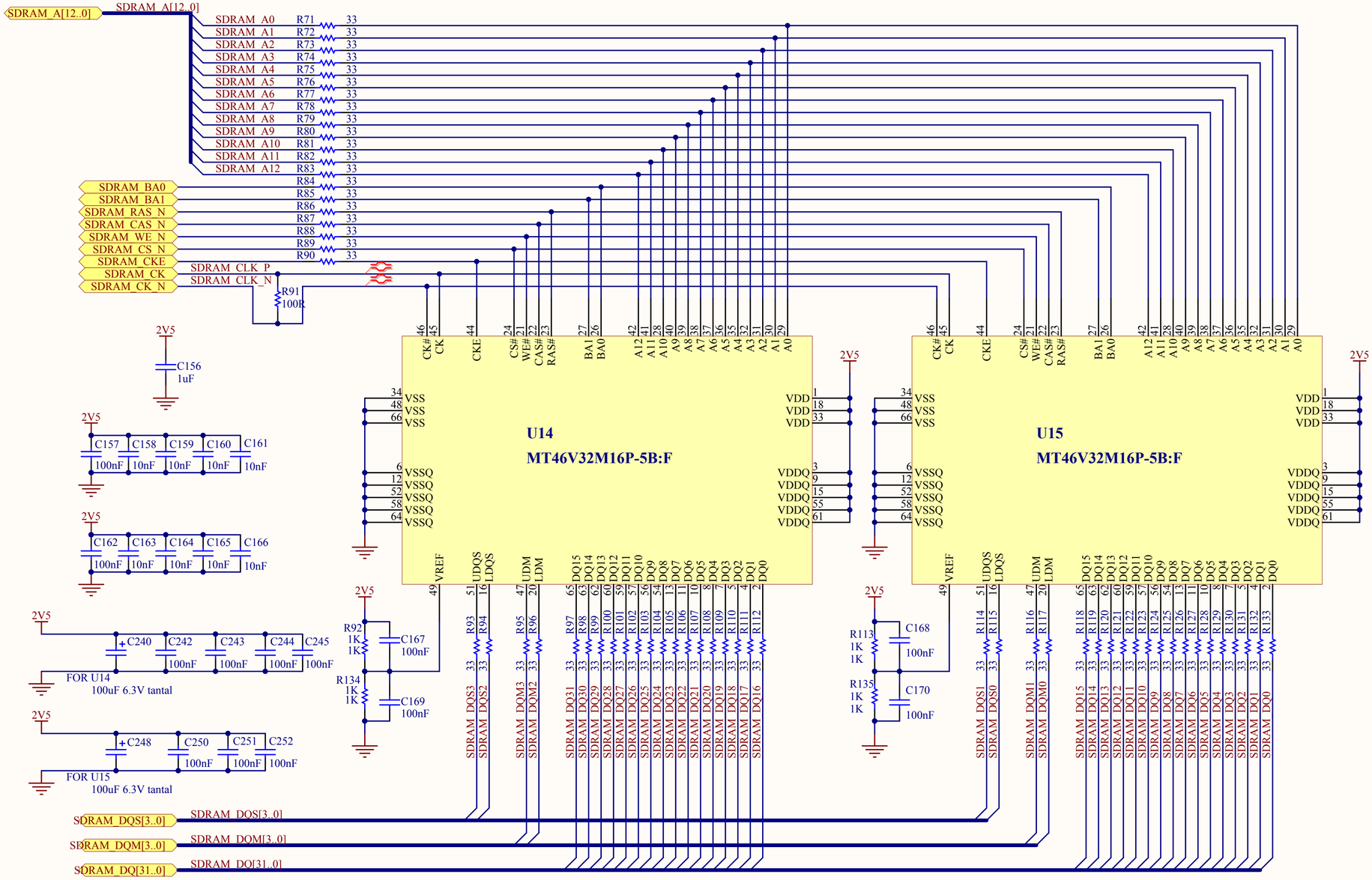




not mounted - low cost DC/DC option



Title: Mixxeo - Power Supply		
Size: A4	Number:	Revision: R4
Date: 2013-08-13		Sheet of
File: C:\Users\..\Power.SchDoc		Drawn By:



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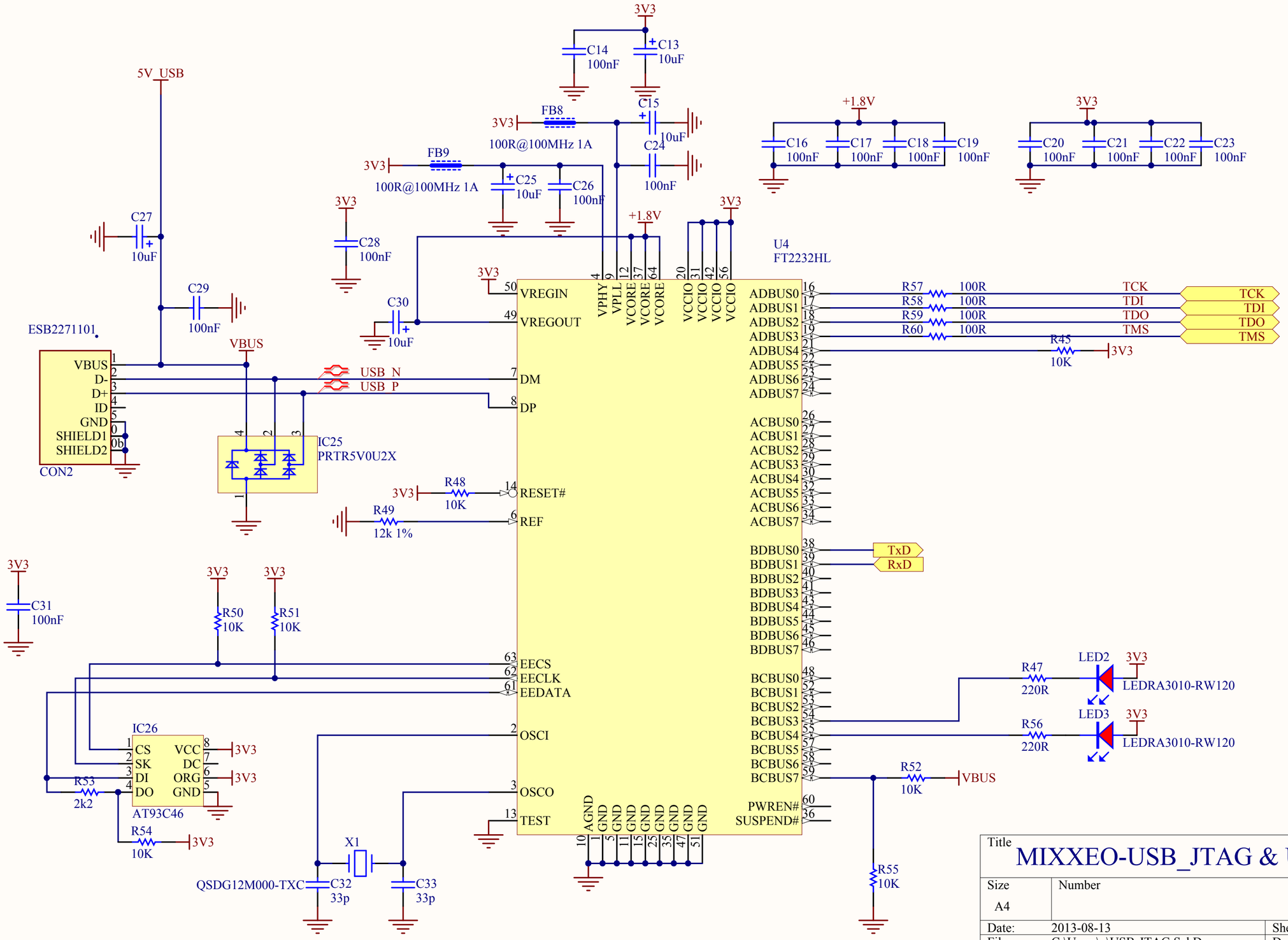
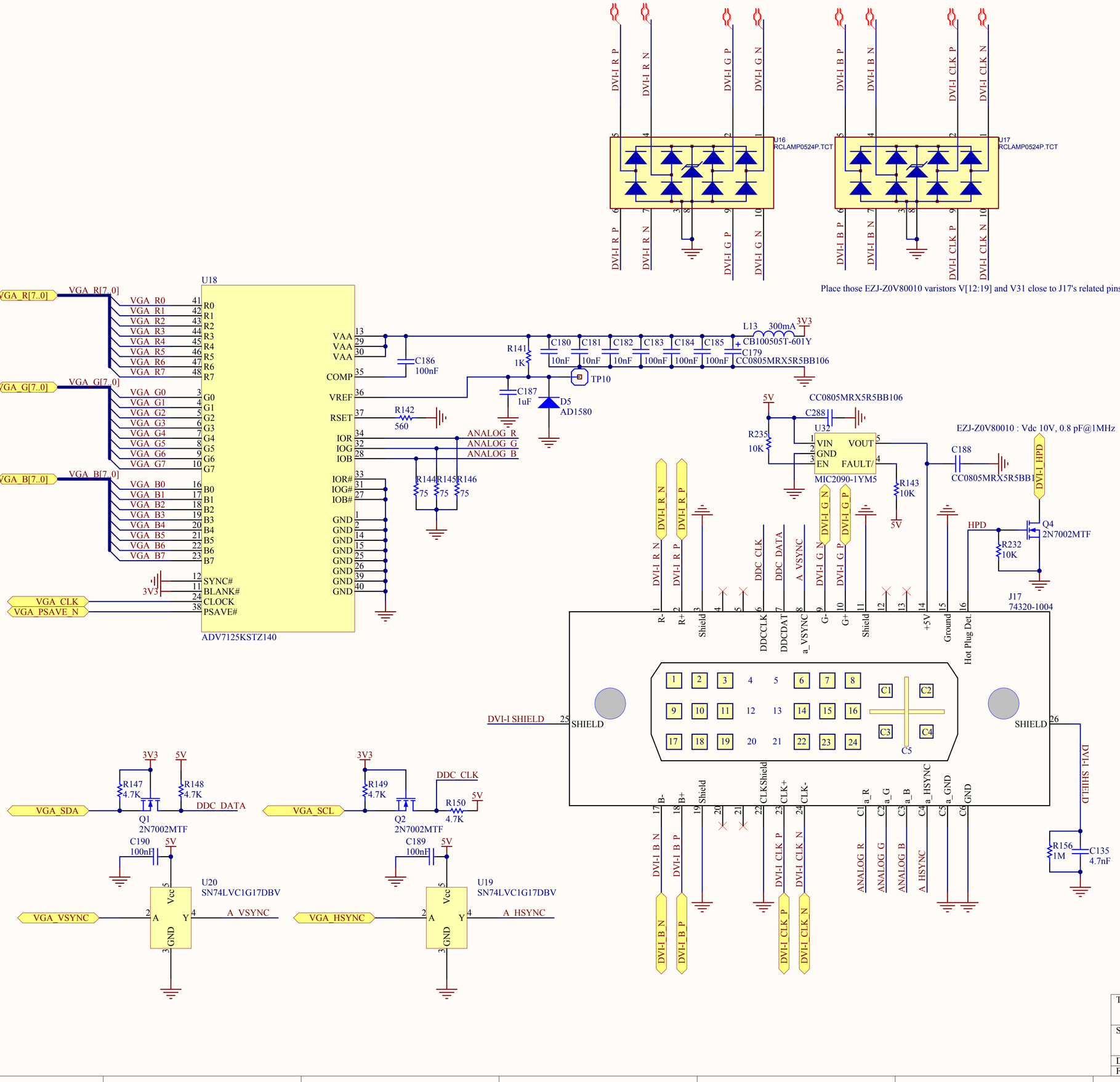
Size: A3	Number	Revision
Date: 2013-08-13		Sheet of
File: C:\Users\..\SDRAM.SchDoc		Drawn By:



Title	MIXXEO-USB_JTAG & UART	
Size: A4	Number	Revision
Date: 2013-08-13		Sheet of
File: C:\Users\..\USB-JTAG.SchDoc		Drawn By:



Title	Mixxeo - DVI-I Single output		
Size A3	Number		Revision
Date: 2013-08-13		Sheet of	
File: C:\Users\..\DVI-ISingle.SchDoc		Drawn By:	