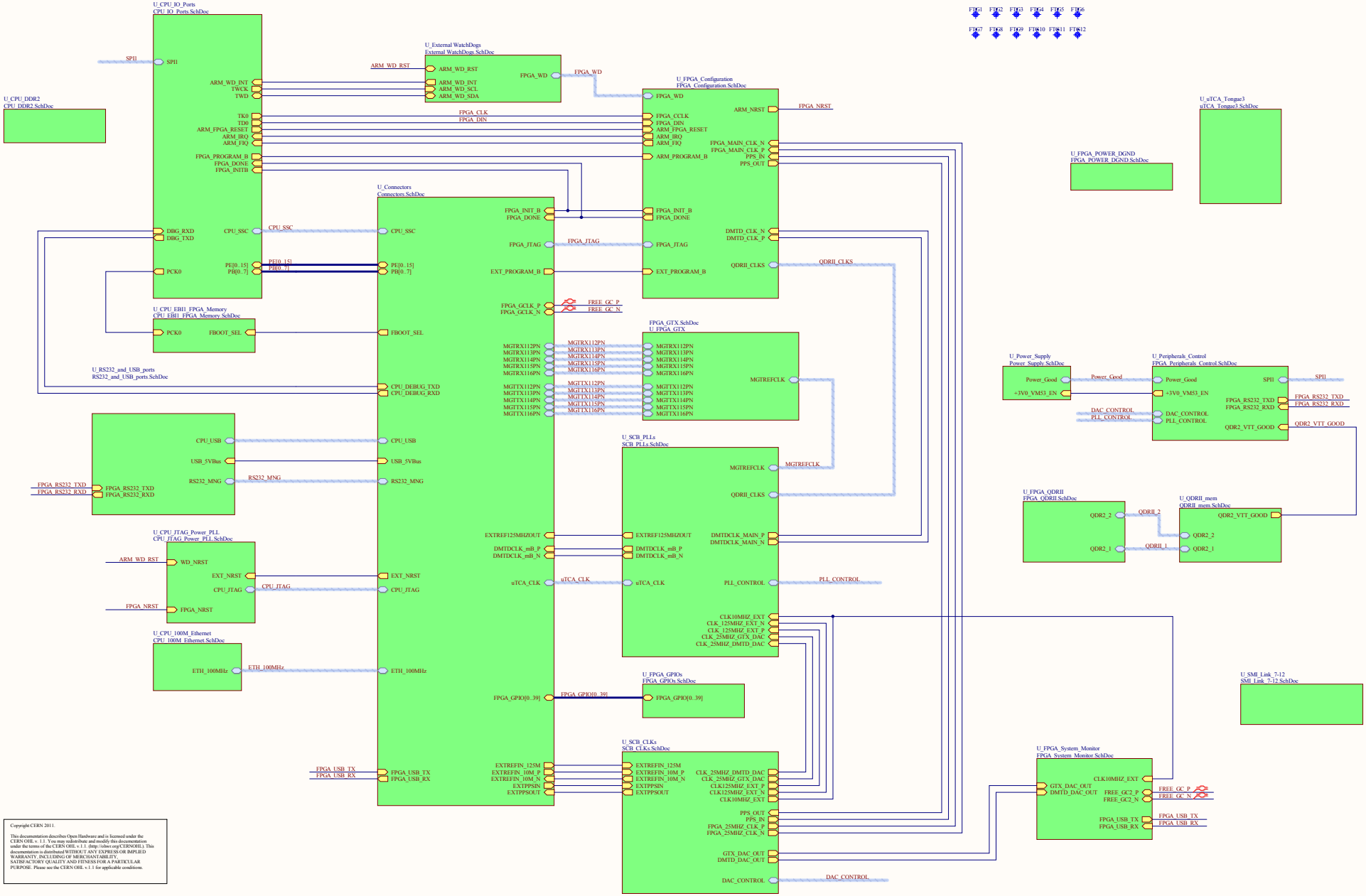
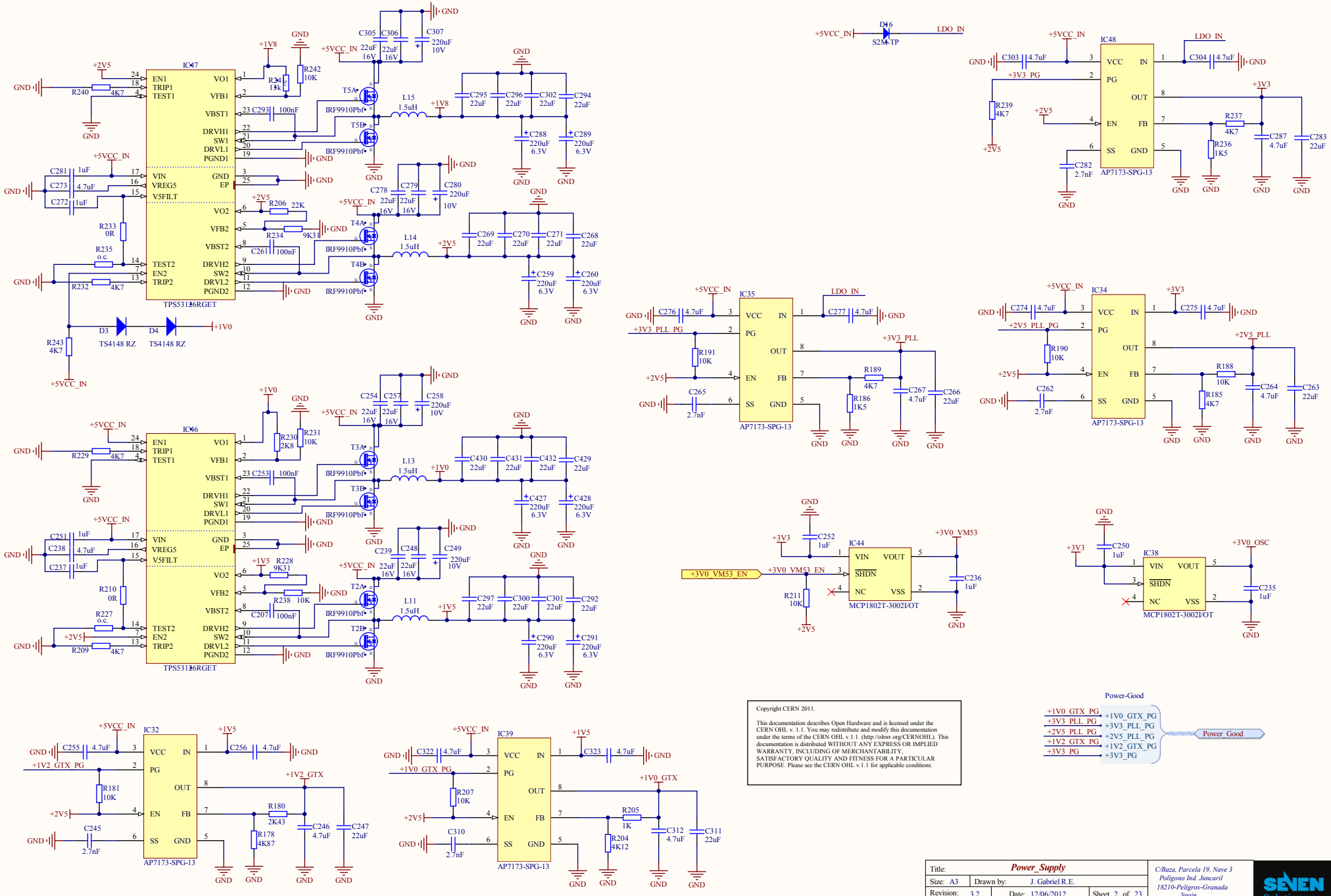


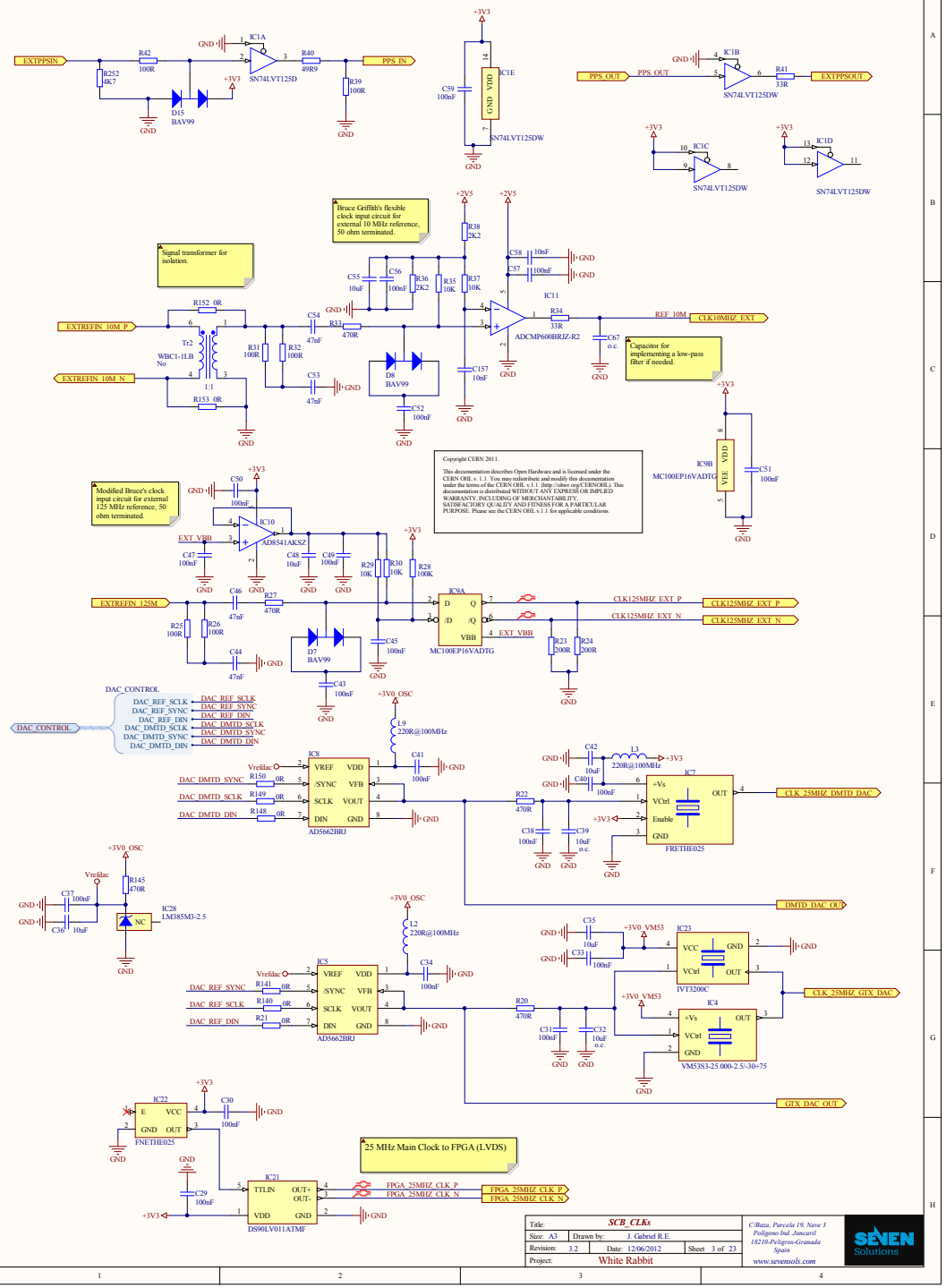
Title:	SCB_MAIN		
Size: A2	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 1 of 23	
Project:	White Rabbit		

C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com



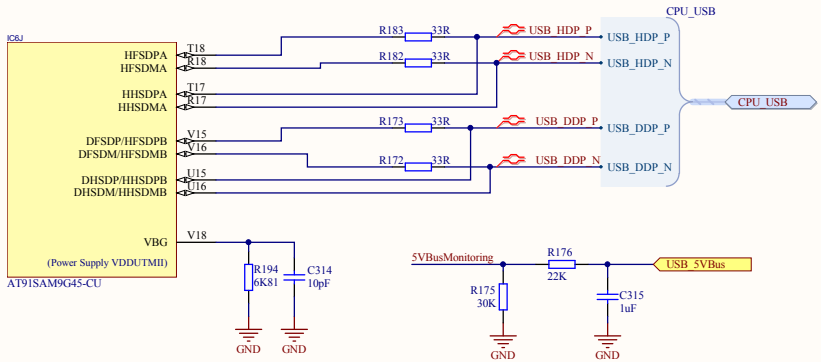
Title:	*Power_Supply*		
Size: A3	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 2 of 23	
Project:	White Rabbit		

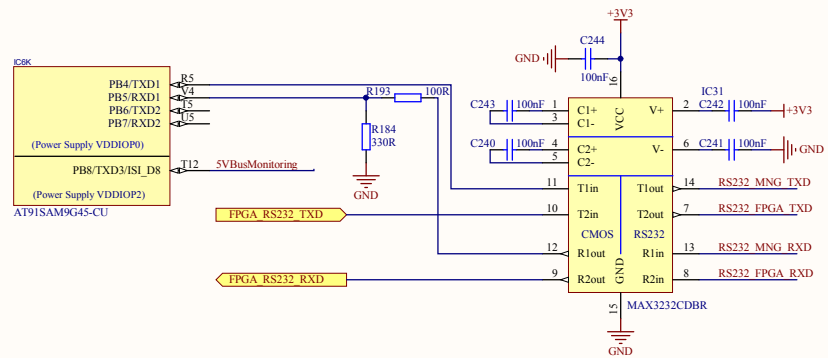
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com



Title:	*SCB_CLKs*		
Size: A3	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 3 of 23	
Project:	White Rabbit		

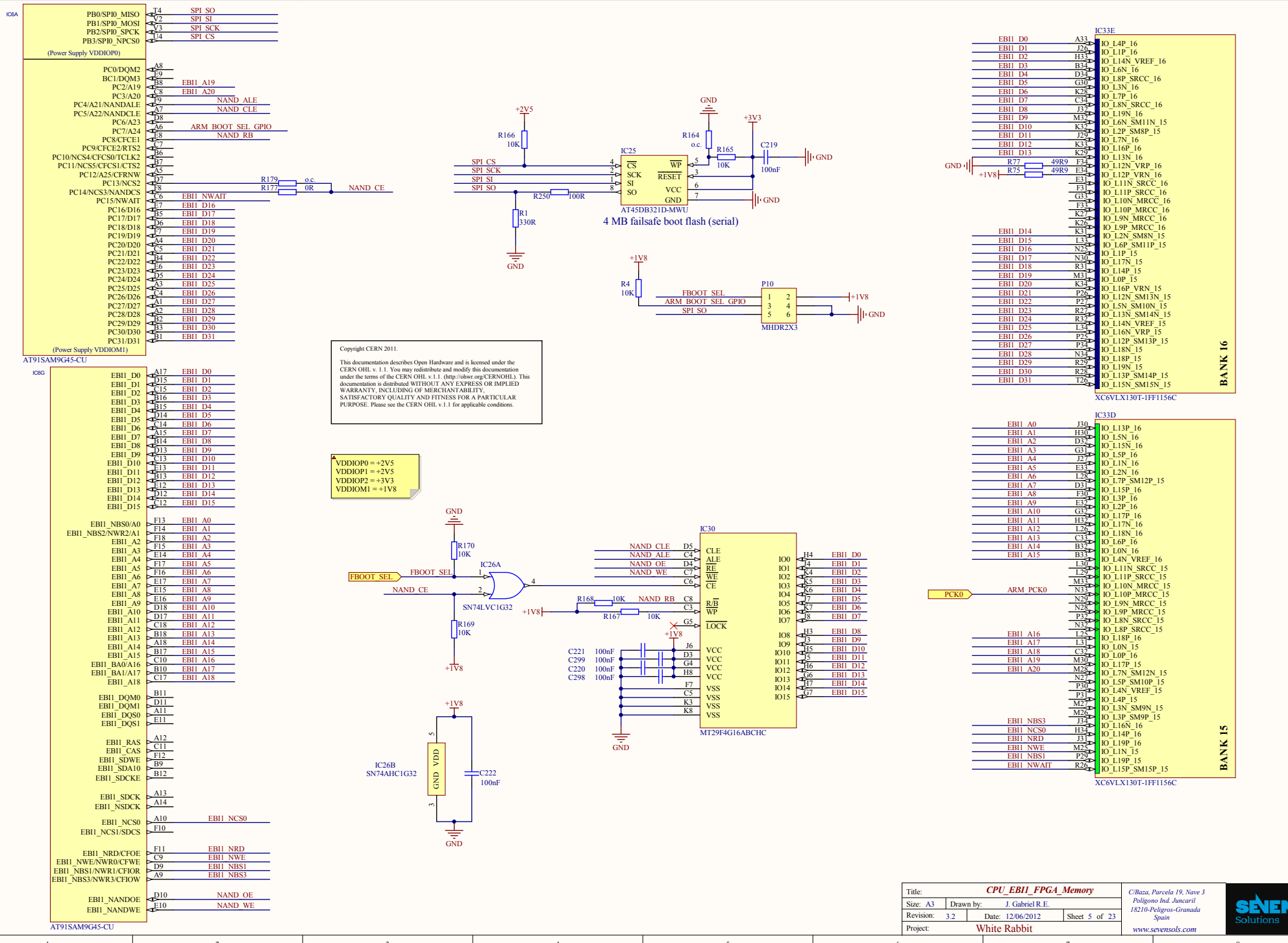
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

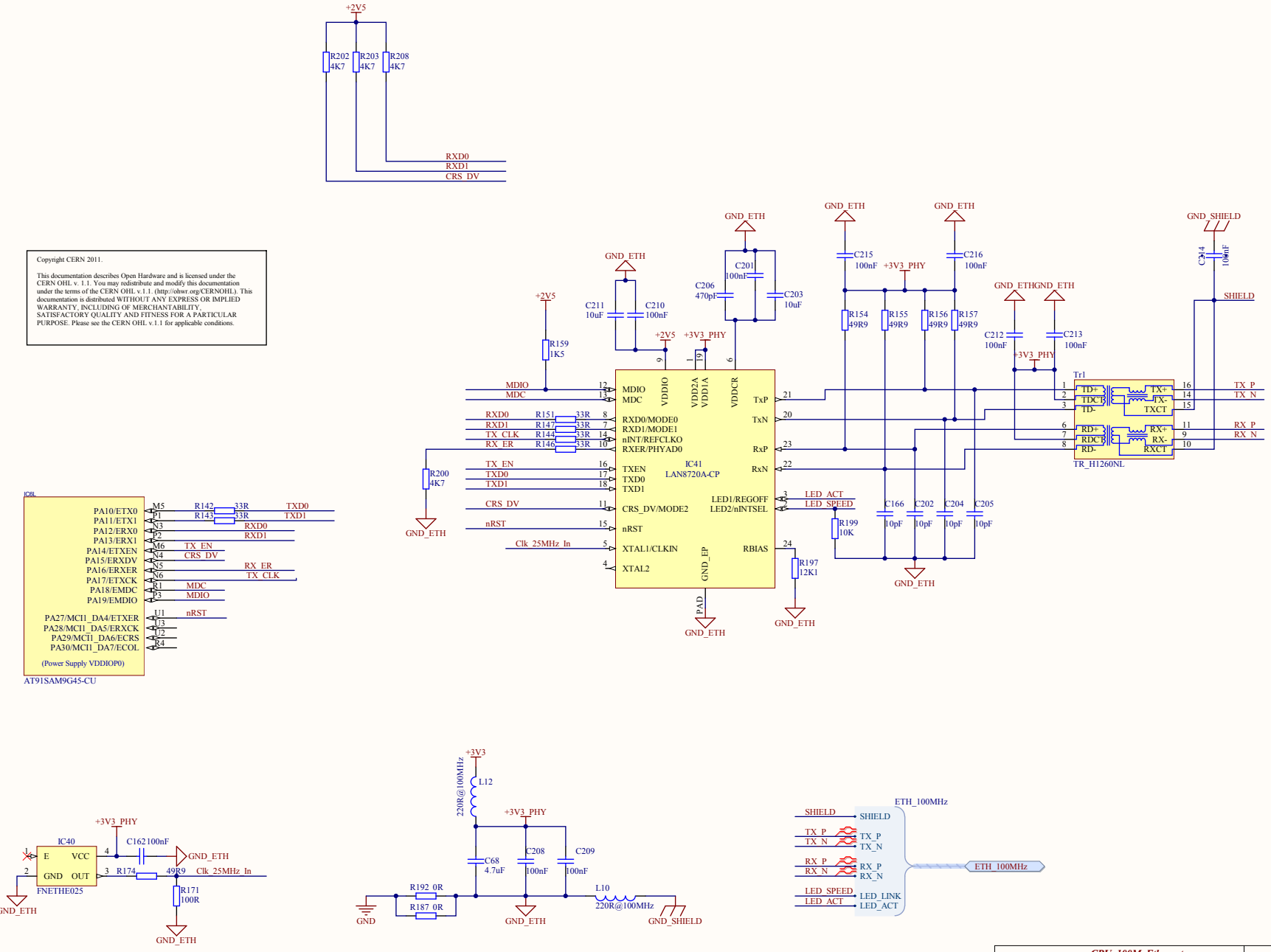




Title:	***RS232_and_USB_ports***		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 4 of 23	
Project:	White Rabbit		

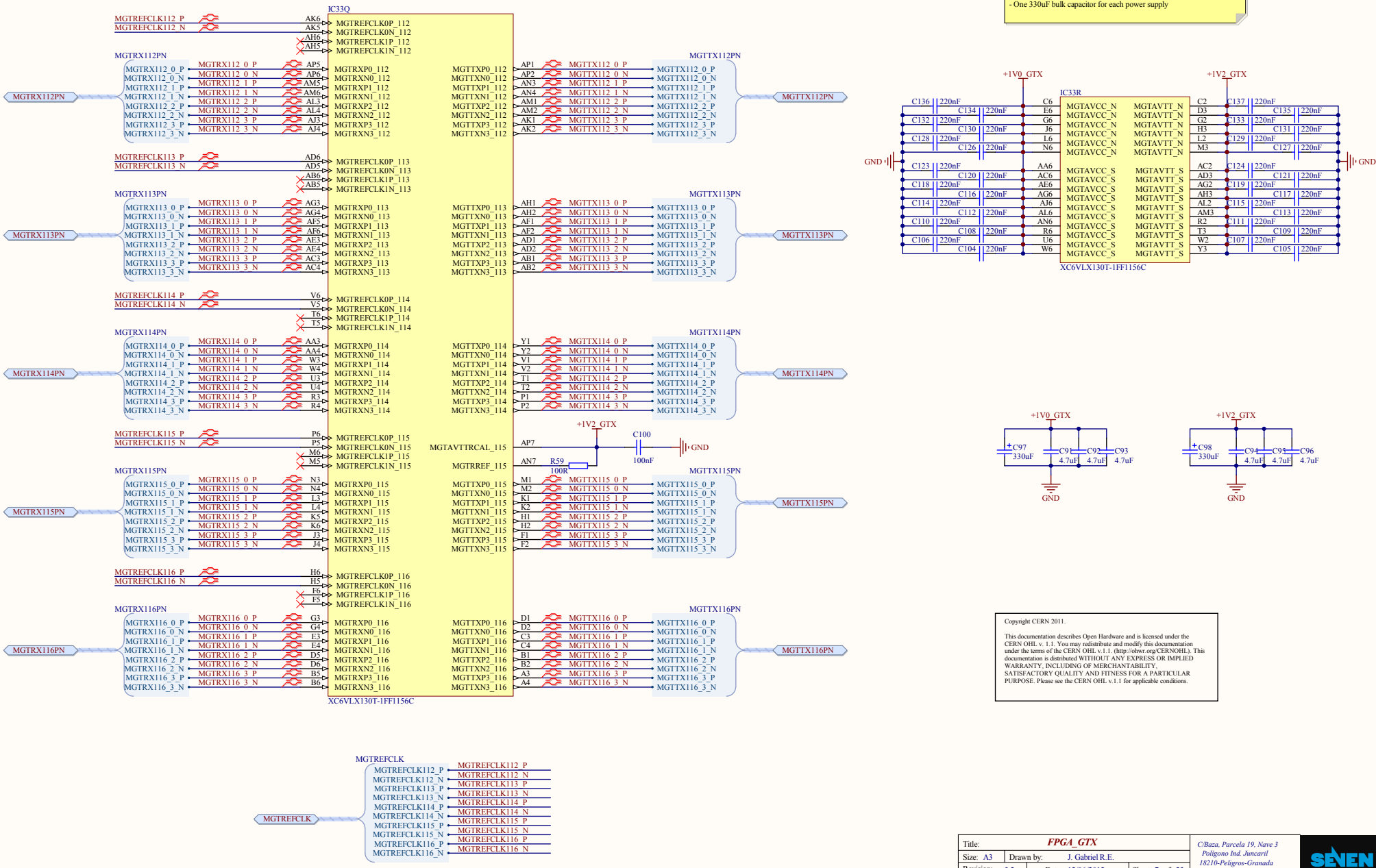
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com


IC6A
PB0/SPI0_MISO
PB1/SPI0_MOSI
PB2/SPI0_SPCK
PB3/SPI0_NPCS0
(Power Supply VDDIOP0)
PC0/DQM2
PC1/DQM3
PC2/A19
PC3/A20
PC4/A21/NANDALE
PC5/A22/NANDCLE
PC6/A23
PC7/A24
PC8/CFCE1
PC9/CFCE2/RTS2
PC10/NCS4/CFCS0/TCLK2
PC11/NCS5/CFCS1/CTS2
PC12/A25/CFRNW
PC13/NCS2
PC14/NCS3/NANDCS
PC15/NWAIT
PC16/D16
PC17/D17
PC18/D18
PC19/D19
PC20/D20
PC21/D21
PC22/D22
PC23/D23
PC24/D24
PC25/D25
PC26/D26
PC27/D27
PC28/D28
PC29/D29
PC30/D30
PC31/D31
(Power Supply VDDIOM1)
AT91SAM9G45-CU
SPI_SO
SPI_SI
SPI_SCK
SPI_CS
EBI1_A19
EBI1_A20
NAND_ALE
NAND_CLE
ARM_BOOT_SEL_GPIO
NAND_RB
R179
R177
0R
o.c.
NAND_CE
EBI1_NWAIT
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
IC6G
EBI1_D0
EBI1_D1
EBI1_D2
EBI1_D3
EBI1_D4
EBI1_D5
EBI1_D6
EBI1_D7
EBI1_D8
EBI1_D9
EBI1_D10
EBI1_D11
EBI1_D12
EBI1_D13
EBI1_D14
EBI1_D15
EBI1_NBS0/A0
EBI1_NBS2/NWR2/A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
EBI1_BA0/A16
EBI1_BA1/A17
EBI1_A18
EBI1_DQM0
EBI1_DQM1
EBI1_DQS0
EBI1_DQS1
EBI1_RAS
EBI1_CAS
EBI1_SDWE
EBI1_SDA10
EBI1_SDCKE
EBI1_SDCK
EBI1_NSDCK
EBI1_NCS0
EBI1_NCS1/SDCS
EBI1_NCS0
EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR
EBI1_NBS3/NWR3/CFIOW
EBI1_NRD
EBI1_NWE
EBI1_NBS1
EBI1_NBS3
EBI1_NANDOE
EBI1_NANDWE
NAND_OE
NAND_WE
AT91SAM9G45-CU
+2V5
R166
10K
SPI_CS
SPI_SCK
SPI_SI
SPI_SO
R250
100R
R1
330R
GND
IC25
CS
SCK
SI
SO
WP
RESET
VCC
GND
AT45DB321D-MWU
4 MB failsafe boot flash (serial)
+3V3
R164
o.c.
R165
10K
C219
100nF
+1V8
R4
10K
FBOOT_SEL
ARM_BOOT_SEL_GPIO
SPI_SO
P10
MHDR2X3
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3
VDDIOM1 = +1V8
R170
10K
IC26A
SN74LVC1G32
R169
10K
R168
10K
R167
10K
NAND_RB
IC30
CLE
ALE
RE
WE
CE
R/B
WP
LOCK
VCC
VSS
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
MT29F4G16ABCHC
C221
C299
C220
C298
100nF
IC26B
SN74AHC1G32
C222
100nF
IC33E
IC33D
BANK 16
BANK 15
XC6VLX130T-1FF1156C
PCK0
ARM_PCK0
R77
R75
49R9
Title: CPU_EBI1_FPGA_Memory
Size: A3
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 5 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions



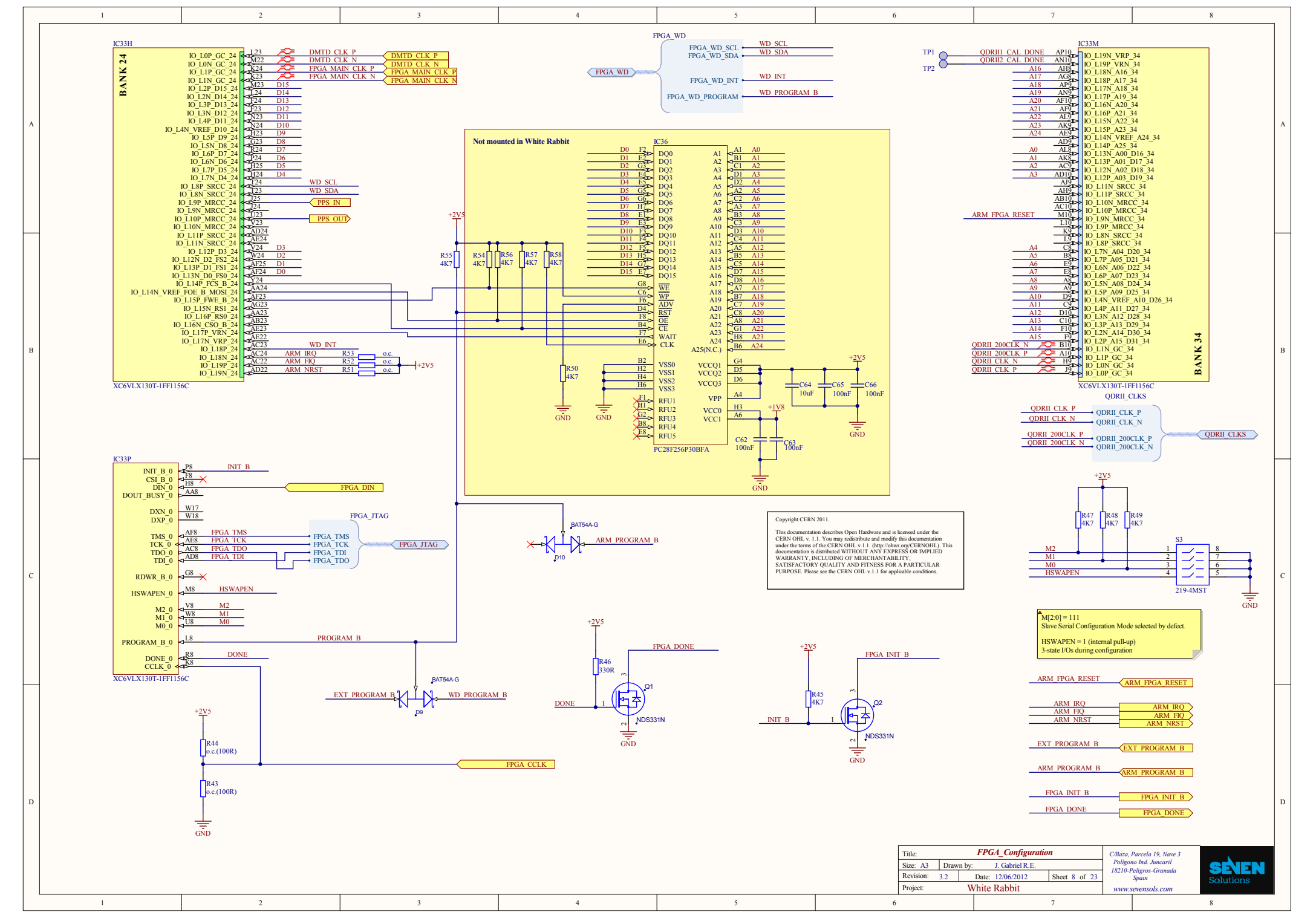
Title:	*CPU_100M_Ethernet*		
Size: A3	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 6 of 23	
Project: White Rabbit			

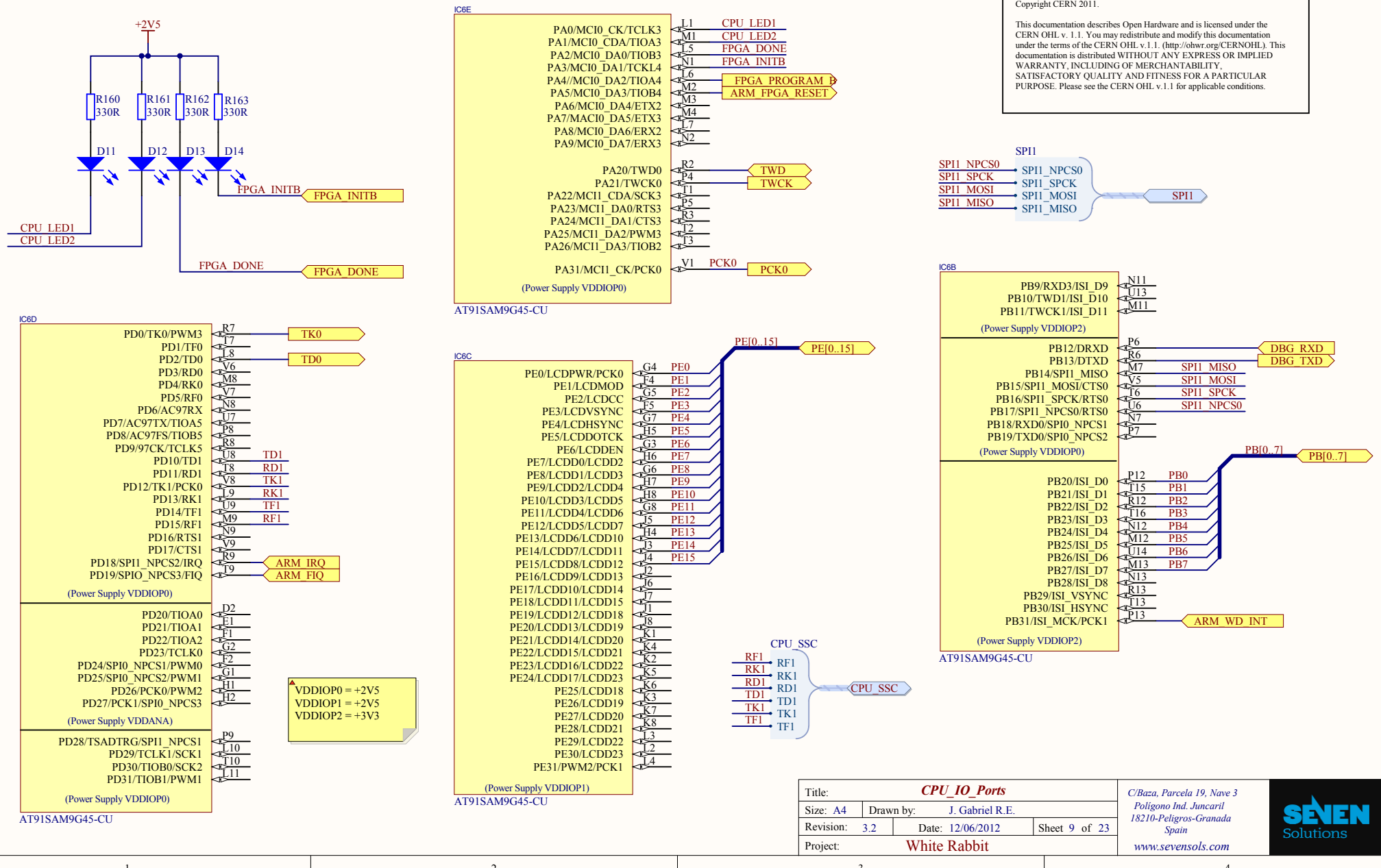
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

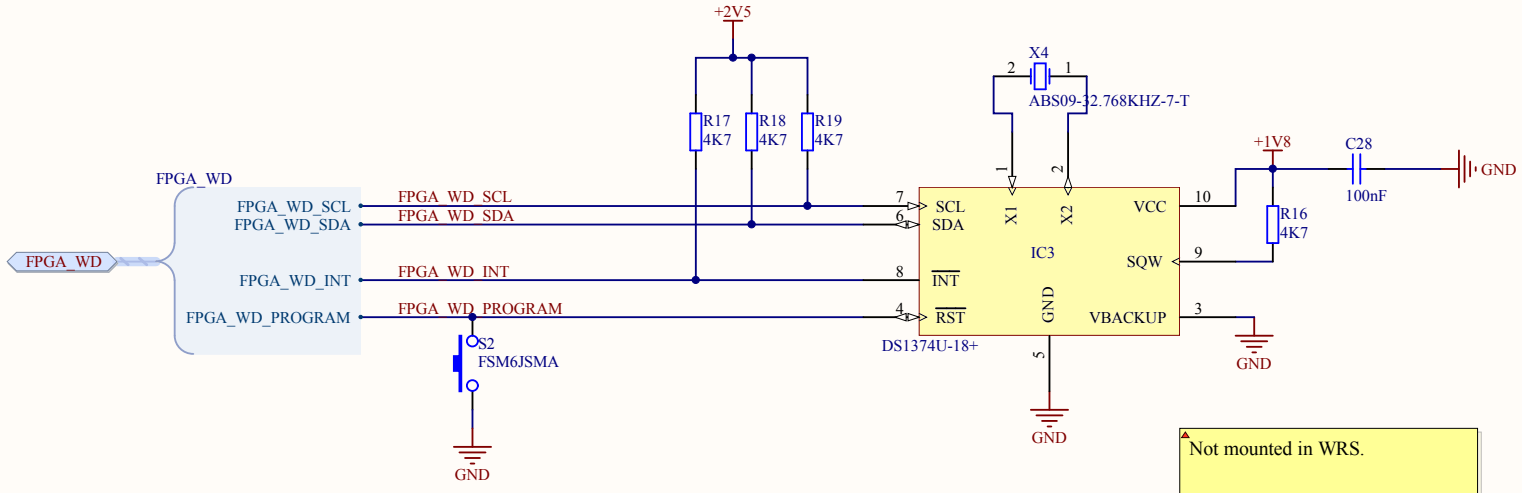


Title:	*FPGA_GTX*		
Size: A3	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 7 of 23	
Project: White Rabbit			

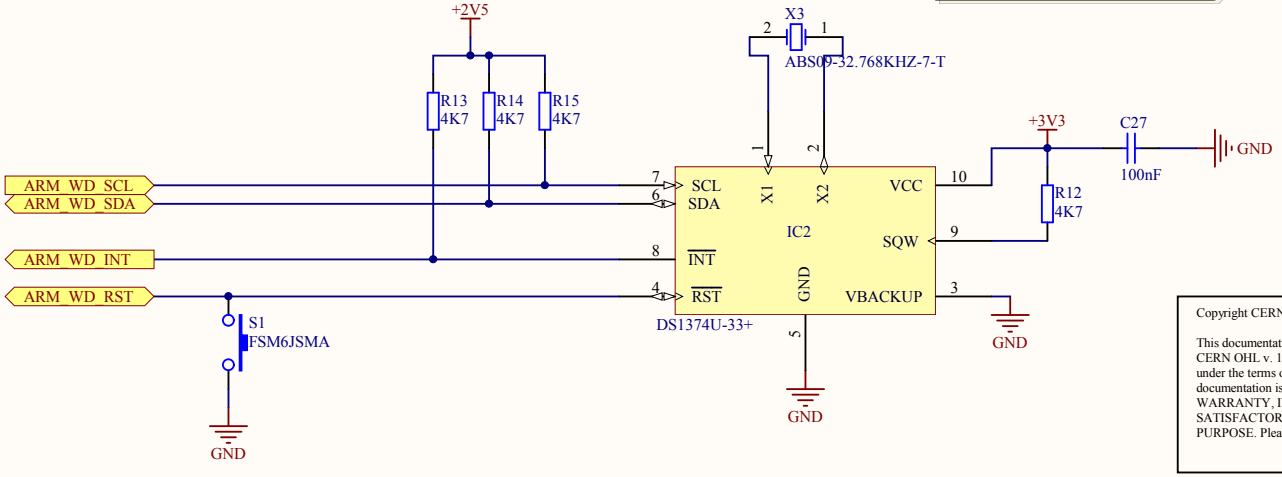
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com


IC33H
BANK 24
XC6VLX130T-1FF1156C
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
WD_INT
ARM_IRQ
ARM_FIQ
ARM_NRST
R53
R52
R51
o.c.
+2V5
FPGA_WD
FPGA_WD_SCL
FPGA_WD_SDA
FPGA_WD_INT
FPGA_WD_PROGRAM
WD_PROGRAM_B
Not mounted in White Rabbit
IC36
PC28F256P30BFA
R55
R54
R56
R57
R58
R50
4K7
GND
C64
C65
C66
C62
C63
10uF
100nF
+1V8
IC33M
BANK 34
XC6VLX130T-1FF1156C
TP1
TP2
QDRII1_CAL_DONE
QDRII2_CAL_DONE
ARM_FPGA_RESET
QDRII_200CLK_N
QDRII_200CLK_P
QDRII_CLK_N
QDRII_CLK_P
QDRII_CLKS
IC33P
INIT_B_0
CSI_B_0
DIN_0
DOUT_BUSY_0
DXN_0
DXP_0
TMS_0
TCK_0
TDO_0
TDI_0
RDWR_B_0
HSWAPEN_0
M2_0
M1_0
M0_0
PROGRAM_B_0
DONE_0
CCLK_0
INIT_B
FPGA_DIN
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
HSWAPEN
M2
M1
M0
PROGRAM_B
DONE
BAT54A-G
D10
ARM_PROGRAM_B
D9
EXT_PROGRAM_B
WD_PROGRAM_B
R44
o.c.(100R)
R43
o.c.(100R)
FPGA_CCLK
R46
330R
Q1
NDS331N
FPGA_DONE
R45
4K7
Q2
FPGA_INIT_B
R47
R48
R49
S3
219-4MST
M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Title: FPGA_Configuration
Size: A3
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 8 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions


+2V5
R160 330R
R161 330R
R162 330R
R163 330R
D11
D12
D13
D14
FPGA_INITB
FPGA_INITB
CPU_LED1
CPU_LED2
FPGA_DONE
FPGA_DONE
IC6E
PA0/MCI0_CK/TCLK3
PA1/MCI0_CDA/TIOA3
PA2/MCI0_DA0/TIOB3
PA3/MCI0_DA1/TCKL4
PA4//MCI0_DA2/TIOA4
PA5/MCI0_DA3/TIOB4
PA6/MCI0_DA4/ETX2
PA7/MACI0_DA5/ETX3
PA8/MCI0_DA6/ERX2
PA9/MCI0_DA7/ERX3
PA20/TWD0
PA21/TWCK0
PA22/MCI1_CDA/SCK3
PA23/MCI1_DA0/RTS3
PA24/MCI1_DA1/CTS3
PA25/MCI1_DA2/PWM3
PA26/MCI1_DA3/TIOB2
PA31/MCI1_CK/PCK0
(Power Supply VDDIOP0)
L1 CPU_LED1
M1 CPU_LED2
L5 FPGA_DONE
N1 FPGA_INITB
L6
M2 FPGA_PROGRAM_B
M3 ARM_FPGA_RESET
M4
L7
N2
R2 TWD
P4 TWCK
T1
P5
R3
T2
T3
V1 PCK0
PCK0
AT91SAM9G45-CU
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
SPI1
SPI1_NPCS0
SPI1_SPCK
SPI1_MOSI
SPI1_MISO
SPI1
IC6D
PD0/TK0/PWM3
PD1/TF0
PD2/TD0
PD3/RD0
PD4/RK0
PD5/RF0
PD6/AC97RX
PD7/AC97TX/TIOA5
PD8/AC97FS/TIOB5
PD9/97CK/TCLK5
PD10/TD1
PD11/RD1
PD12/TK1/PCK0
PD13/RK1
PD14/TF1
PD15/RF1
PD16/RTS1
PD17/CTS1
PD18/SPI1_NPCS2/IRQ
PD19/SPIO_NPCS3/FIQ
(Power Supply VDDIOP0)
R7
T7
L8 TK0
V6 TD0
M8
V7
N8
U7
P8
R8
U8 TD1
T8 RD1
V8 TK1
J9 RK1
U9 TF1
M9 RF1
N9
V9
R9 ARM_IRQ
J9 ARM_FIQ
PD20/TIOA0
PD21/TIOA1
PD22/TIOA2
PD23/TCLK0
PD24/SPI0_NPCS1/PWM0
PD25/SPI0_NPCS2/PWM1
PD26/PCK0/PWM2
PD27/PCK1/SPI0_NPCS3
(Power Supply VDDANA)
D2
E1
F1
G2
F2
G1
H1
H2
VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3
PD28/TSADTRG/SPI1_NPCS1
PD29/TCLK1/SCK1
PD30/TIOB0/SCK2
PD31/TIOB1/PWM1
(Power Supply VDDIOP0)
P9
L10
T10
L11
AT91SAM9G45-CU
IC6C
PE0/LCDPWR/PCK0
PE1/LCDMOD
PE2/LCDCC
PE3/LCDVSYNC
PE4/LCDHSYNC
PE5/LCDDOTCK
PE6/LCDDEN
PE7/LCDD0/LCDD2
PE8/LCDD1/LCDD3
PE9/LCDD2/LCDD4
PE10/LCDD3/LCDD5
PE11/LCDD4/LCDD6
PE12/LCDD5/LCDD7
PE13/LCDD6/LCDD10
PE14/LCDD7/LCDD11
PE15/LCDD8/LCDD12
PE16/LCDD9/LCDD13
PE17/LCDD10/LCDD14
PE18/LCDD11/LCDD15
PE19/LCDD12/LCDD18
PE20/LCDD13/LCDD19
PE21/LCDD14/LCDD20
PE22/LCDD15/LCDD21
PE23/LCDD16/LCDD22
PE24/LCDD17/LCDD23
PE25/LCDD18
PE26/LCDD19
PE27/LCDD20
PE28/LCDD21
PE29/LCDD22
PE30/LCDD23
PE31/PWM2/PCK1
(Power Supply VDDIOP1)
G4 PE0
F4 PE1
G5 PE2
F5 PE3
G7 PE4
H5 PE5
G3 PE6
H6 PE7
G6 PE8
H7 PE9
H8 PE10
G8 PE11
J5 PE12
H4 PE13
J3 PE14
J4 PE15
J2
J6
J7
J1
J8
K1
K4
K2
K5
K6
K3
K7
K8
L3
L2
L4
PE[0..15]
PE[0..15]
AT91SAM9G45-CU
CPU_SSC
RF1
RK1
RD1
TD1
TK1
TF1
CPU_SSC
IC6B
PB9/RXD3/ISI_D9
PB10/TWD1/ISI_D10
PB11/TWCK1/ISI_D11
(Power Supply VDDIOP2)
N11
J13
M11
PB12/DRXD
PB13/DTXD
PB14/SPI1_MISO
PB15/SPI1_MOSI/CTS0
PB16/SPI1_SPCK/RTS0
PB17/SPI1_NPCS0/RTS0
PB18/RXD0/SPI0_NPCS1
PB19/TXD0/SPI0_NPCS2
(Power Supply VDDIOP0)
P6 DBG_RXD
R6 DBG_TXD
M7 SPI1_MISO
V5 SPI1_MOSI
T6 SPI1_SPCK
J6 SPI1_NPCS0
N7
P7
PB20/ISI_D0
PB21/ISI_D1
PB22/ISI_D2
PB23/ISI_D3
PB24/ISI_D4
PB25/ISI_D5
PB26/ISI_D6
PB27/ISI_D7
PB28/ISI_D8
PB29/ISI_VSYNC
PB30/ISI_HSYNC
PB31/ISI_MCK/PCK1
(Power Supply VDDIOP2)
P12 PB0
T15 PB1
R12 PB2
T16 PB3
N12 PB4
M12 PB5
J14 PB6
M13 PB7
N13
R13
T13
P13 ARM_WD_INT
PB[0..7]
PB[0..7]
AT91SAM9G45-CU
Title: CPU_IO_Ports
Size: A4
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 9 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions



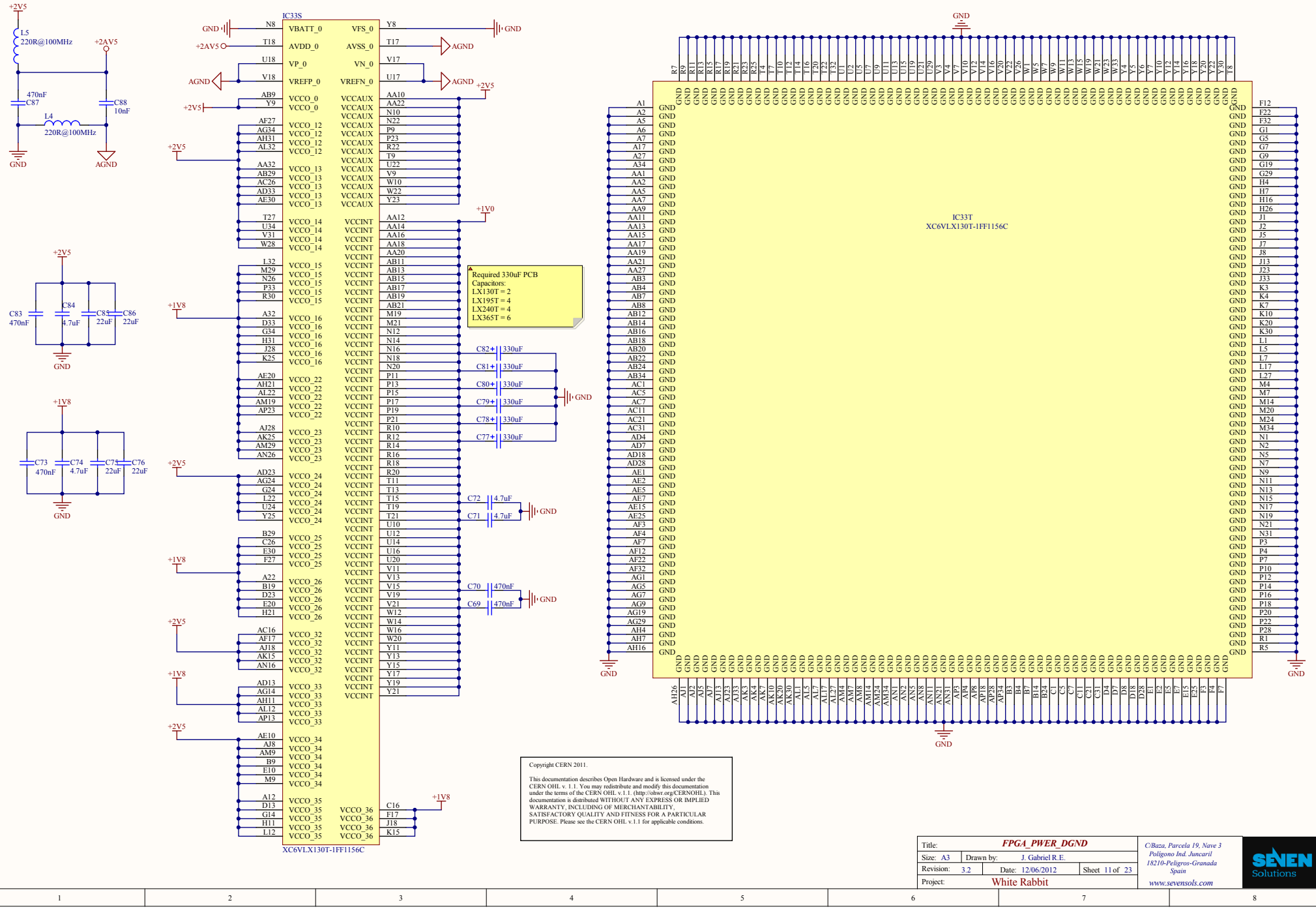
Not mounted in WRS.

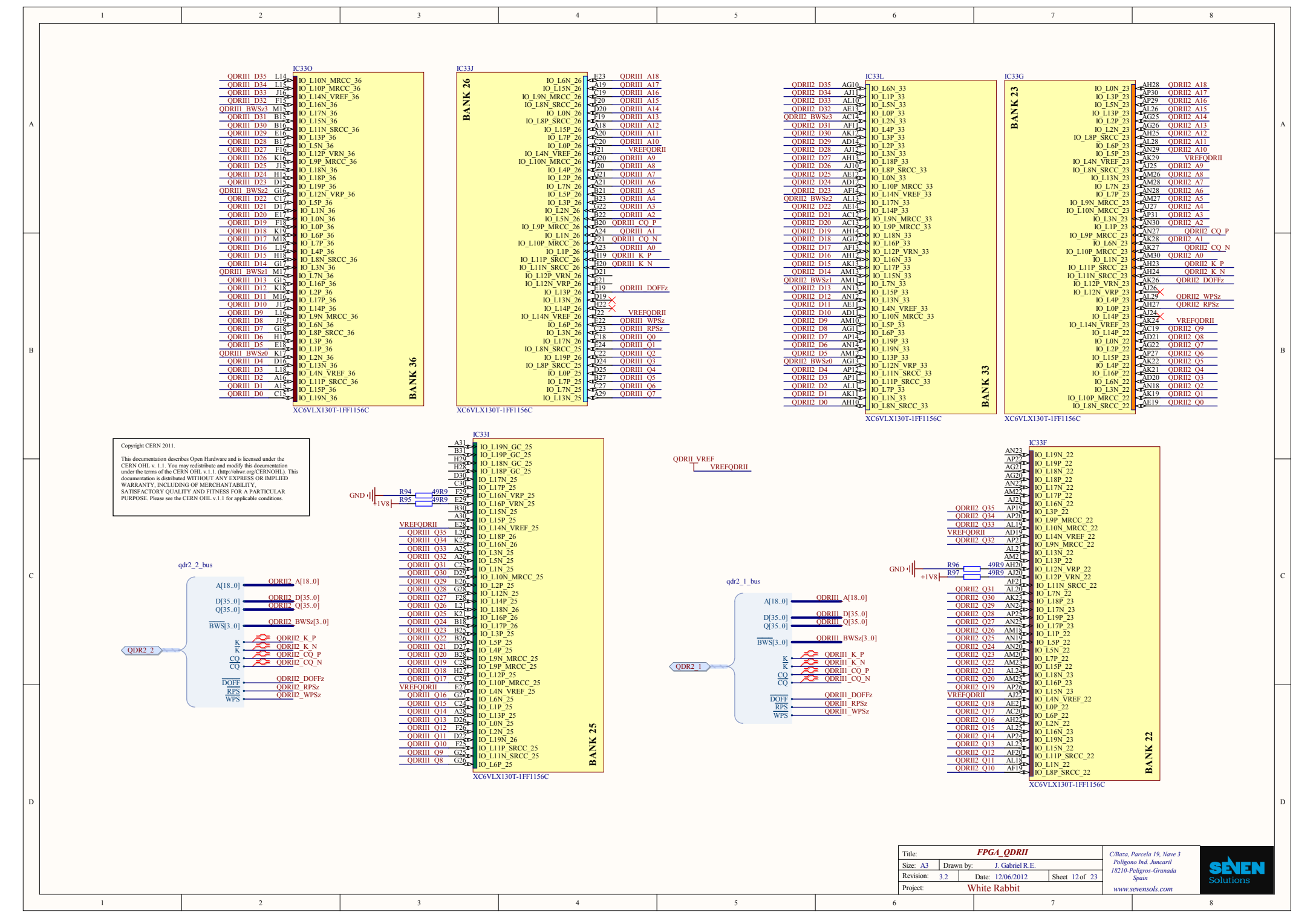


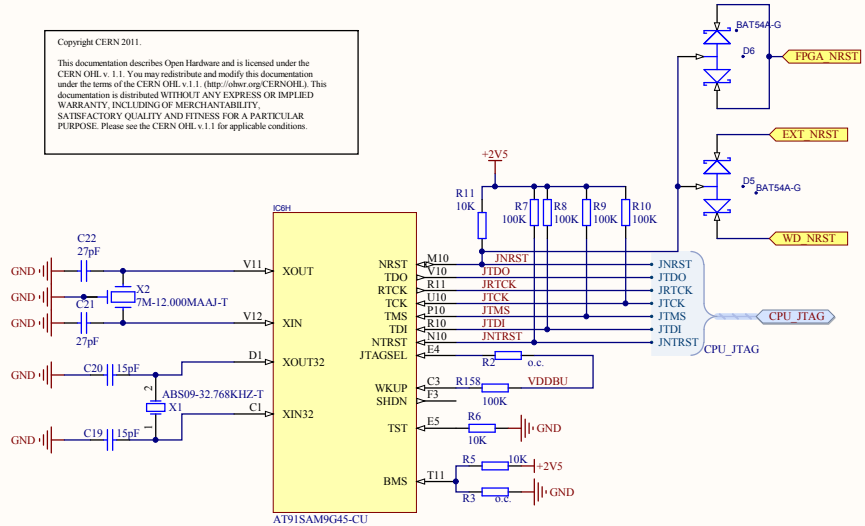
Title:	*ExternalWatchDogs*		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 10 of 23	
Project:	White Rabbit		

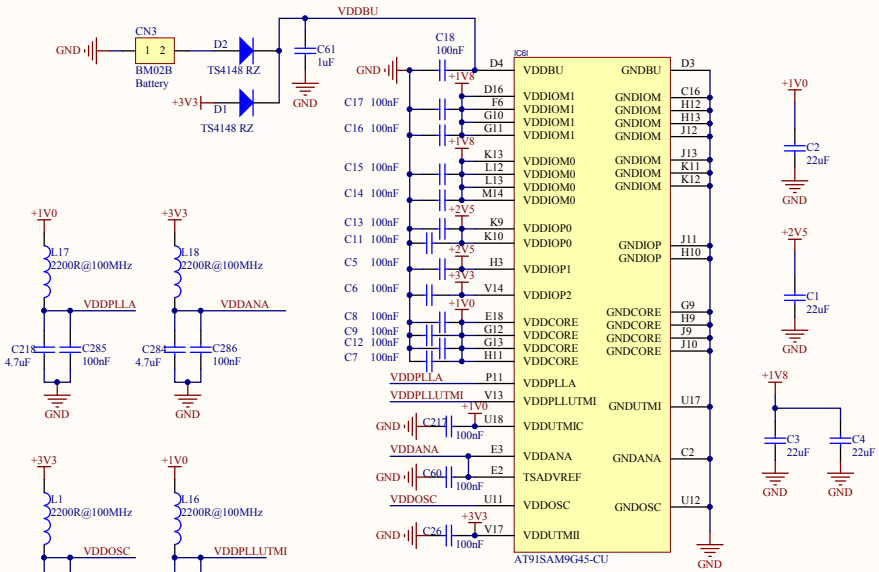
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

SEVEN Solutions


+2V5
L5
220R@100MHz
+2AV5
470nF
C87
C88
10nF
L4
220R@100MHz
GND
AGND
IC33S
VBATT_0
VFS_0
AVDD_0
AVSS_0
VP_0
VN_0
VREFP_0
VREFN_0
VCCO_0
VCCAUX
VCCO_12
VCCO_13
VCCO_14
VCCO_15
VCCO_16
VCCO_22
VCCO_23
VCCO_24
VCCO_25
VCCO_26
VCCO_32
VCCO_33
VCCO_34
VCCO_35
VCCO_36
VCCINT
XC6VLX130T-1FF1156C
+1V0
+1V8
C83
470nF
C84
4.7uF
C85
22uF
C86
22uF
C73
470nF
C74
4.7uF
C75
22uF
C76
22uF
Required 330uF PCB
Capacitors:
LX130T = 2
LX195T = 4
LX240T = 4
LX365T = 6
C82
C81
C80
C79
C78
C77
330uF
C72
C71
4.7uF
C70
C69
470nF
C16
F17
J18
K15
IC33T
XC6VLX130T-1FF1156C
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Title: FPGA_PWER_DGND
Size: A3
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 11 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions


IC33O
BANK 36
XC6VLX130T-1FF1156C
IC33J
BANK 26
XC6VLX130T-1FF1156C
IC33L
BANK 33
XC6VLX130T-1FF1156C
IC33G
BANK 23
XC6VLX130T-1FF1156C
IC33I
BANK 25
XC6VLX130T-1FF1156C
IC33F
BANK 22
XC6VLX130T-1FF1156C
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL) This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
qdr2_2_bus
QDR2_2
qdr2_1_bus
QDR2_1
GND
+1V8
R94
R95
R96
R97
49R9
VREFQDRII
QDRII_VREF
Title: FPGA_QDRII
Size: A3
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 12 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions





Title:	*CPU_JTAG_Power_PLL*		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 13 of 23	
Project:	White Rabbit		

C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

SEVEN Solutions

SMI links 1-6 -> fabric E

CN4C

77	TxFE-6+	RxFE-6+	94
78	TxFE-6-	RxFE-6-	93
65	TxFE-5+	RxFE-5+	106
66	TxFE-5-	RxFE-5-	105
53	TxFE-4+	RxFE-4+	118
54	TxFE-4-	RxFE-4-	117
41	TxFE-3+	RxFE-3+	130
42	TxFE-3-	RxFE-3-	129
29	TxFE-2+	RxFE-2+	142
30	TxFE-2-	RxFE-2-	141
17	TxFE-1+	RxFE-1+	154
18	TxFE-1-	RxFE-1-	153

UTCA_MCH_TONGUE3

SMI links 1-6 -> fabric D

CN4A

TxFD6_P	74	TxFD-6+	RxFD-6+	97	RxFD6_P
TxFD6_N	75	TxFD-6-	RxFD-6-	96	RxFD6_N
TxFD5_P	62	TxFD-5+	RxFD-5+	109	RxFD5_P
TxFD5_N	63	TxFD-5-	RxFD-5-	108	RxFD5_N
TxFD4_P	50	TxFD-4+	RxFD-4+	121	RxFD4_P
TxFD4_N	51	TxFD-4-	RxFD-4-	120	RxFD4_N
TxFD3_P	38	TxFD-3+	RxFD-3+	133	RxFD3_P
TxFD3_N	39	TxFD-3-	RxFD-3-	132	RxFD3_N
TxFD2_P	26	TxFD-2+	RxFD-2+	145	RxFD2_P
TxFD2_N	27	TxFD-2-	RxFD-2-	144	RxFD2_N
TxFD1_P	14	TxFD-1+	RxFD-1+	157	RxFD1_P
TxFD1_N	15	TxFD-1-	RxFD-1-	156	RxFD1_N

UTCA_MCH_TONGUE3

IC33C

BANK 14

IO_L18P_14	W25	TxFD6_P	
IO_L18N_14	Y25	TxFD6_N	
IO_L19P_14	W27	TxFD5_P	
IO_L19N_14	W26	TxFD5_N	
IO_L15P_14	W29	TxFD4_P	
IO_L15N_14	Y29	TxFD4_N	
IO_L5P_14	U26	TxFD3_P	
IO_L5N_14	U27	TxFD3_N	
IO_L1P_14	U28	TxFD2_P	
IO_L1N_14	V29	TxFD2_N	
IO_L4P_14	T33	TxFD1_P	
IO_L4N_VREF_14	T34	TxFD1_N	
IO_L6P_14	U33		
IO_L6N_14	U32		
IO_L7P_14	U28		
IO_L7N_14	V29		
IO_L8P_SRCC_14	T31		
IO_L8N_SRCC_14	T30		
IO_L9P_MRCC_14	Y30		
IO_L9N_MRCC_14	W30		
IO_L10P_MRCC_14	Y34		
IO_L10N_MRCC_14	W34		
IO_L11P_SRCC_14	V28		
IO_L11N_SRCC_14	Y27		
IO_L12P_VRN_14	V32		
IO_L12N_VRP_14	Y33		
IO_L13P_14	Y32		
IO_L13N_14	Y31		
IO_L0P_14	U25	RxFD6_P	
IO_L0N_14	T25	RxFD6_N	
IO_L17P_14	T28	RxFD5_P	
IO_L17N_14	Y27	RxFD5_N	
IO_L14P_14	Y33	RxFD4_P	
IO_L14N_VREF_14	Y34	RxFD4_N	
IO_L16P_14	W31	RxFD3_P	
IO_L16N_14	W32	RxFD3_N	
IO_L3P_14	T30	RxFD2_P	
IO_L3N_14	T31	RxFD2_N	
IO_L2P_14	R33	RxFD1_P	
IO_L2N_14	R34	RxFD1_N	

XC6VLX130T-1FF1156C

CN4B

2	RSVD	GND	86
3	RSVD	GND	89
5	RSVD	GND	92
6	RSVD	GND	95
169	RSVD	GND	98
168	RSVD	GND	10
166	RSVD	GND	10
165	RSVD	GND	10
		GND	11
1	GND	GND	11
4	GND	GND	11
7	GND	GND	11
10	GND	GND	12
13	GND	GND	12
16	GND	GND	12
19	GND	GND	13
22	GND	GND	13
25	GND	GND	13
28	GND	GND	14
31	GND	GND	14
34	GND	GND	14
37	GND	GND	14
40	GND	GND	15
43	GND	GND	15
46	GND	GND	15
49	GND	GND	16
52	GND	GND	16
55	GND	GND	16
58	GND	GND	17
61	GND	GND	85
64	GND	GND	82
67	GND	GND	79
70	GND	GND	76
73	GND		

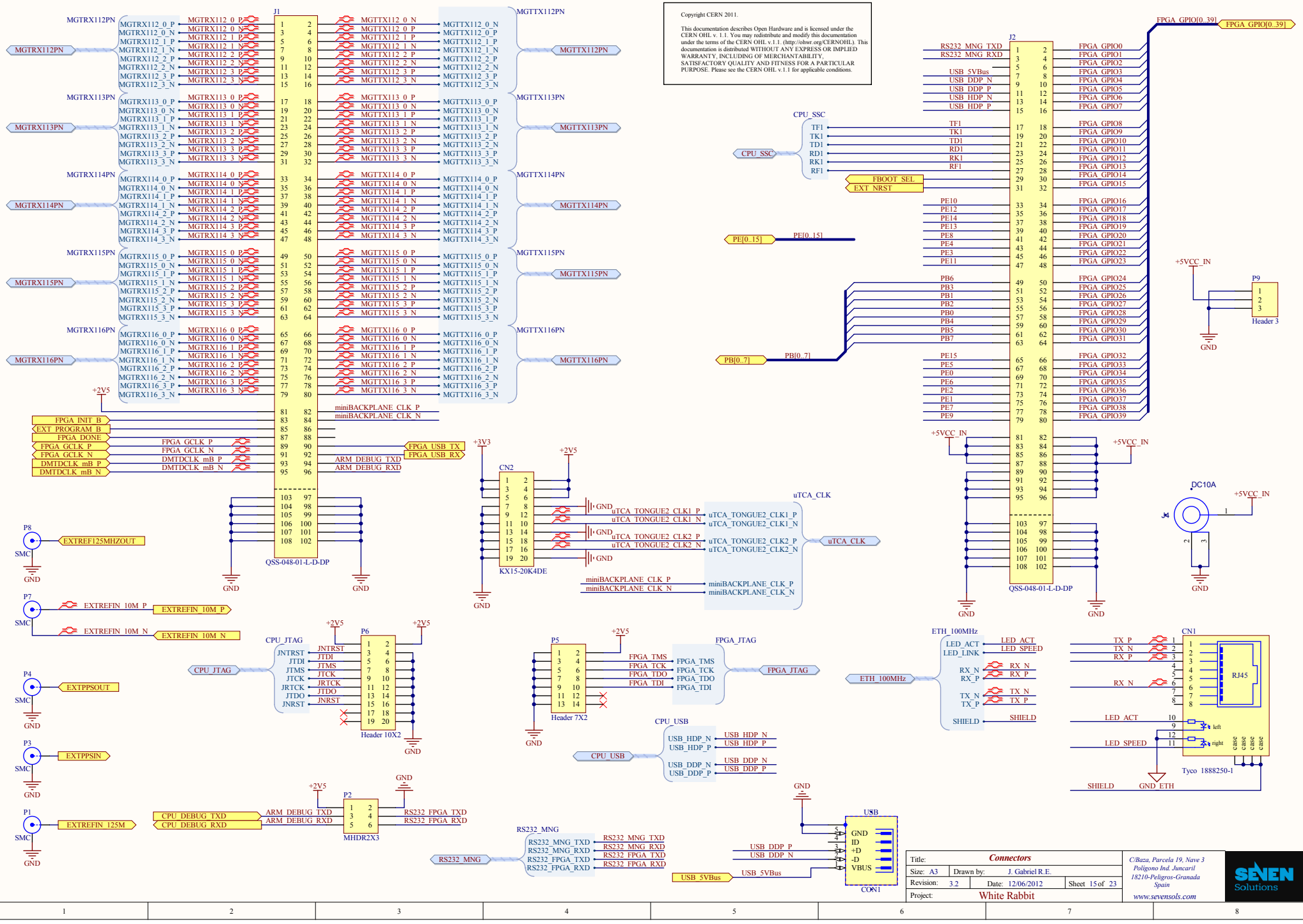
UTCA_MCH_TONGUE3

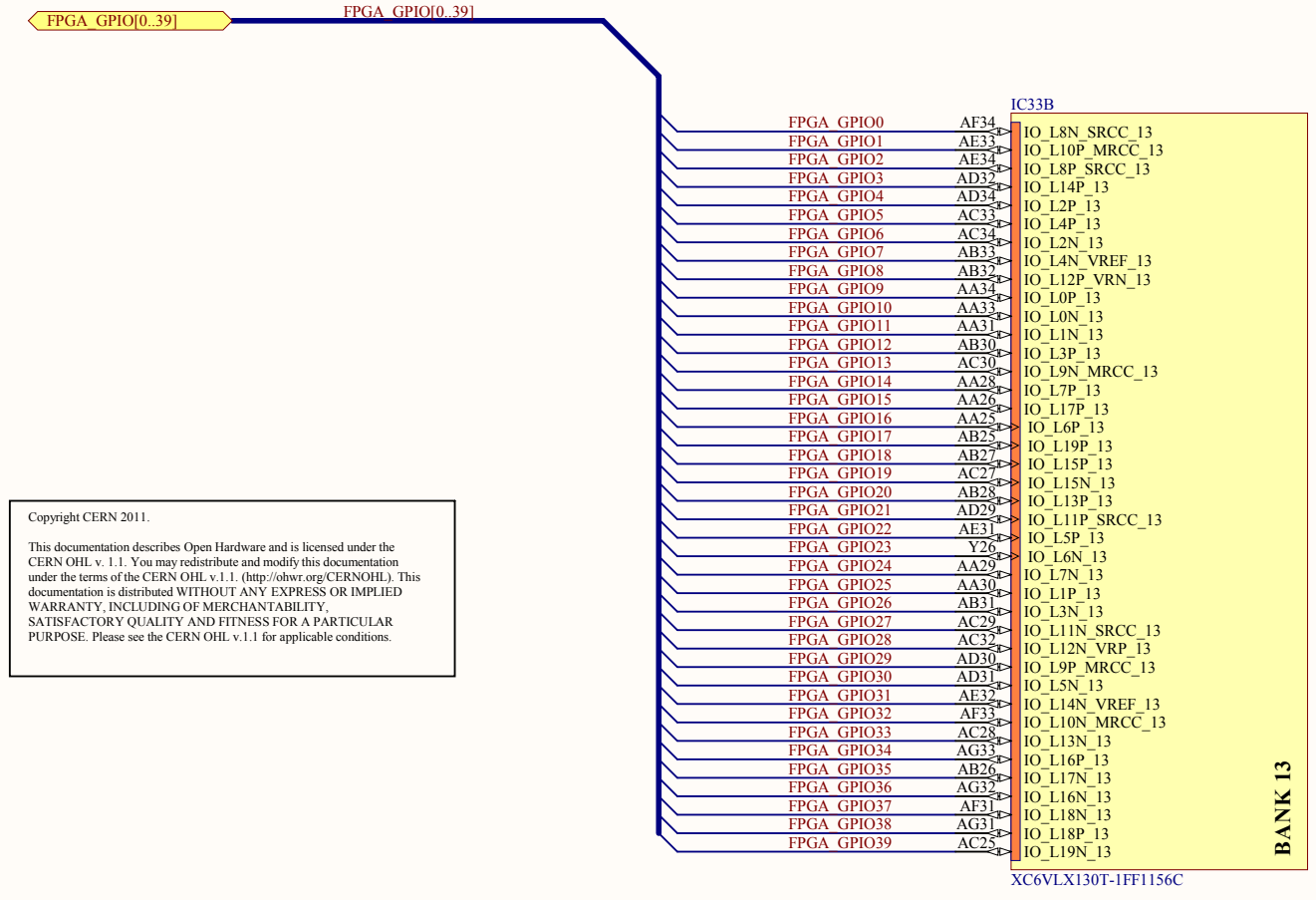
GND

Title:	*uTCA_Tongue3*		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 14 of 23	
Project:	White Rabbit		

C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

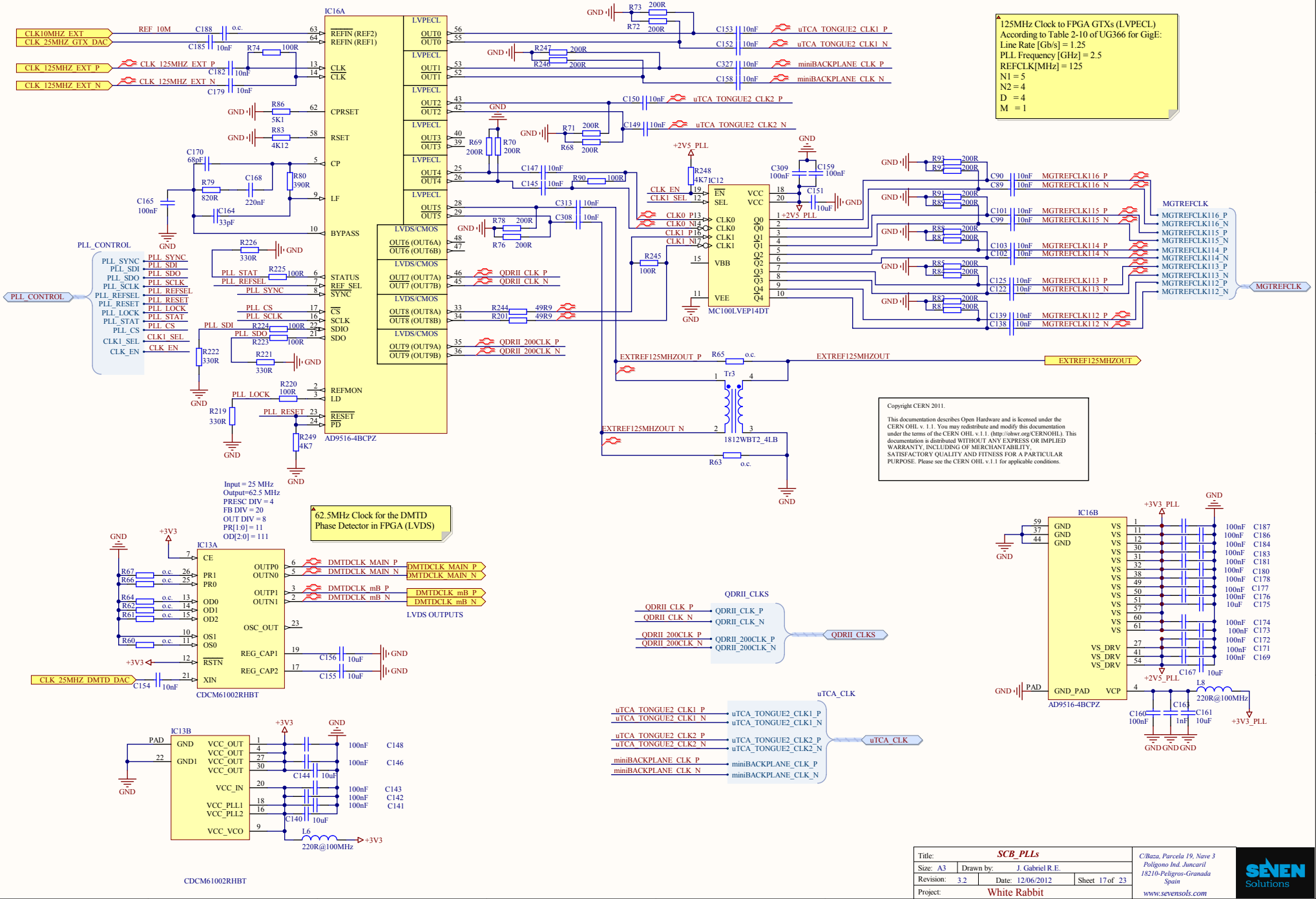
SEVEN Solutions

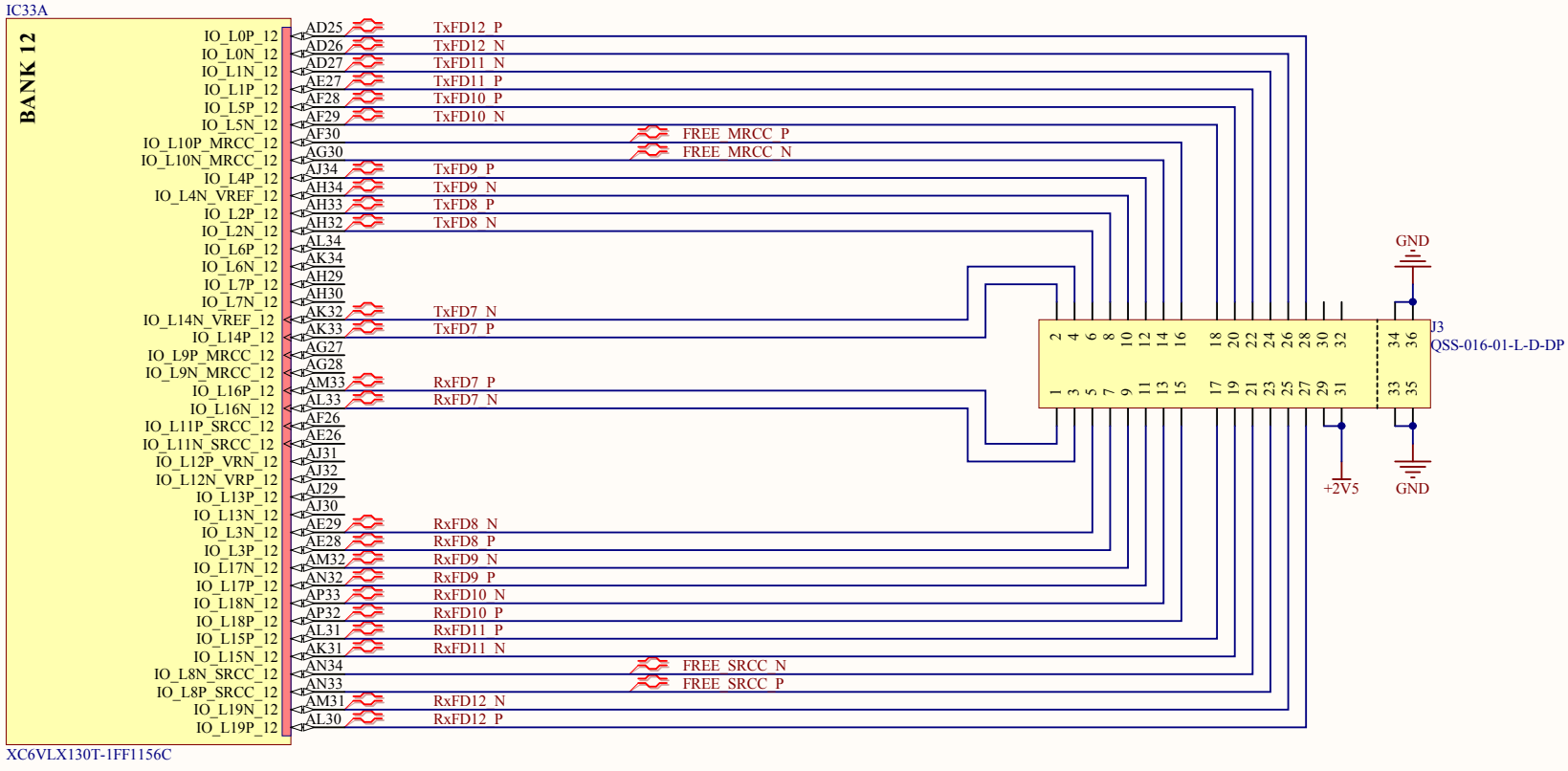

Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
J1
QSS-048-01-L-D-DP
J2
QSS-048-01-L-D-DP
CN2
KX15-20K4DE
P1
P2
P3
P4
P5
P6
P7
P8
P9
CN1
RJ45
Tyco 1888250-1
CON1
USB
Header 7X2
Header 10X2
MHDR2X3
Header 3
DC10A
J4
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
FPGA_GPIO[0..39]
PE[0..15]
PB[0..7]
CPU_SSC
CPU_JTAG
CPU_USB
FPGA_JTAG
uTCA_CLK
ETH_100MHz
RS232_MNG
miniBACKPLANE_CLK_P
miniBACKPLANE_CLK_N
+2V5
+3V3
+5VCC_IN
GND
FPGA_INIT_B
EXT_PROGRAM_B
FPGA_DONE
FPGA_GCLK_P
FPGA_GCLK_N
DMTDCLK_mB_P
DMTDCLK_mB_N
FPGA_USB_TX
FPGA_USB_RX
ARM_DEBUG_TXD
ARM_DEBUG_RXD
EXTREF125MHZOUT
EXTREFIN_10M_P
EXTREFIN_10M_N
EXTPPSOUT
EXTPPSIN
EXTREFIN_125M
CPU_DEBUG_TXD
CPU_DEBUG_RXD
RS232_FPGA_TXD
RS232_FPGA_RXD
RS232_MNG_TXD
RS232_MNG_RXD
FBOOT_SEL
EXT_NRST
USB_5VBus
USB_HDP_N
USB_HDP_P
USB_DDP_N
USB_DDP_P
TF1
TK1
TD1
RD1
RK1
RF1
JNTRST
JTDI
JTMS
JTCK
JRTCK
JTDO
JNRST
LED_ACT
LED_SPEED
LED_LINK
RX_N
RX_P
TX_N
TX_P
SHIELD
GND_ETH
ID
+D
-D
VBUS
left
right
case
Title: Connectors
Size: A3
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 15 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions



Title:	***FPGA_GPIOs***		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 16 of 23	
Project:	White Rabbit		

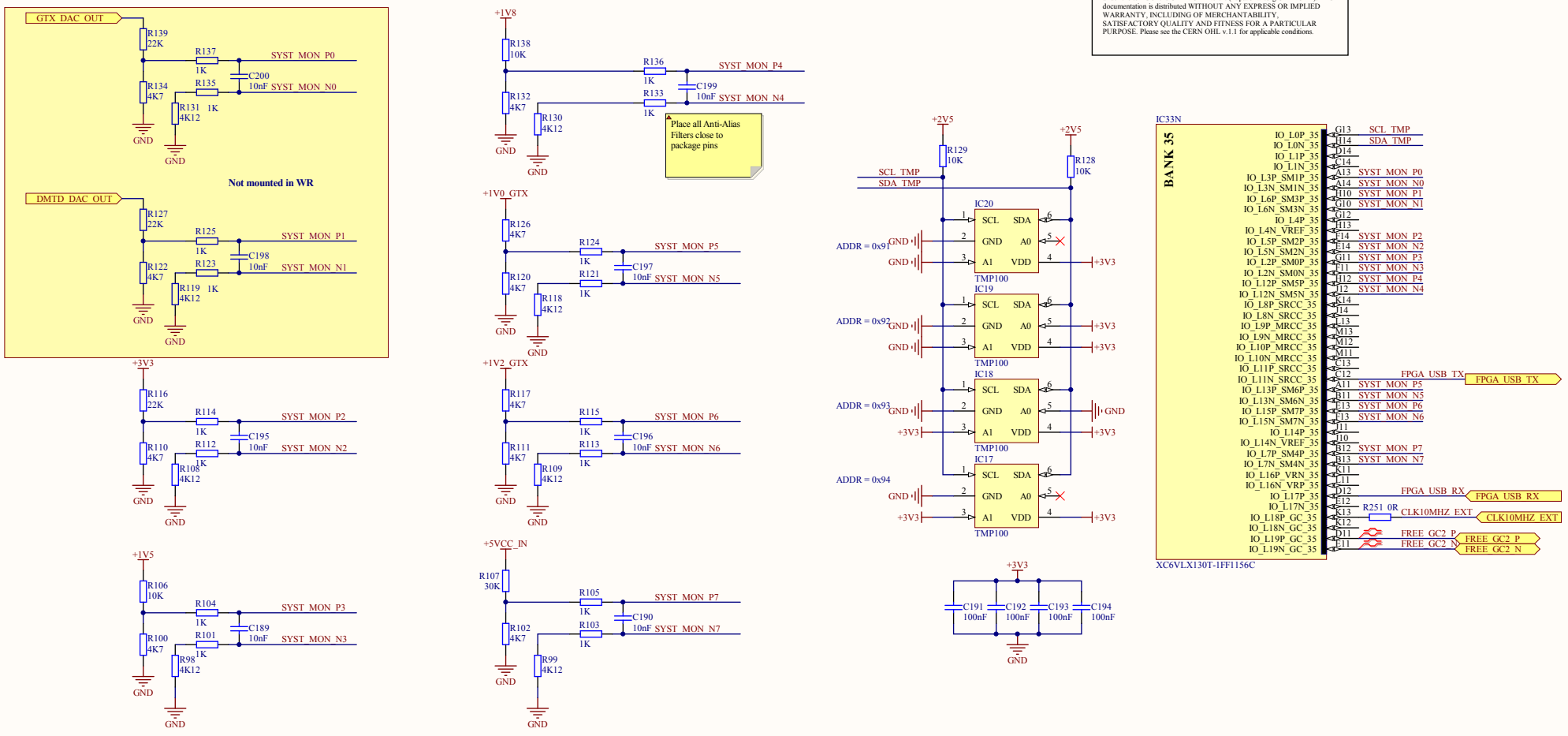
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com


125MHz Clock to FPGA GTXs (LVPECL)
According to Table 2-10 of UG366 for GigE:
Line Rate [Gb/s] = 1.25
PLL Frequency [GHz] = 2.5
REFCLK[MHz] = 125
N1 = 5
N2 = 4
D = 4
M = 1
IC16A
AD9516-4BCPZ
MC100LVEP14DT
IC12
IC16B
AD9516-4BCPZ
IC13A
CDCM61002RHBT
IC13B
CDCM61002RHBT
Input = 25 MHz
Output=62.5 MHz
PRESC DIV = 4
FB DIV = 20
OUT DIV = 8
PR[1:0] = 11
OD[2:0] = 111
62.5MHz Clock for the DMTD
Phase Detector in FPGA (LVDS)
LVDS OUTPUTS
QDRII_CLKS
uTCA_CLK
1812WBT2_4LB
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
Title: SCB_PLLs
Size: A3
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 17 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions



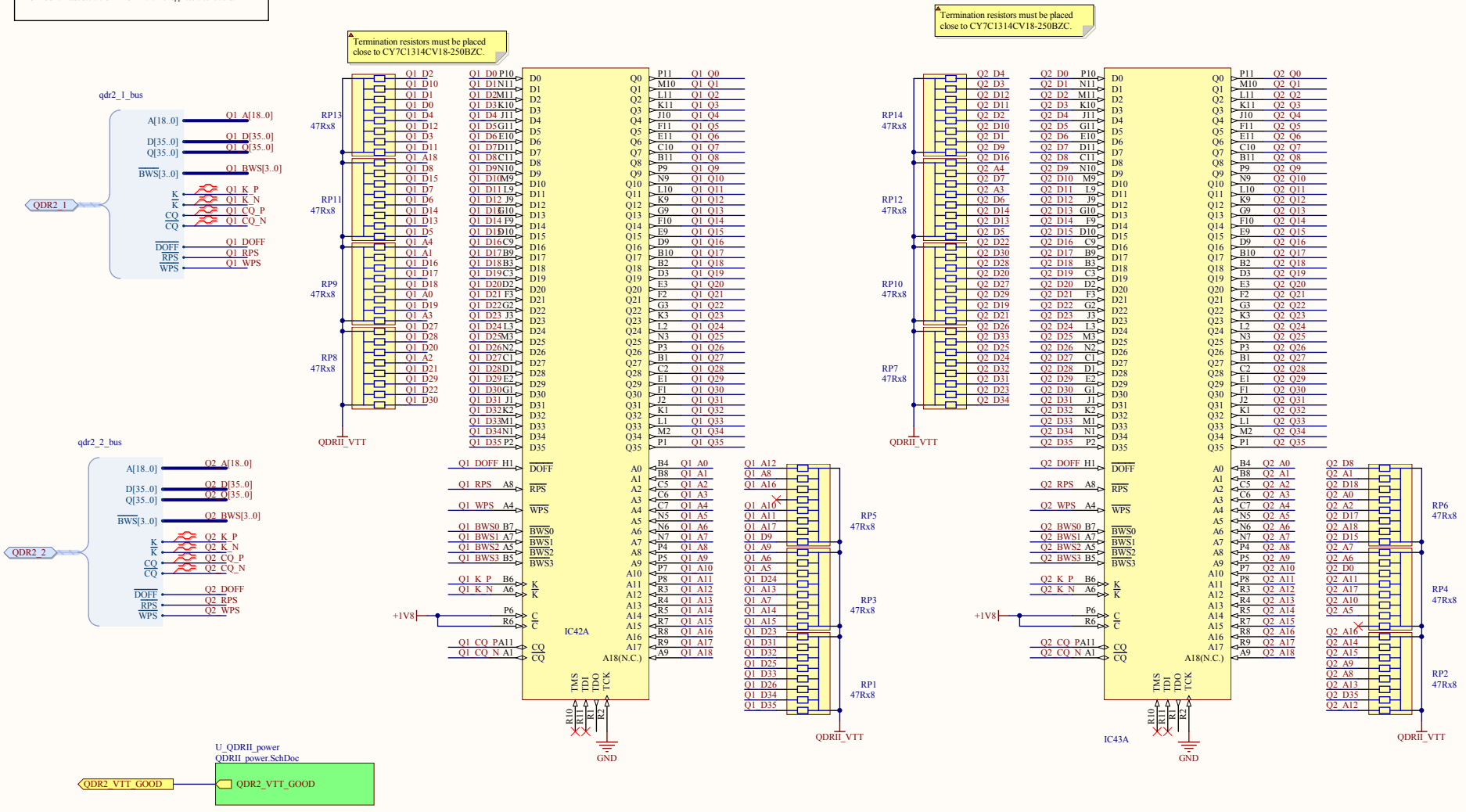
Title:	***SMI_Link_7-12***		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 18 of 23	
Project:	White Rabbit		

C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com



Title:	*FPGA_System_Monitor*		
Size: A3	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 19 of 23	
Project: White Rabbit			

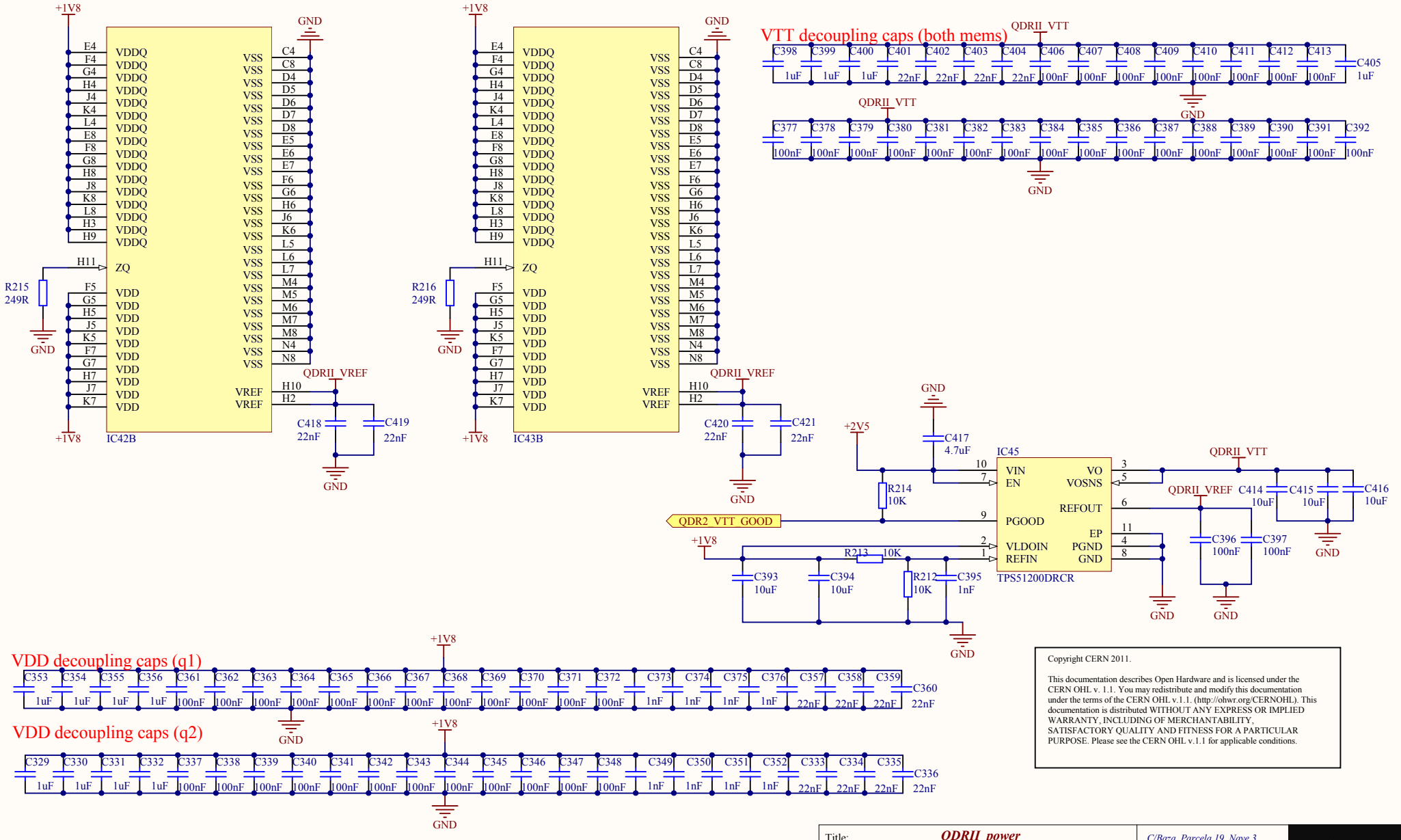
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com



Title:	***QDRII_mem***		
Size: A3	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 20 of 23	
Project: White Rabbit			

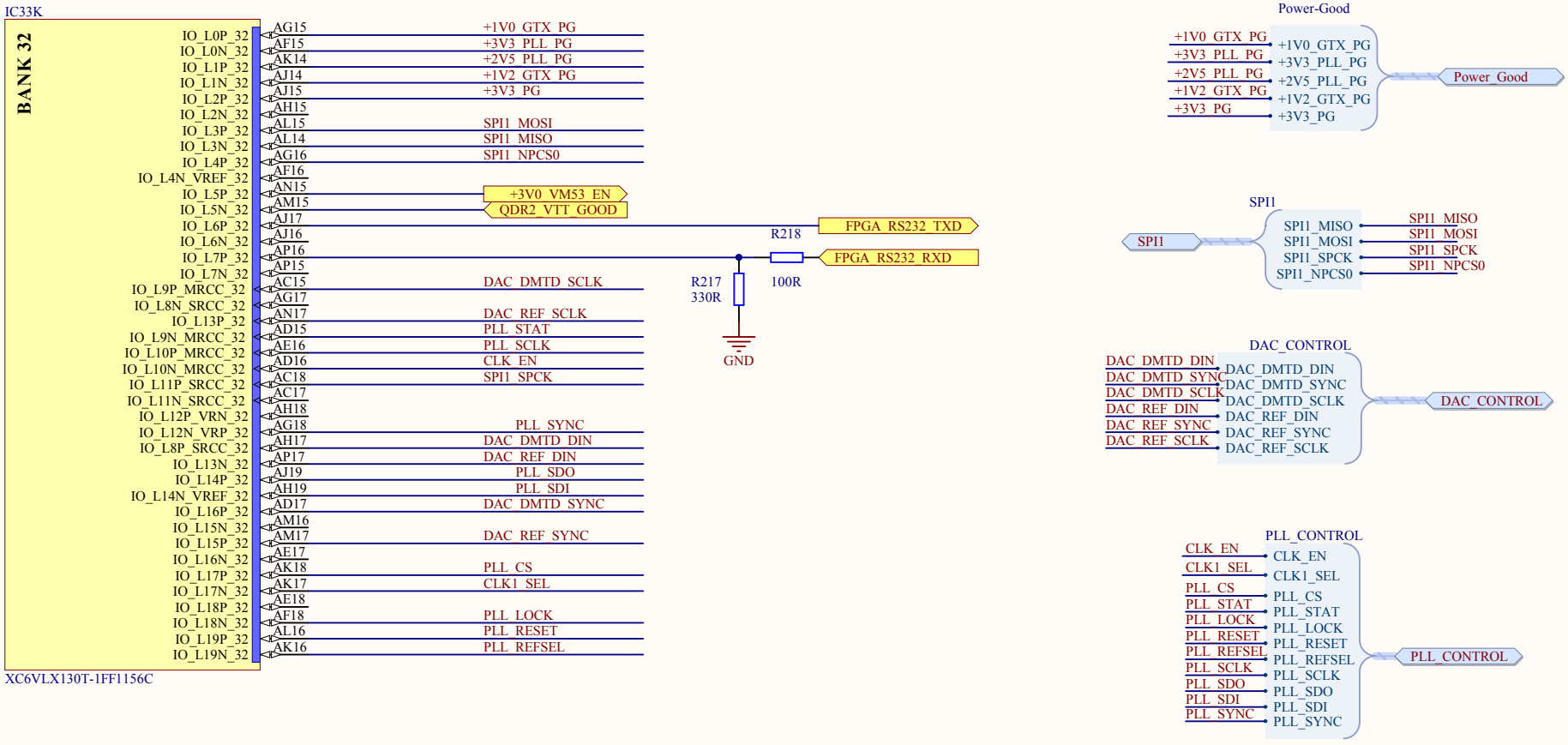
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

SEVEN Solutions



Title:	***QDRII_power***		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 21 of 23	
Project:	White Rabbit		

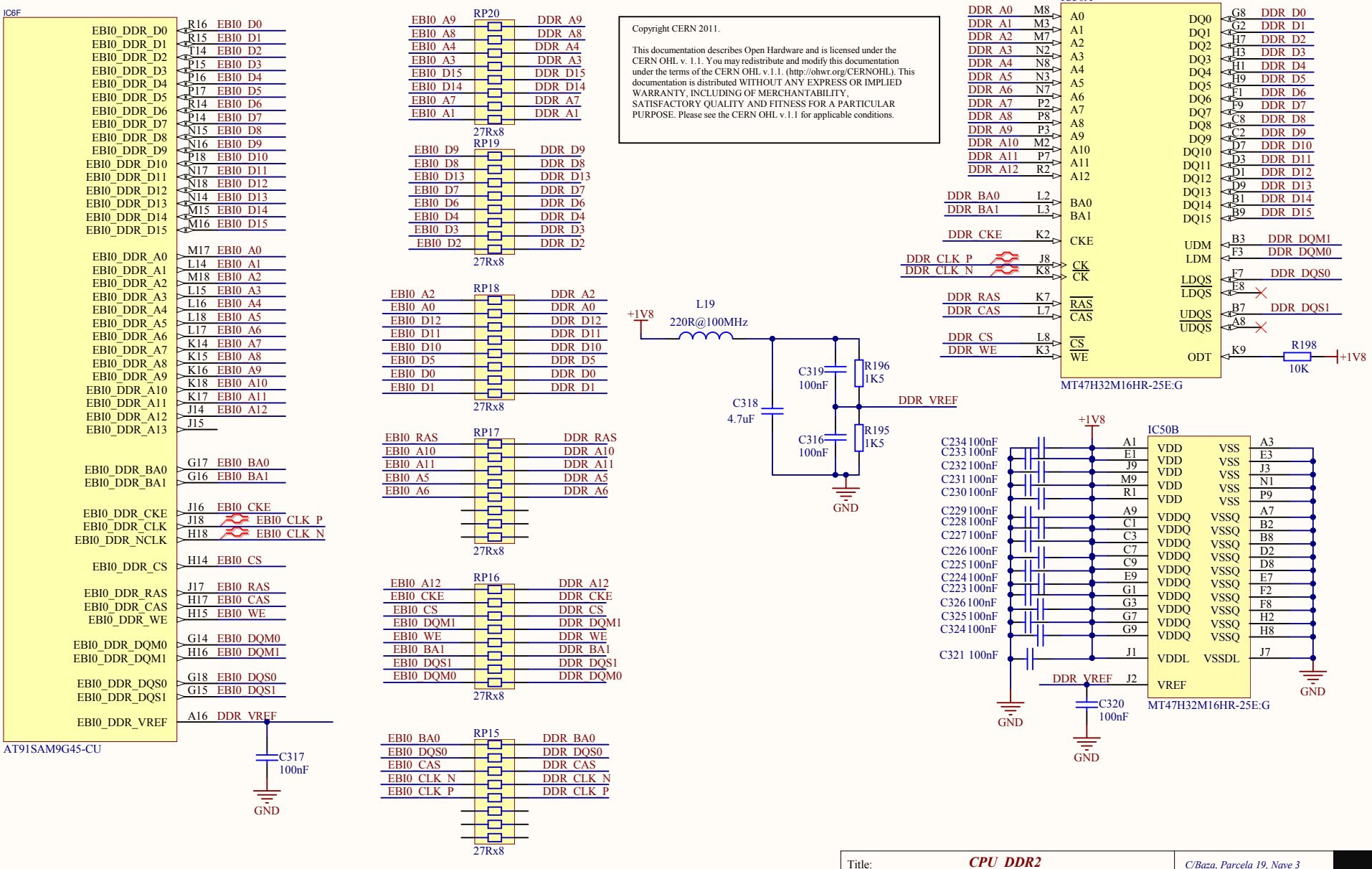
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com



Title:	*FPGA_Peripherals_Control*		
Size: A4	Drawn by: J. Gabriel R.E.		
Revision: 3.2	Date: 12/06/2012	Sheet 22 of 23	
Project:	White Rabbit		

C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com

SEVEN Solutions


IC6F
EBI0_DDR_D0 R16 EBI0_D0
EBI0_DDR_D1 R15 EBI0_D1
EBI0_DDR_D2 T14 EBI0_D2
EBI0_DDR_D3 P15 EBI0_D3
EBI0_DDR_D4 P16 EBI0_D4
EBI0_DDR_D5 P17 EBI0_D5
EBI0_DDR_D6 R14 EBI0_D6
EBI0_DDR_D7 P14 EBI0_D7
EBI0_DDR_D8 N15 EBI0_D8
EBI0_DDR_D9 N16 EBI0_D9
EBI0_DDR_D10 P18 EBI0_D10
EBI0_DDR_D11 N17 EBI0_D11
EBI0_DDR_D12 N18 EBI0_D12
EBI0_DDR_D13 N14 EBI0_D13
EBI0_DDR_D14 M15 EBI0_D14
EBI0_DDR_D15 M16 EBI0_D15
EBI0_DDR_A0 M17 EBI0_A0
EBI0_DDR_A1 L14 EBI0_A1
EBI0_DDR_A2 M18 EBI0_A2
EBI0_DDR_A3 L15 EBI0_A3
EBI0_DDR_A4 L16 EBI0_A4
EBI0_DDR_A5 L18 EBI0_A5
EBI0_DDR_A6 L17 EBI0_A6
EBI0_DDR_A7 K14 EBI0_A7
EBI0_DDR_A8 K15 EBI0_A8
EBI0_DDR_A9 K16 EBI0_A9
EBI0_DDR_A10 K18 EBI0_A10
EBI0_DDR_A11 K17 EBI0_A11
EBI0_DDR_A12 J14 EBI0_A12
EBI0_DDR_A13 J15
EBI0_DDR_BA0 G17 EBI0_BA0
EBI0_DDR_BA1 G16 EBI0_BA1
EBI0_DDR_CKE J16 EBI0_CKE
EBI0_DDR_CLK J18 EBI0_CLK_P
EBI0_DDR_NCLK H18 EBI0_CLK_N
EBI0_DDR_CS H14 EBI0_CS
EBI0_DDR_RAS J17 EBI0_RAS
EBI0_DDR_CAS H17 EBI0_CAS
EBI0_DDR_WE H15 EBI0_WE
EBI0_DDR_DQM0 G14 EBI0_DQM0
EBI0_DDR_DQM1 H16 EBI0_DQM1
EBI0_DDR_DQS0 G18 EBI0_DQS0
EBI0_DDR_DQS1 G15 EBI0_DQS1
EBI0_DDR_VREF A16 DDR_VREF
AT91SAM9G45-CU
C317 100nF
GND
RP20
EBI0_A9 DDR_A9
EBI0_A8 DDR_A8
EBI0_A4 DDR_A4
EBI0_A3 DDR_A3
EBI0_D15 DDR_D15
EBI0_D14 DDR_D14
EBI0_A7 DDR_A7
EBI0_A1 DDR_A1
27Rx8
RP19
EBI0_D9 DDR_D9
EBI0_D8 DDR_D8
EBI0_D13 DDR_D13
EBI0_D7 DDR_D7
EBI0_D6 DDR_D6
EBI0_D4 DDR_D4
EBI0_D3 DDR_D3
EBI0_D2 DDR_D2
27Rx8
RP18
EBI0_A2 DDR_A2
EBI0_A0 DDR_A0
EBI0_D12 DDR_D12
EBI0_D11 DDR_D11
EBI0_D10 DDR_D10
EBI0_D5 DDR_D5
EBI0_D0 DDR_D0
EBI0_D1 DDR_D1
27Rx8
RP17
EBI0_RAS DDR_RAS
EBI0_A10 DDR_A10
EBI0_A11 DDR_A11
EBI0_A5 DDR_A5
EBI0_A6 DDR_A6
27Rx8
RP16
EBI0_A12 DDR_A12
EBI0_CKE DDR_CKE
EBI0_CS DDR_CS
EBI0_DQM1 DDR_DQM1
EBI0_WE DDR_WE
EBI0_BA1 DDR_BA1
EBI0_DQS1 DDR_DQS1
EBI0_DQM0 DDR_DQM0
27Rx8
RP15
EBI0_BA0 DDR_BA0
EBI0_DQS0 DDR_DQS0
EBI0_CAS DDR_CAS
EBI0_CLK_N DDR_CLK_N
EBI0_CLK_P DDR_CLK_P
27Rx8
Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
+1V8
L19
220R@100MHz
C319 100nF
R196 1K5
C318 4.7uF
DDR_VREF
C316 100nF
R195 1K5
GND
IC50A
DDR_A0 M8
DDR_A1 M3
DDR_A2 M7
DDR_A3 N2
DDR_A4 N8
DDR_A5 N3
DDR_A6 N7
DDR_A7 P2
DDR_A8 P8
DDR_A9 P3
DDR_A10 M2
DDR_A11 P7
DDR_A12 R2
DDR_BA0 L2
DDR_BA1 L3
DDR_CKE K2
DDR_CLK_P J8
DDR_CLK_N K8
DDR_RAS K7
DDR_CAS L7
DDR_CS L8
DDR_WE K3
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
BA0 BA1
CKE
CK CK
RAS CAS CS WE
DQ0 G8 DDR_D0
DQ1 G2 DDR_D1
DQ2 H7 DDR_D2
DQ3 H3 DDR_D3
DQ4 H1 DDR_D4
DQ5 H9 DDR_D5
DQ6 F1 DDR_D6
DQ7 F9 DDR_D7
DQ8 C8 DDR_D8
DQ9 C2 DDR_D9
DQ10 D7 DDR_D10
DQ11 D3 DDR_D11
DQ12 D1 DDR_D12
DQ13 D9 DDR_D13
DQ14 B1 DDR_D14
DQ15 B9 DDR_D15
UDM B3 DDR_DQM1
LDM F3 DDR_DQM0
LDQS F7 DDR_DQS0
LDQS E8
UDQS B7 DDR_DQS1
UDQS A8
ODT K9
R198 10K
+1V8
MT47H32M16HR-25E:G
+1V8
C234 100nF
C233 100nF
C232 100nF
C231 100nF
C230 100nF
C229 100nF
C228 100nF
C227 100nF
C226 100nF
C225 100nF
C224 100nF
C223 100nF
C326 100nF
C325 100nF
C324 100nF
C321 100nF
IC50B
VDD A1 E1 J9 M9 R1
VDDQ A9 C1 C3 C7 C9 E9 G1 G3 G7 G9
VDDL J1
VREF J2
VSS A3 E3 J3 N1 P9
VSSQ A7 B2 B8 D2 D8 E7 F2 F8 H2 H8
VSSDL J7
DDR_VREF
C320 100nF
GND
MT47H32M16HR-25E:G
Title: CPU_DDR2
Size: A4
Drawn by: J. Gabriel R.E.
Revision: 3.2
Date: 12/06/2012
Sheet 23 of 23
Project: White Rabbit
C/Baza, Parcela 19, Nave 3
Polígono Ind. Juncaril
18210-Peligros-Granada
Spain
www.sevensols.com
SEVEN Solutions