

Figure 10 illustrates the pin connections for the JAE-KX15-50p package. The diagram shows the package pins (CNS, CN1, CN4) and their connections to the JAE-KX15-50p package. The connections are as follows:

- Power Supply:**
 - VDD (Pin 1) to +12V_BULK
 - VSS (Pin 2) to +V3
 - VDD1 (Pin 3) to +12V_BULK
 - VSS1 (Pin 4) to +V3
 - VDD2 (Pin 5) to +12V_BULK
 - VSS2 (Pin 6) to +V3
 - VDD3 (Pin 7) to +12V_BULK
 - VSS3 (Pin 8) to +V3
 - VDD4 (Pin 9) to +12V_BULK
 - VSS4 (Pin 10) to +V3
- Control Pins:**
 - RD (Pin 11) to RD
 - WR (Pin 12) to WR
 - CS (Pin 13) to CS
 - OE (Pin 14) to OE
 - WE (Pin 15) to WE
 - CS1 (Pin 16) to CS1
 - OE1 (Pin 17) to OE1
 - WE1 (Pin 18) to WE1
 - CS2 (Pin 19) to CS2
 - OE2 (Pin 20) to OE2
 - WE2 (Pin 21) to WE2
 - CS3 (Pin 22) to CS3
 - OE3 (Pin 23) to OE3
 - WE3 (Pin 24) to WE3
 - CS4 (Pin 25) to CS4
 - OE4 (Pin 26) to OE4
 - WE4 (Pin 27) to WE4
 - CS5 (Pin 28) to CS5
 - OE5 (Pin 29) to OE5
 - WE5 (Pin 30) to WE5
- Data Pins:**
 - DQ (Pin 31) to DQ
 - DQ1 (Pin 32) to DQ1
 - DQ2 (Pin 33) to DQ2
 - DQ3 (Pin 34) to DQ3
 - DQ4 (Pin 35) to DQ4
 - DQ5 (Pin 36) to DQ5
 - DQ6 (Pin 37) to DQ6
 - DQ7 (Pin 38) to DQ7
 - DQ8 (Pin 39) to DQ8
 - DQ9 (Pin 40) to DQ9
 - DQ10 (Pin 41) to DQ10
 - DQ11 (Pin 42) to DQ11
 - DQ12 (Pin 43) to DQ12
 - DQ13 (Pin 44) to DQ13
 - DQ14 (Pin 45) to DQ14
 - DQ15 (Pin 46) to DQ15
 - DQ16 (Pin 47) to DQ16
 - DQ17 (Pin 48) to DQ17
 - DQ18 (Pin 49) to DQ18
 - DQ19 (Pin 50) to DQ19
- Package Connections:**
 - JAE-KX15-50p (Pin 1) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 2) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 3) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 4) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 5) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 6) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 7) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 8) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 9) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 10) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 11) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 12) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 13) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 14) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 15) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 16) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 17) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 18) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 19) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 20) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 21) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 22) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 23) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 24) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 25) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 26) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 27) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 28) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 29) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 30) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 31) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 32) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 33) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 34) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 35) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 36) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 37) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 38) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 39) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 40) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 41) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 42) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 43) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 44) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 45) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 46) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 47) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 48) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 49) to JAE-KX15-50p
 - JAE-KX15-50p (Pin 50) to JAE-KX15-50p

Main System Diagram with:

- big Cyclone3-120 FPGA
- AT91SAM9263 CPU + memories + peripherals
- downlink PHYs and uCA backplane interface

Includes all front panel controls/connectors being placed on MCH PCB1 and most important connectors (backplane, mezzanines JTACs)

DP0				DP4			
MB downlink phy SchDoc				MB downlink phy SchDoc			
DP SYNCH0	SYNCH			DP SYNCH4	SYNCH		
DP LOOP0	LOOPEN			DP LOOP4	LOOPEN		
DP PRE0	PRESN			DP PRE4	PRESN		
DP ENAB0	ENABEN			DP ENAB4	ENABEN		
DP SYNC PASS0	SYNPASS			DP SYNC PASS4	SYNPASS		
DP TX0		TX	Tx0	DP TX4		TX	Tx4
DP RX0		RX	Rx0	DP RX4		RX	Rx4
REFLCK DP0	REFLCK			REFLCK DP4	REFLCK		
REFLCK DP0	REFLCK			REFLCK DP4	REFLCK		
DP SYNCH0	SYNCH			DP SYNCH8	SYNCH		
DP LOOP0	LOOPEN			DP LOOP8	LOOPEN		
DP PRE0	PRESN			DP PRE8	PRESN		
DP ENAB0	ENABEN			DP ENAB8	ENABEN		
DP SYNC PASS0	SYNPASS			DP SYNC PASS8	SYNPASS		
DP TX0		TX	Tx0	DP TX8		TX	Tx8
DP RX0		RX	Rx0	DP RX8		RX	Rx8
REFLCK DP0	REFLCK			REFLCK DP8	REFLCK		
REFLCK DP0	REFLCK			REFLCK DP8	REFLCK		
DP SYNCH0	SYNCH			DP SYNCH12	SYNCH		
DP LOOP0	LOOPEN			DP LOOP12	LOOPEN		
DP PRE0	PRESN			DP PRE12	PRESN		
DP ENAB0	ENABEN			DP ENAB12	ENABEN		
DP SYNC PASS0	SYNPASS			DP SYNC PASS12	SYNPASS		
DP TX0		TX	Tx0	DP TX12		TX	Tx12
DP RX0		RX	Rx0	DP RX12		RX	Rx12
REFLCK DP0	REFLCK			REFLCK DP12	REFLCK		
REFLCK DP0	REFLCK			REFLCK DP12	REFLCK		
DP SYNCH0	SYNCH			DP SYNCH16	SYNCH		
DP LOOP0	LOOPEN			DP LOOP16	LOOPEN		
DP PRE0	PRESN			DP PRE16	PRESN		
DP ENAB0	ENABEN			DP ENAB16	ENABEN		
DP SYNC PASS0	SYNPASS			DP SYNC PASS16	SYNPASS		
DP TX0		TX	Tx0	DP TX16		TX	Tx16
DP RX0		RX	Rx0	DP RX16		RX	Rx16
REFLCK DP0	REFLCK			REFLCK DP16	REFLCK		
REFLCK DP0	REFLCK			REFLCK DP16	REFLCK		
DP SYNCH0	SYNCH			DP SYNCH20	SYNCH		
DP LOOP0	LOOPEN			DP LOOP20	LOOPEN		
DP PRE0	PRESN			DP PRE20	PRESN		
DP ENAB0	ENABEN			DP ENAB20	ENABEN		
DP SYNC PASS0	SYNPASS			DP SYNC PASS20	SYNPASS		
DP TX0		TX	Tx0	DP TX20		TX	Tx20
DP RX0		RX	Rx0	DP RX20		RX	Rx20
REFLCK DP0	REFLCK			REFLCK DP20	REFLCK		
REFLCK DP0	REFLCK			REFLCK DP20	REFLCK		
DP SYNCH0	SYNCH			DP SYNCH24	SYNCH		
DP LOOP0	LOOPEN			DP LOOP24	LOOPEN		
DP PRE0	PRESN			DP PRE24	PRESN		
DP ENAB0	ENABEN			DP ENAB24	ENABEN		
DP SYNC PASS0	SYNPASS			DP SYNC PASS24	SYNPASS		
DP TX0		TX	Tx0	DP TX24		TX	Tx24
DP RX0		RX	Rx0	DP RX24		RX	Rx24
REFLCK DP0	REFLCK			REFLCK DP24	REFLCK		
REFLCK DP0	REFLCK			REFLCK DP24	REFLCK		
DP SYNCH0	SYNCH			DP SYNCH28	SYNCH		
DP LOOP0	LOOPEN			DP LOOP28	LOOPEN		
DP PRE0	PRESN			DP PRE28	PRESN		
DP ENAB0							

[illegible]

Figure 1: JTAG / DBGU pin connections for the iBM7265. The diagram shows two 16-pin connectors. The left connector (CN7) is connected to a -2V5 supply and has pins for JTAG TCK, JTAG TDO, JTAG TDI, JTAG TMS, JTAG TMS, JTAG TMS, CPU INTSEI, CPU TCK, CPU TCK, and DBG TxD. The right connector (CN8) is connected to a +2V5 supply and has pins for JTAG TCK, JTAG TDO, JTAG TDI, JTAG TMS, JTAG TMS, JTAG TMS, CPU INTSEI, CPU TCK, CPU TCK, and DBG RxD. A note indicates that JTAG TMS and CPU INTSEI are connected to the same pin on the right connector. A legend at the bottom shows the pin numbers for CN7 and CN8.

Pin	Signal	Pin	Signal
1	JTAG TCK	1	JTAG TCK
2	JTAG TDO	2	JTAG TDO
3	JTAG TDI	3	JTAG TDI
4	JTAG TMS	4	JTAG TMS
5	JTAG TMS	5	JTAG TMS
6	JTAG TMS	6	JTAG TMS
7	CPU INTSEI	7	CPU INTSEI
8	CPU TCK	8	CPU TCK
9	CPU TCK	9	CPU TCK
10	DBG TxD	10	DBG RxD

The diagram illustrates the internal structure of the SMI TX00-TX03 and SMI RX00-RX03 components. A central CNU (Control and Network Unit) block, labeled 'SMT 14 0.5-30DS-0.5V(S7)', is connected to four SMI TX blocks (TX00, TX01, TX02, TX03) and four SMI RX blocks (RX00, RX01, RX02, RX03). The CNU block has 32 pins, numbered 1 to 32. Pins 1-8 are connected to SMI TX00, pins 9-16 to SMI TX01, pins 17-24 to SMI TX02, and pins 25-32 to SMI TX03. The CNU block also has pins for SMI RX00, SMI RX01, SMI RX02, and SMI RX03. A +V3.3 supply is connected to pin 1, and a GND connection is shown at the bottom. The CNU block is labeled 'CNU' and 'SMT 14 0.5-30DS-0.5V(S7)'.

Project:	White Rabbit Switch MCH - mainboard		
Sheet:	Main (top-level) diagram		
Version:	1.1.0	Date:	2009/11/12
Author:	Tomasz Wlostawski	License:	Open Hardware License (OHL)
Company:	CERN BE-CO-IT		