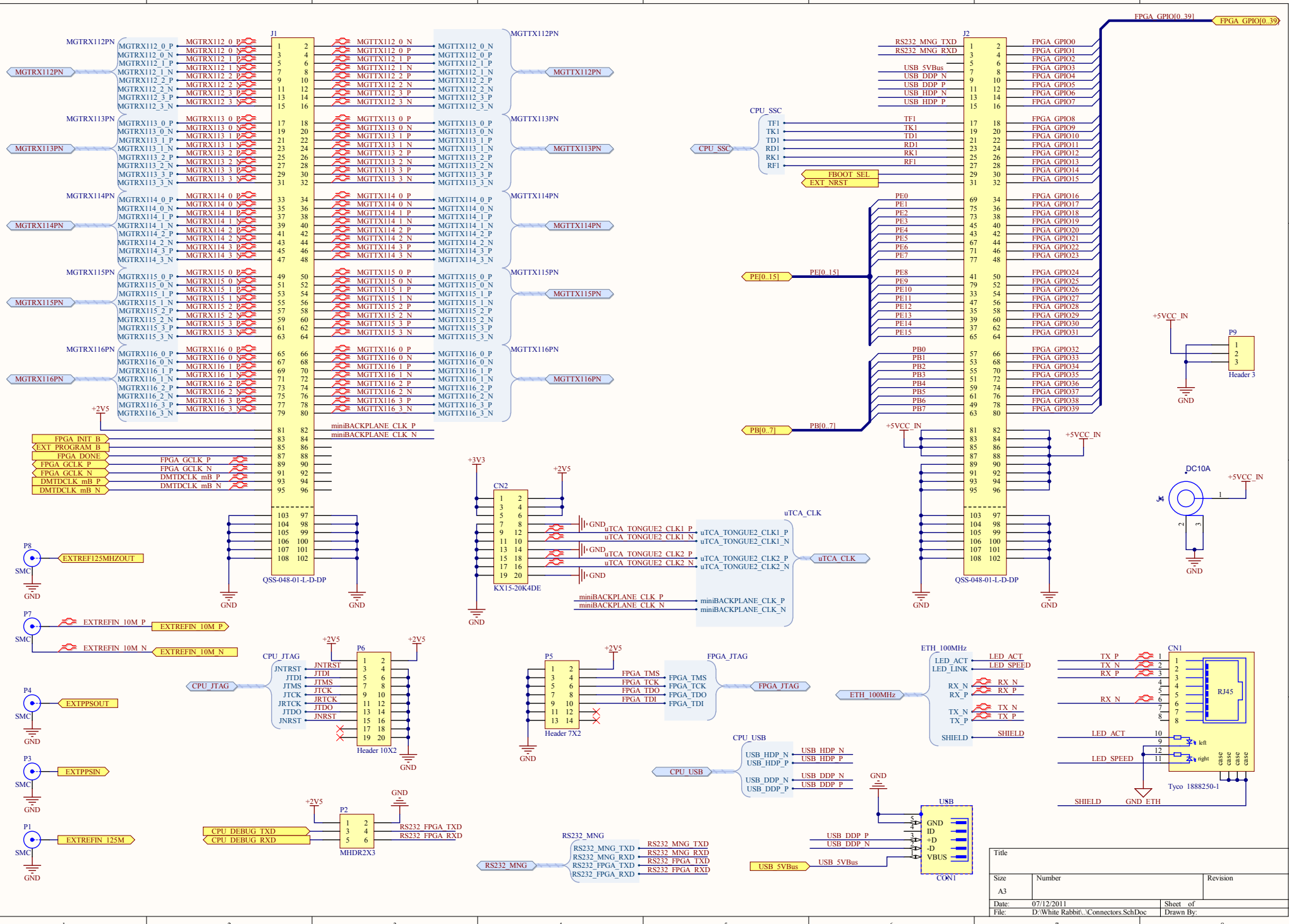
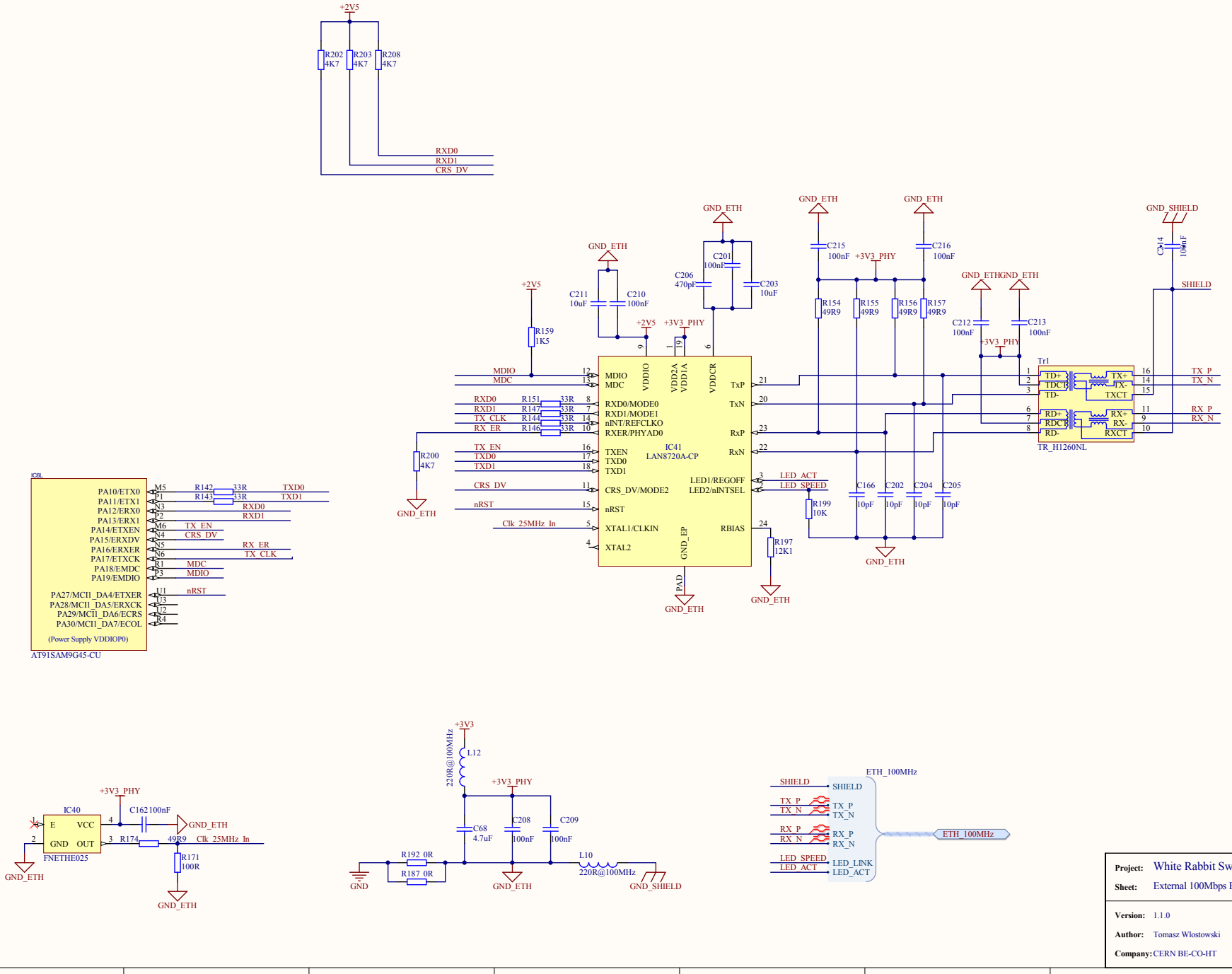
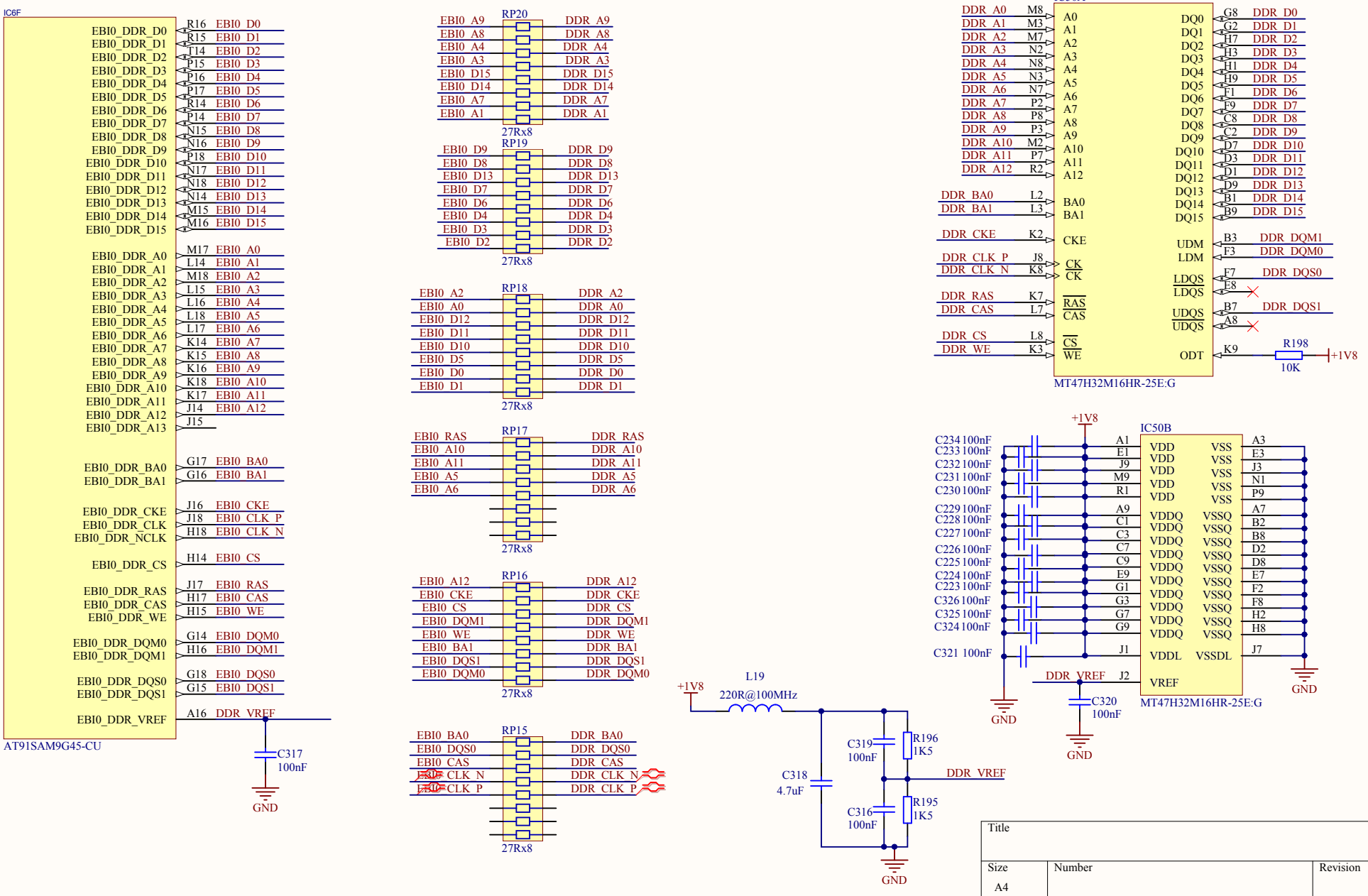

J1
QSS-048-01-L-D-DP
J2
QSS-048-01-L-D-DP
CN2
KX15-20K4DE
P1
P2
MHDR2X3
P3
P4
P5
Header 7X2
P6
Header 10X2
P7
P8
P9
Header 3
DC10A
CN1
RJ45
Tyco 1888250-1
USB
CON1
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
FPGA_GPIO[0..39]
PE[0..15]
PB[0..7]
+5VCC_IN
+2V5
+3V3
GND
uTCA_CLK
FPGA_JTAG
CPU_JTAG
CPU_SSC
CPU_USB
ETH_100MHz
RS232_MNG
miniBACKPLANE_CLK_P
miniBACKPLANE_CLK_N
FPGA_INIT_B
EXT_PROGRAM_B
FPGA_DONE
FPGA_GCLK_P
FPGA_GCLK_N
DMTDCLK_mB_P
DMTDCLK_mB_N
EXTREF125MHZOUT
EXTREFIN_10M_P
EXTREFIN_10M_N
EXTPPSOUT
EXTPPSIN
EXTREFIN_125M
FBOOT_SEL
EXT_NRST
CPU_DEBUG_TXD
CPU_DEBUG_RXD
RS232_FPGA_TXD
RS232_FPGA_RXD
RS232_MNG_TXD
RS232_MNG_RXD
USB_HDP_N
USB_HDP_P
USB_DDP_N
USB_DDP_P
USB_5VBus
LED_ACT
LED_SPEED
SHIELD
Title
Size
A3
Number
Revision
Date: 07/12/2011
File: D:\White Rabbit\..\Connectors.SchDoc
Sheet of
Drawn By:



Project:	White Rabbit Switch MCH - mainboard
Sheet:	External 100Mbps Ethernet PHY & magnetics
Version:	1.1.0
Date:	2009/11/12
Author:	Tomasz Wlostowski
License:	Open Hardware License (OHL)
Company:	CERN BE-CO-HT


IC6F
EBI0_DDR_D0 R16 EBI0_D0
EBI0_DDR_D1 R15 EBI0_D1
EBI0_DDR_D2 T14 EBI0_D2
EBI0_DDR_D3 P15 EBI0_D3
EBI0_DDR_D4 P16 EBI0_D4
EBI0_DDR_D5 P17 EBI0_D5
EBI0_DDR_D6 R14 EBI0_D6
EBI0_DDR_D7 P14 EBI0_D7
EBI0_DDR_D8 N15 EBI0_D8
EBI0_DDR_D9 N16 EBI0_D9
EBI0_DDR_D10 P18 EBI0_D10
EBI0_DDR_D11 N17 EBI0_D11
EBI0_DDR_D12 N18 EBI0_D12
EBI0_DDR_D13 N14 EBI0_D13
EBI0_DDR_D14 M15 EBI0_D14
EBI0_DDR_D15 M16 EBI0_D15
EBI0_DDR_A0 M17 EBI0_A0
EBI0_DDR_A1 L14 EBI0_A1
EBI0_DDR_A2 M18 EBI0_A2
EBI0_DDR_A3 L15 EBI0_A3
EBI0_DDR_A4 L16 EBI0_A4
EBI0_DDR_A5 L18 EBI0_A5
EBI0_DDR_A6 L17 EBI0_A6
EBI0_DDR_A7 K14 EBI0_A7
EBI0_DDR_A8 K15 EBI0_A8
EBI0_DDR_A9 K16 EBI0_A9
EBI0_DDR_A10 K18 EBI0_A10
EBI0_DDR_A11 K17 EBI0_A11
EBI0_DDR_A12 J14 EBI0_A12
EBI0_DDR_A13 J15
EBI0_DDR_BA0 G17 EBI0_BA0
EBI0_DDR_BA1 G16 EBI0_BA1
EBI0_DDR_CKE J16 EBI0_CKE
EBI0_DDR_CLK J18 EBI0_CLK_P
EBI0_DDR_NCLK H18 EBI0_CLK_N
EBI0_DDR_CS H14 EBI0_CS
EBI0_DDR_RAS J17 EBI0_RAS
EBI0_DDR_CAS H17 EBI0_CAS
EBI0_DDR_WE H15 EBI0_WE
EBI0_DDR_DQM0 G14 EBI0_DQM0
EBI0_DDR_DQM1 H16 EBI0_DQM1
EBI0_DDR_DQS0 G18 EBI0_DQS0
EBI0_DDR_DQS1 G15 EBI0_DQS1
EBI0_DDR_VREF A16 DDR_VREF
AT91SAM9G45-CU
C317 100nF
GND
RP20
EBI0_A9 DDR_A9
EBI0_A8 DDR_A8
EBI0_A4 DDR_A4
EBI0_A3 DDR_A3
EBI0_D15 DDR_D15
EBI0_D14 DDR_D14
EBI0_A7 DDR_A7
EBI0_A1 DDR_A1
27Rx8
RP19
EBI0_D9 DDR_D9
EBI0_D8 DDR_D8
EBI0_D13 DDR_D13
EBI0_D7 DDR_D7
EBI0_D6 DDR_D6
EBI0_D4 DDR_D4
EBI0_D3 DDR_D3
EBI0_D2 DDR_D2
27Rx8
RP18
EBI0_A2 DDR_A2
EBI0_A0 DDR_A0
EBI0_D12 DDR_D12
EBI0_D11 DDR_D11
EBI0_D10 DDR_D10
EBI0_D5 DDR_D5
EBI0_D0 DDR_D0
EBI0_D1 DDR_D1
27Rx8
RP17
EBI0_RAS DDR_RAS
EBI0_A10 DDR_A10
EBI0_A11 DDR_A11
EBI0_A5 DDR_A5
EBI0_A6 DDR_A6
27Rx8
RP16
EBI0_A12 DDR_A12
EBI0_CKE DDR_CKE
EBI0_CS DDR_CS
EBI0_DQM1 DDR_DQM1
EBI0_WE DDR_WE
EBI0_BA1 DDR_BA1
EBI0_DQS1 DDR_DQS1
EBI0_DQM0 DDR_DQM0
27Rx8
RP15
EBI0_BA0 DDR_BA0
EBI0_DQS0 DDR_DQS0
EBI0_CAS DDR_CAS
EBI0_CLK_N DDR_CLK_N
EBI0_CLK_P DDR_CLK_P
27Rx8
IC50A
DDR_A0 M8
DDR_A1 M3
DDR_A2 M7
DDR_A3 N2
DDR_A4 N8
DDR_A5 N3
DDR_A6 N7
DDR_A7 P2
DDR_A8 P8
DDR_A9 P3
DDR_A10 M2
DDR_A11 P7
DDR_A12 R2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
DDR_BA0 L2
DDR_BA1 L3
BA0 BA1
DDR_CKE K2
CKE
DDR_CLK_P J8
DDR_CLK_N K8
CK CK
DDR_RAS K7
DDR_CAS L7
RAS CAS
DDR_CS L8
DDR_WE K3
CS WE
DQ0 G8 DDR_D0
DQ1 G2 DDR_D1
DQ2 H7 DDR_D2
DQ3 H3 DDR_D3
DQ4 H1 DDR_D4
DQ5 H9 DDR_D5
DQ6 F1 DDR_D6
DQ7 F9 DDR_D7
DQ8 C8 DDR_D8
DQ9 C2 DDR_D9
DQ10 D7 DDR_D10
DQ11 D3 DDR_D11
DQ12 D1 DDR_D12
DQ13 D9 DDR_D13
DQ14 B1 DDR_D14
DQ15 B9 DDR_D15
UDM B3 DDR_DQM1
LDM F3 DDR_DQM0
LDQS F7 DDR_DQS0
LDQS E8
UDQS B7 DDR_DQS1
UDQS A8
ODT K9
R198 10K
+1V8
MT47H32M16HR-25E:G
+1V8
IC50B
C234 100nF
C233 100nF
C232 100nF
C231 100nF
C230 100nF
C229 100nF
C228 100nF
C227 100nF
C226 100nF
C225 100nF
C224 100nF
C223 100nF
C326 100nF
C325 100nF
C324 100nF
C321 100nF
A1 E1 J9 M9 R1 A9 C1 C3 C7 C9 E9 G1 G3 G7 G9 J1
VDD VDD VDD VDD VDD VDDQ VDDQ VDDQ VDDQ VDDQ VDDQ VDDQ VDDQ VDDQ VDDQ VDDL
VSS VSS VSS VSS VSS VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSQ VSSDL
A3 E3 J3 N1 P9 A7 B2 B8 D2 D8 E7 F2 F8 H2 H8 J7
DDR_VREF J2
VREF
C320 100nF
GND
MT47H32M16HR-25E:G
+1V8
L19
220R@100MHz
C319 100nF
C318 4.7uF
C316 100nF
R196 1K5
R195 1K5
DDR_VREF
GND
Title
Size A4
Number
Revision
Date: 07/12/2011
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Sheet of
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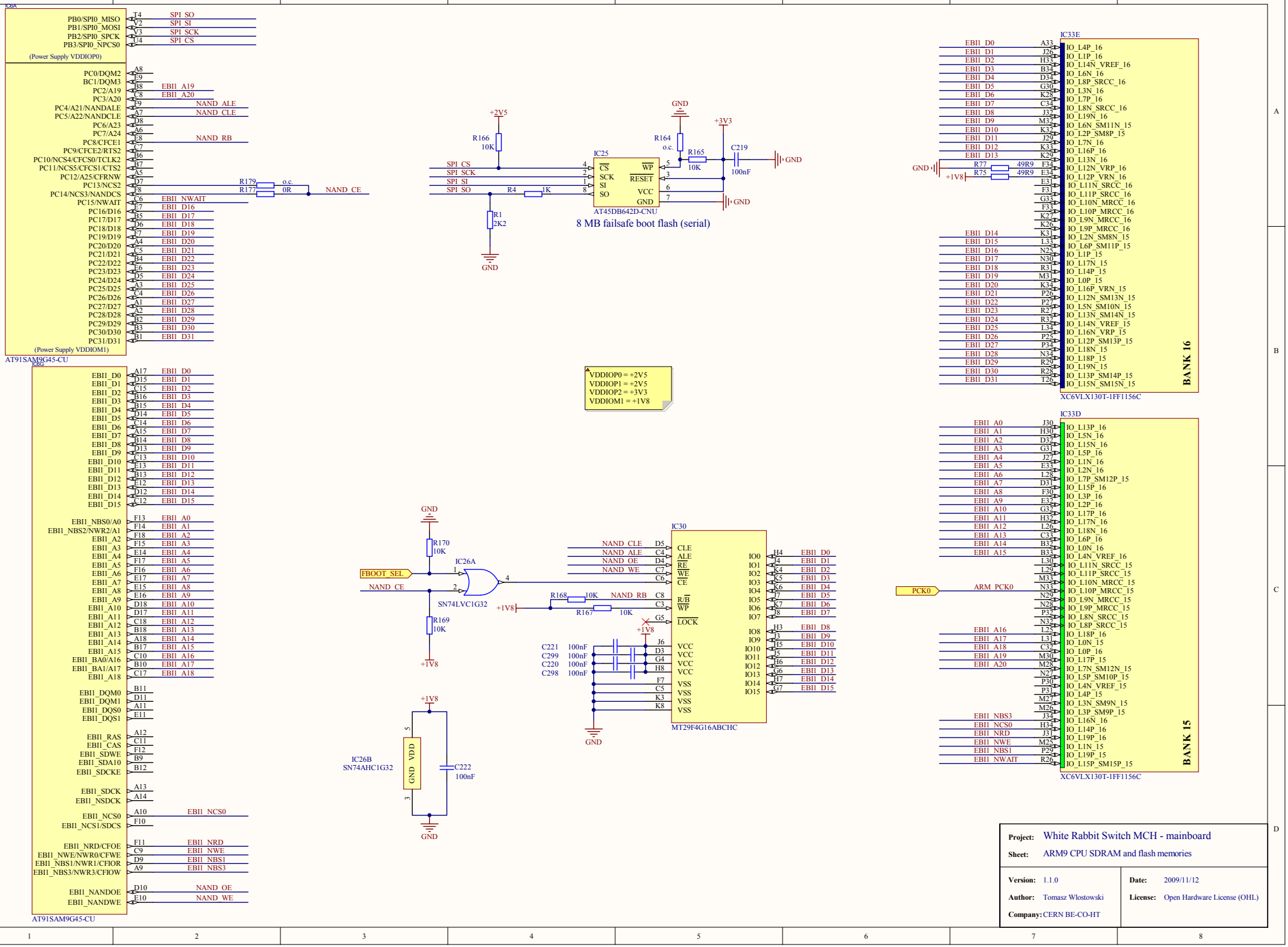
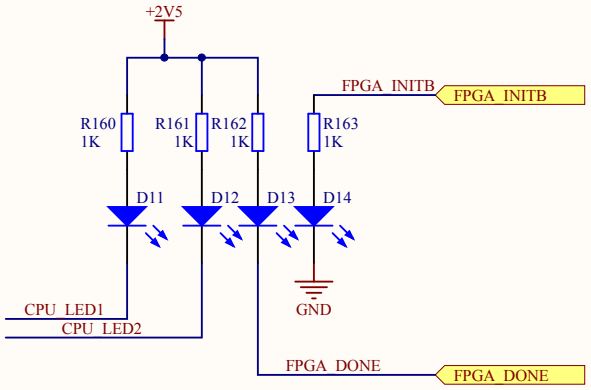
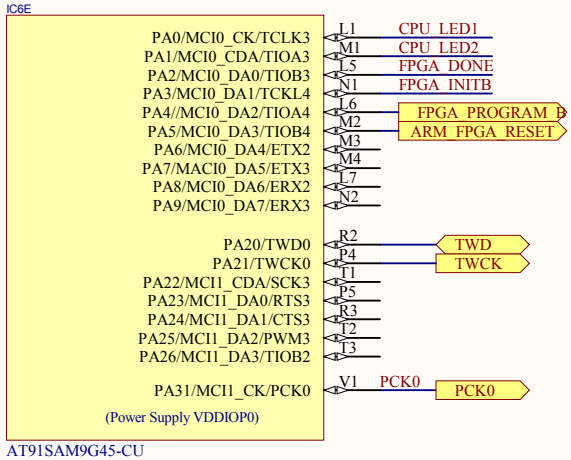
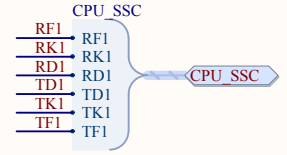
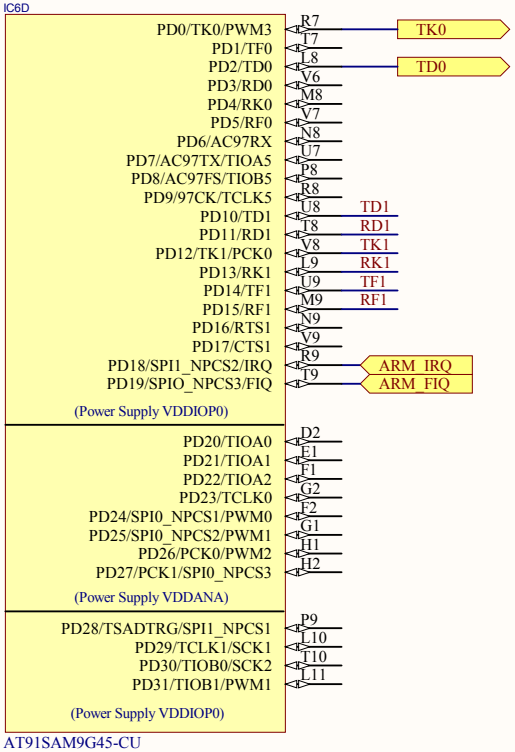


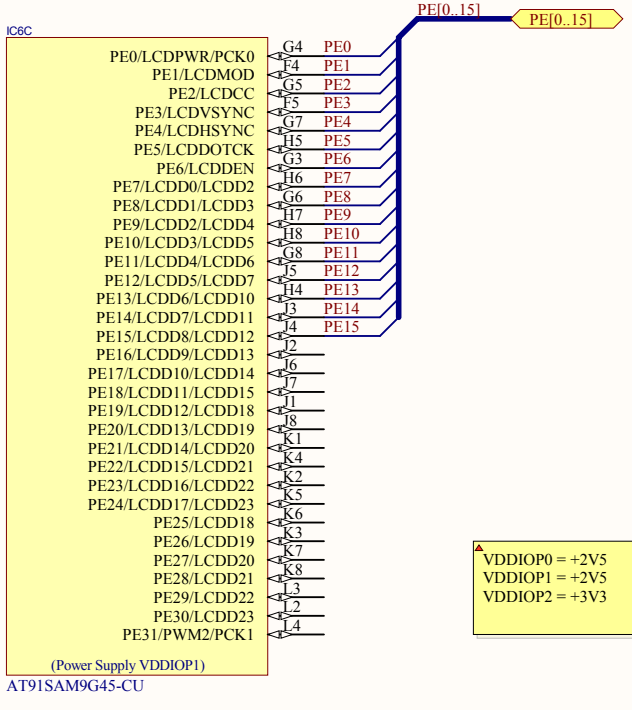
Project:	White Rabbit Switch MCH - mainboard
Sheet:	ARM9 CPU SDRAM and flash memories
Version:	1.1.0
Date:	2009/11/12
Author:	Tomasz Wlostowski
License:	Open Hardware License (OHL)
Company:	CERN BE-CO-HT

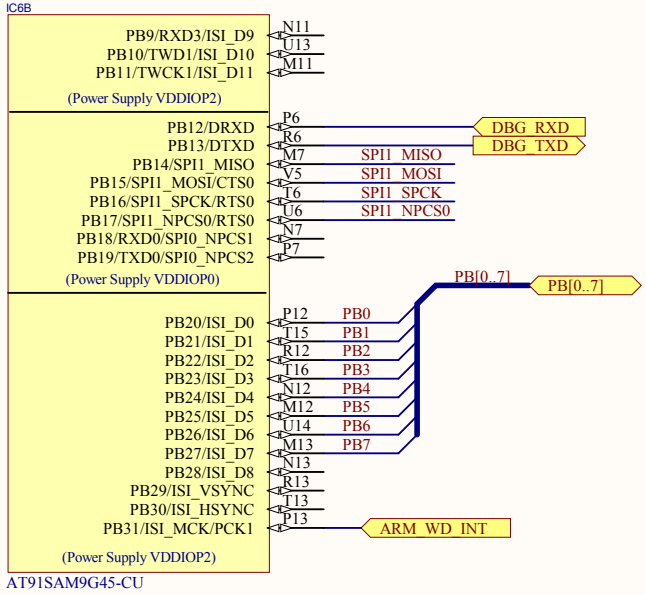












VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3

White Rabbit Switch MCH - mainboard

ARM9 CPU I/O ports, busses and power

Project:

Sheet:

Tomasz Wlostowski

Version:

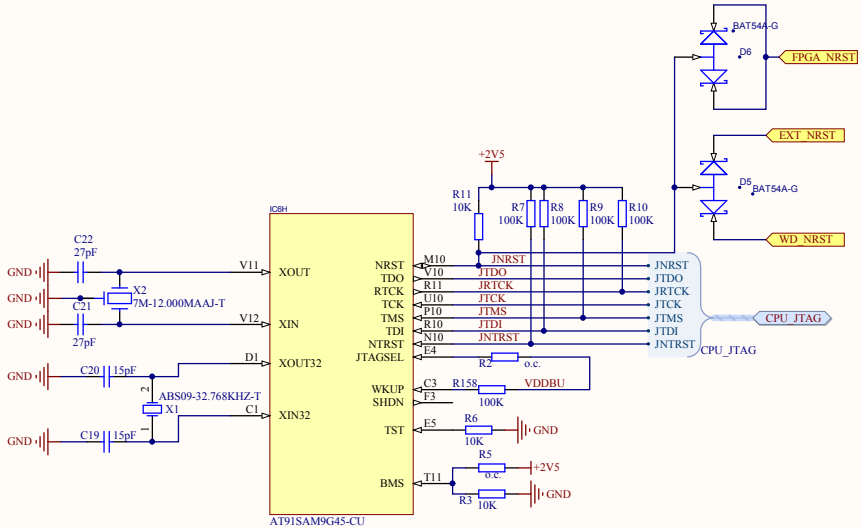
CERN BE-CO-HT

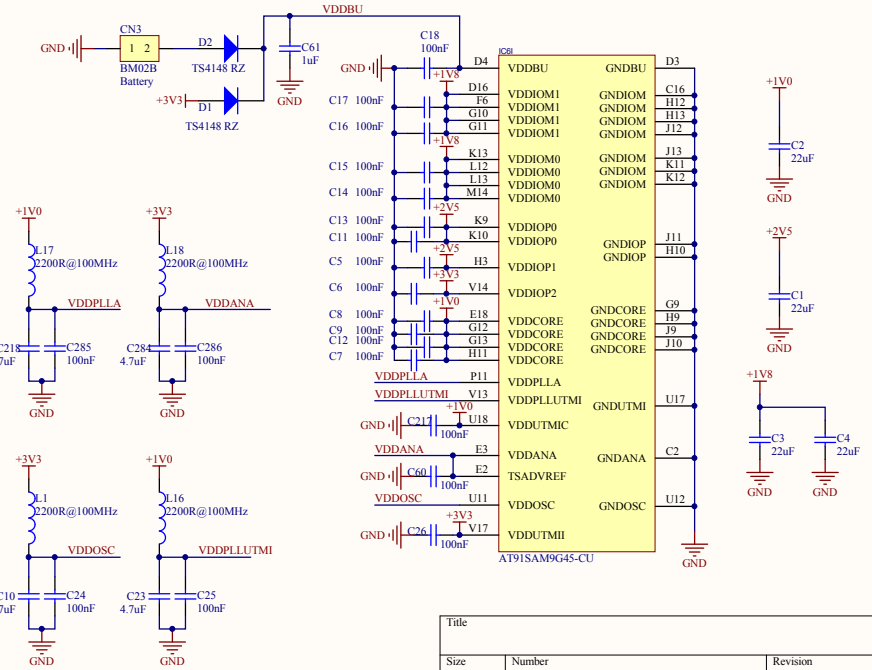
Author:

Date: 2009/11/12

License: Open Hardware License (OHL)

Company:





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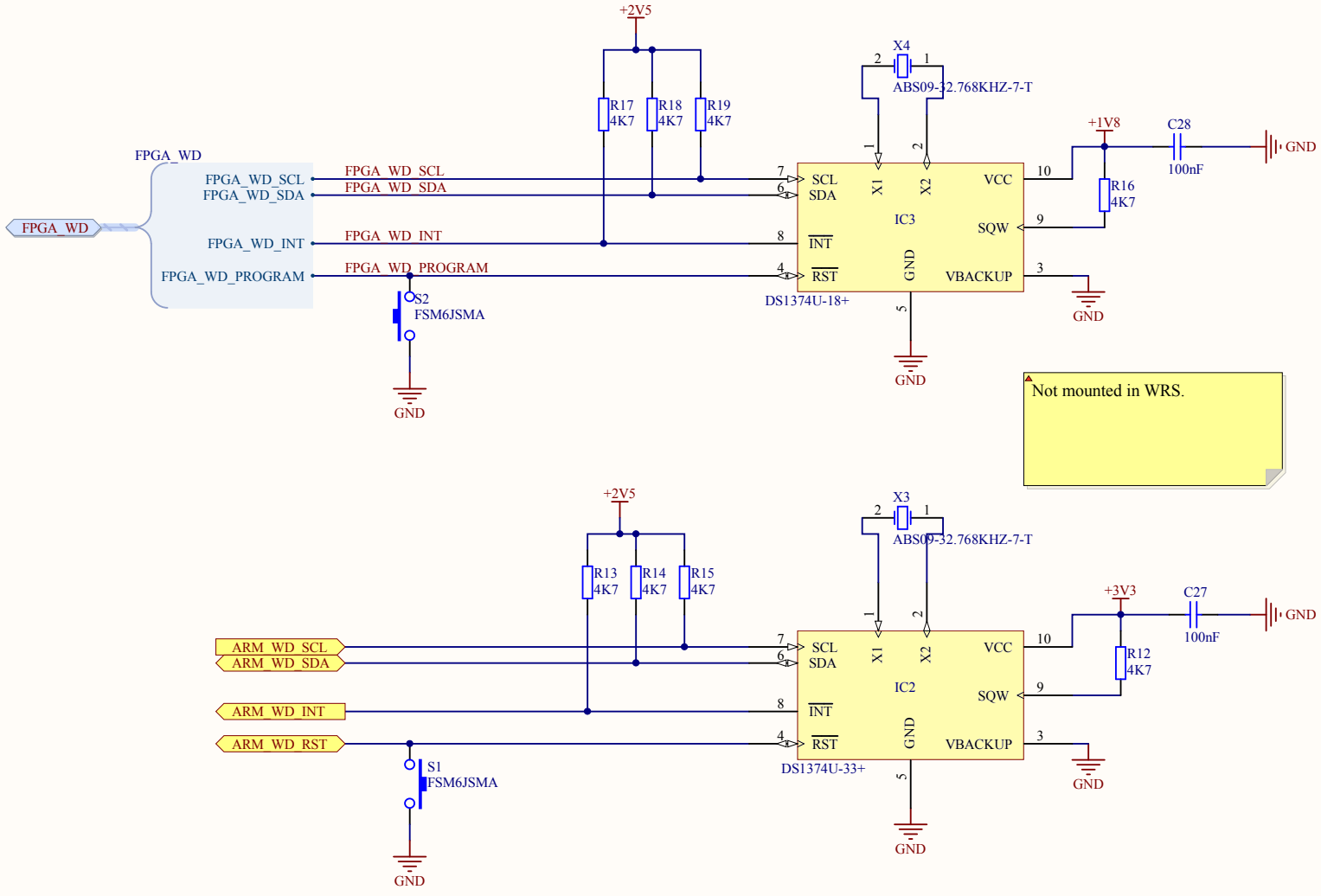

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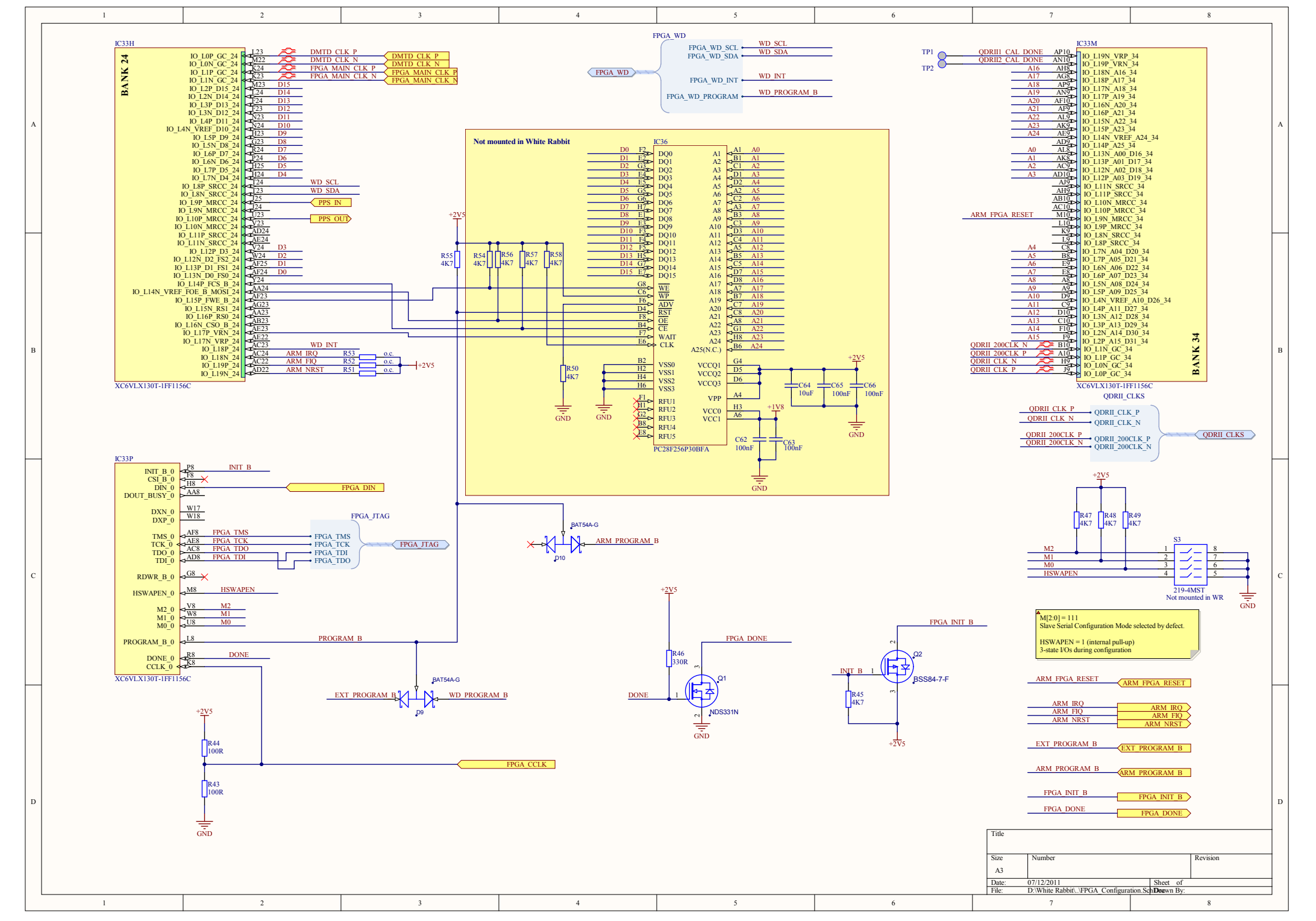
IC33H
BANK 24
XC6VLX130T-1FF1156C
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
WD_INT
ARM_IRQ
ARM_FIQ
ARM_NRST
FPGA_WD
FPGA_WD_SCL
FPGA_WD_SDA
FPGA_WD_INT
FPGA_WD_PROGRAM
Not mounted in White Rabbit
IC36
PC28F256P30BFA
+2V5
+1V8
GND
IC33M
BANK 34
XC6VLX130T-1FF1156C
TP1
TP2
QDRII1_CAL_DONE
QDRII2_CAL_DONE
ARM_FPGA_RESET
QDRII_200CLK_N
QDRII_200CLK_P
QDRII_CLK_N
QDRII_CLK_P
QDRII_CLKS
IC33P
XC6VLX130T-1FF1156C
INIT_B
FPGA_DIN
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
RDWR_B
HSWAPEN
M2
M1
M0
PROGRAM_B
DONE
FPGA_CCLK
BAT54A-G
ARM_PROGRAM_B
EXT_PROGRAM_B
WD_PROGRAM_B
FPGA_DONE
FPGA_INIT_B
BSS84-7-F
NDS331N
S3
219-4MST
Not mounted in WR
M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
Title
Size
A3
Number
Revision
Date: 07/12/2011
Sheet of
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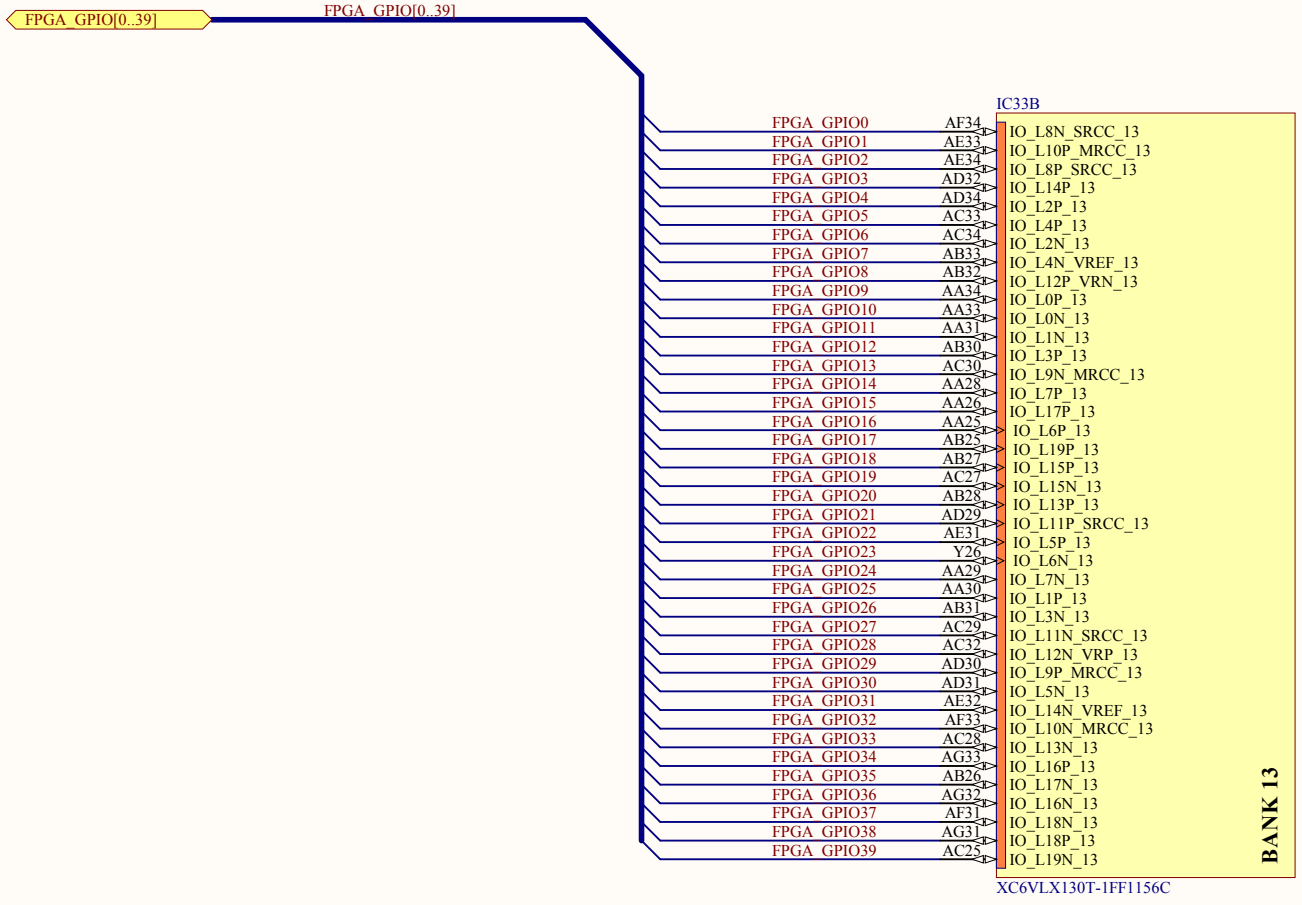
Drawn By:



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Date: 07/12/2011		Sheet of
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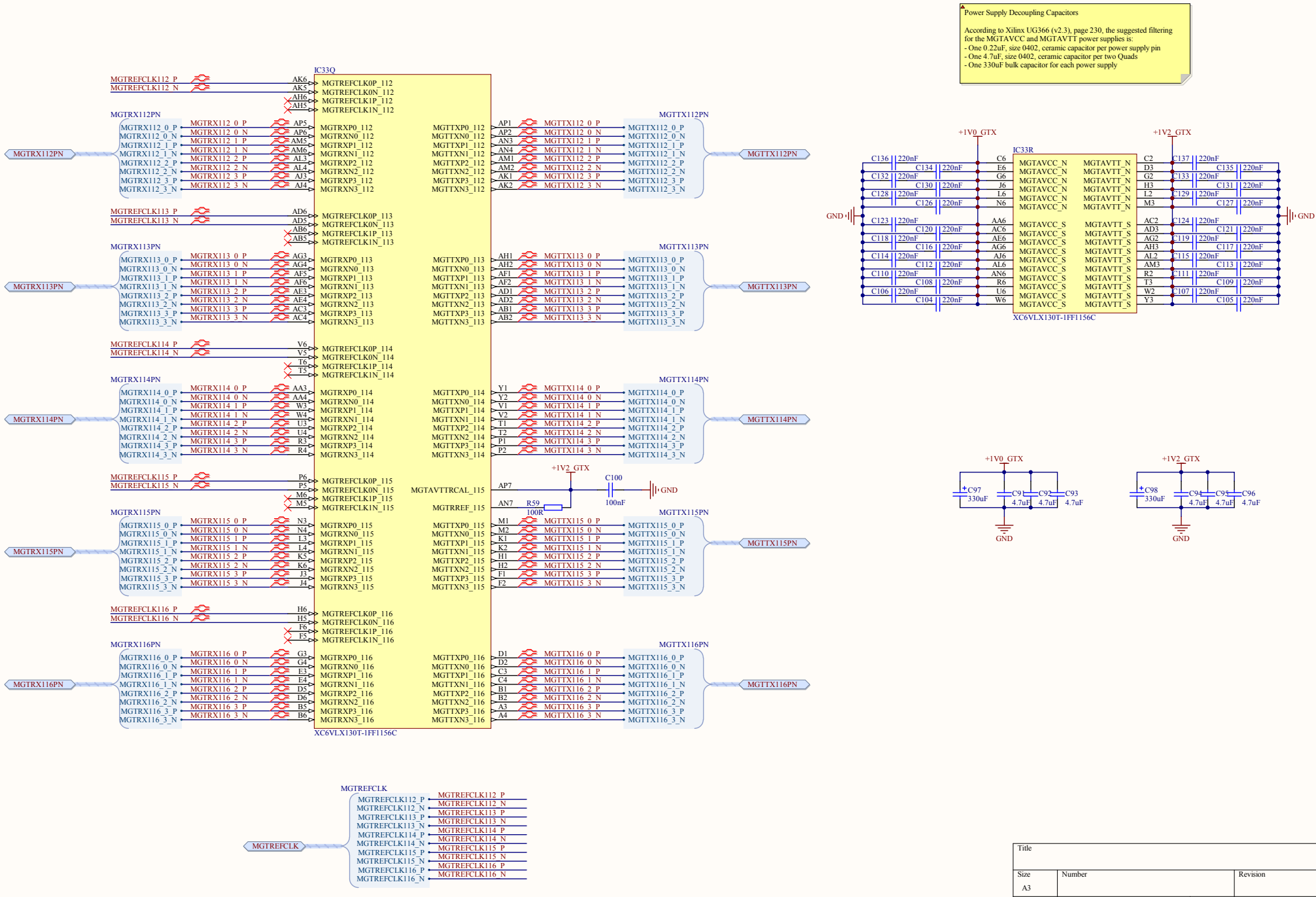

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Size: A3	Number	Revision
Date: 07/12/2011		Sheet of
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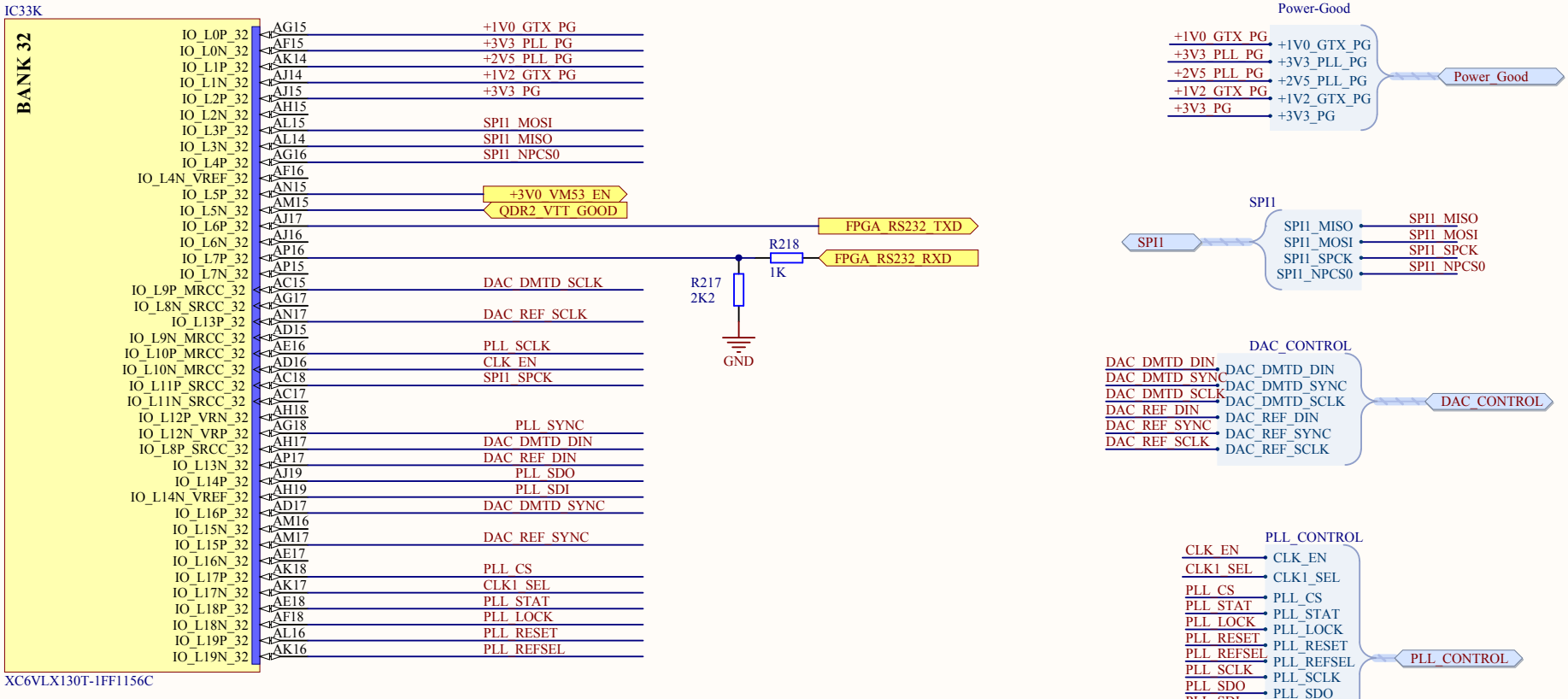

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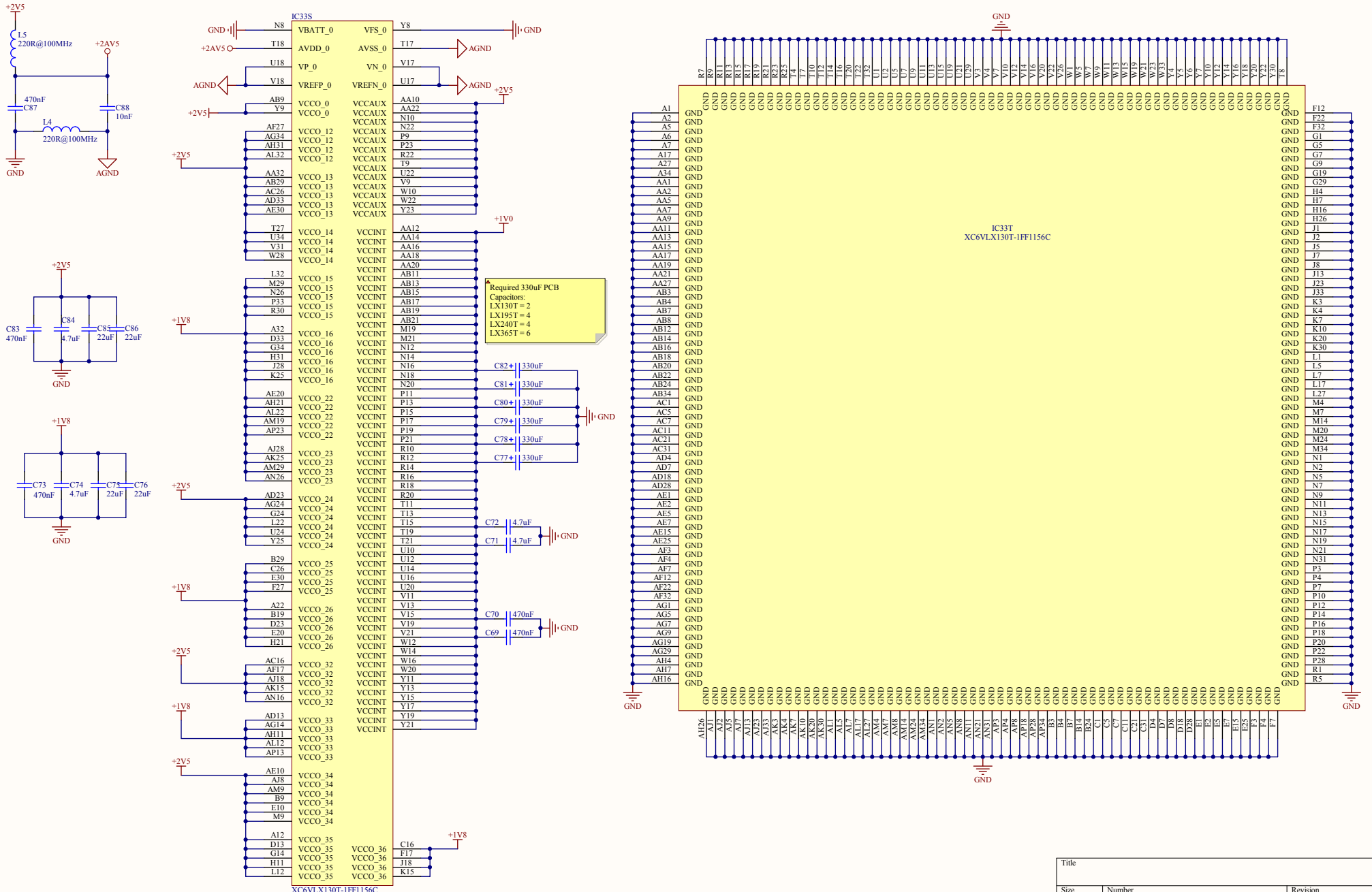
Size: A4	Number	Revision
Date: 07/12/2011	Sheet of	
File: D:\White Rabbit\..\FPGA_Peripherals_Control.SchDoc	Drawn By:	


IC33S
XC6VLX130T-1FF1156C
IC33T
XC6VLX130T-1FF1156C
Required 330uF PCB Capacitors:
LX130T = 2
LX195T = 4
LX240T = 4
LX365T = 6
+2V5
+2AV5
+1V0
+1V8
GND
AGND
L5 220R@100MHz
L4 220R@100MHz
C87 470nF
C88 10nF
C83 470nF
C84 4.7uF
C85 22uF
C86 22uF
C73 470nF
C74 4.7uF
C75 22uF
C76 22uF
C82 330uF
C81 330uF
C80 330uF
C79 330uF
C78 330uF
C77 330uF
C72 4.7uF
C71 4.7uF
C70 470nF
C69 470nF
C16
Title
Size A3
Number
Revision
Date: 07/12/2011
File: D:\White Rabbit\..\FPGA_POWER_DGND.SchDoc
Sheet of
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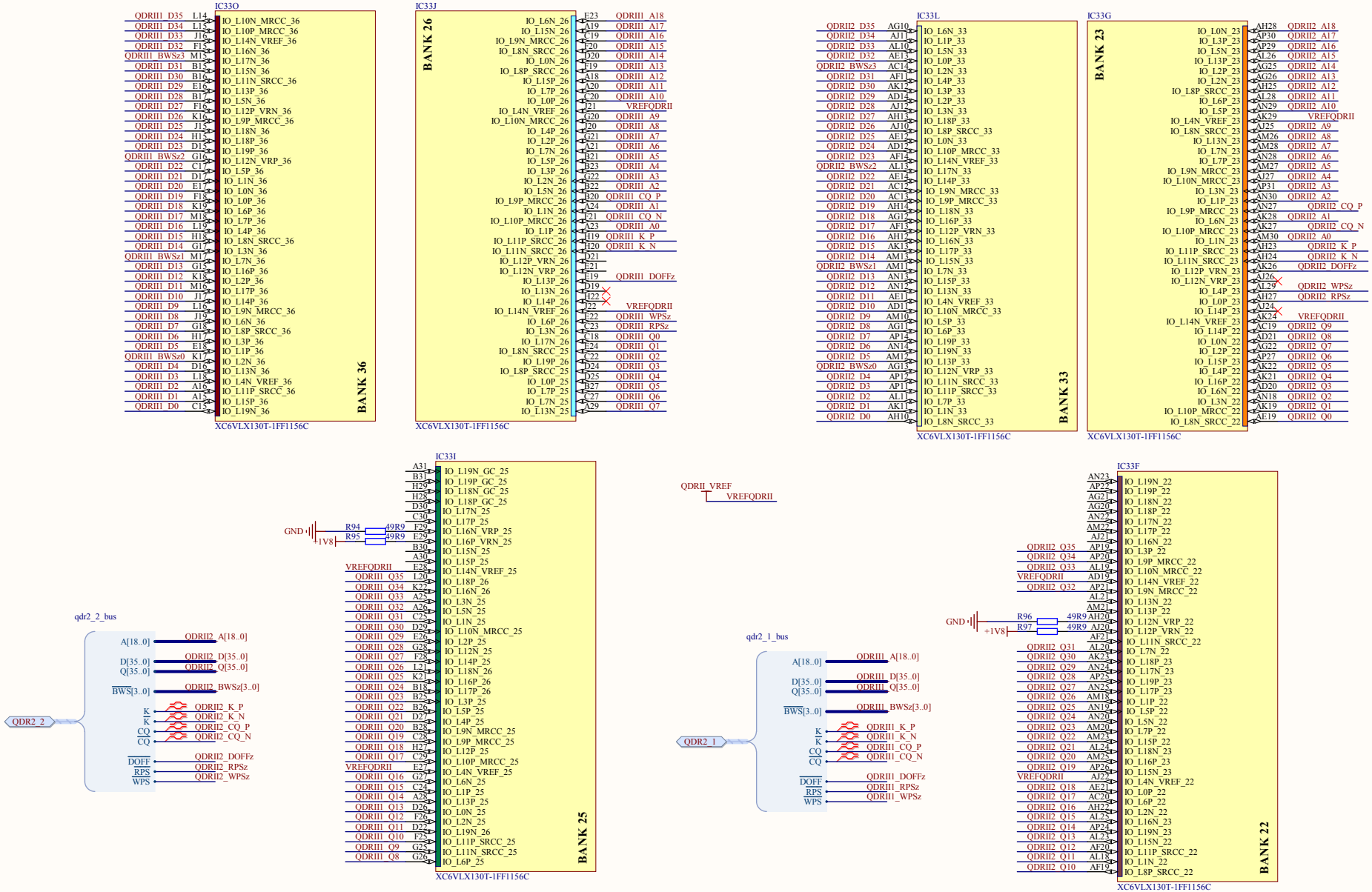

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Size: A3	Number	Revision
Date: 07/12/2011		Sheet of
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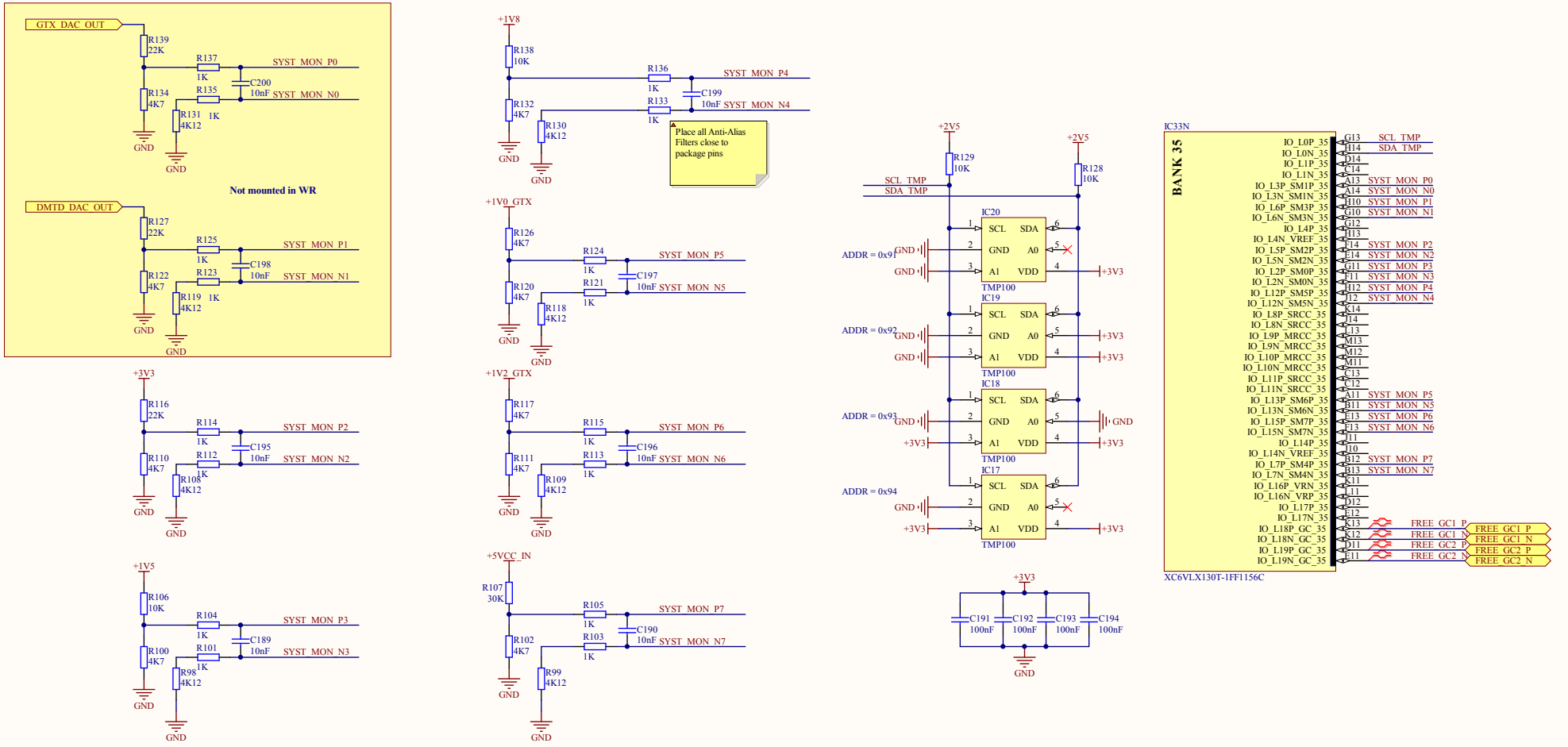
GTX_DAC_OUT
R139 22K
R137 1K
SYST_MON_P0
C200 10nF
SYST_MON_N0
R134 4K7
R135 1K
R131 4K12
GND
Not mounted in WR
DMTD_DAC_OUT
R127 22K
R125 1K
SYST_MON_P1
C198 10nF
SYST_MON_N1
R122 4K7
R123 1K
R119 4K12
+3V3
R116 22K
R114 1K
SYST_MON_P2
C195 10nF
SYST_MON_N2
R110 4K7
R112 1K
R108 4K12
+1V5
R106 10K
R104 1K
SYST_MON_P3
C189 10nF
SYST_MON_N3
R100 4K7
R101 1K
R98 4K12
+1V8
R138 10K
R136 1K
SYST_MON_P4
C199 10nF
SYST_MON_N4
R132 4K7
R133 1K
R130 4K12
Place all Anti-Alias Filters close to package pins
+1V0_GTX
R126 4K7
R124 1K
SYST_MON_P5
C197 10nF
SYST_MON_N5
R120 4K7
R121 1K
R118 4K12
+1V2_GTX
R117 4K7
R115 1K
SYST_MON_P6
C196 10nF
SYST_MON_N6
R111 4K7
R113 1K
R109 4K12
+5VCC_IN
R107 30K
R105 1K
SYST_MON_P7
C190 10nF
SYST_MON_N7
R102 4K7
R103 1K
R99 4K12
+2V5
R129 10K
R128 10K
SCL_TMP
SDA_TMP
IC20
IC19
IC18
IC17
SCL
SDA
GND
A0
A1
VDD
TMP100
ADDR = 0x91
ADDR = 0x92
ADDR = 0x93
ADDR = 0x94
+3V3
C191 100nF
C192 100nF
C193 100nF
C194 100nF
IC33N
BANK 35
IO_L0P_35
IO_L0N_35
IO_L1P_35
IO_L1N_35
IO_L3P_SM1P_35
IO_L3N_SM1N_35
IO_L6P_SM3P_35
IO_L6N_SM3N_35
IO_L4P_35
IO_L4N_VREF_35
IO_L5P_SM2P_35
IO_L5N_SM2N_35
IO_L2P_SM0P_35
IO_L2N_SM0N_35
IO_L12P_SM5P_35
IO_L12N_SM5N_35
IO_L8P_SRCC_35
IO_L8N_SRCC_35
IO_L9P_MRCC_35
IO_L9N_MRCC_35
IO_L10P_MRCC_35
IO_L10N_MRCC_35
IO_L11P_SRCC_35
IO_L11N_SRCC_35
IO_L13P_SM6P_35
IO_L13N_SM6N_35
IO_L15P_SM7P_35
IO_L15N_SM7N_35
IO_L14P_35
IO_L14N_VREF_35
IO_L7P_SM4P_35
IO_L7N_SM4N_35
IO_L16P_VRN_35
IO_L16N_VRP_35
IO_L17P_35
IO_L17N_35
IO_L18P_GC_35
IO_L18N_GC_35
IO_L19P_GC_35
IO_L19N_GC_35
G13 SCL_TMP
H14 SDA_TMP
A13 SYST_MON_P0
A14 SYST_MON_N0
H10 SYST_MON_P1
G10 SYST_MON_N1
F14 SYST_MON_P2
E14 SYST_MON_N2
G11 SYST_MON_P3
F11 SYST_MON_N3
H12 SYST_MON_P4
J12 SYST_MON_N4
A11 SYST_MON_P5
B11 SYST_MON_N5
E13 SYST_MON_P6
F13 SYST_MON_N6
B12 SYST_MON_P7
B13 SYST_MON_N7
FREE_GC1_P
FREE_GC1_N
FREE_GC2_P
FREE_GC2_N
XC6VLX130T-1FF1156C
Title
Size A3
Number
Revision
Date: 07/12/2011
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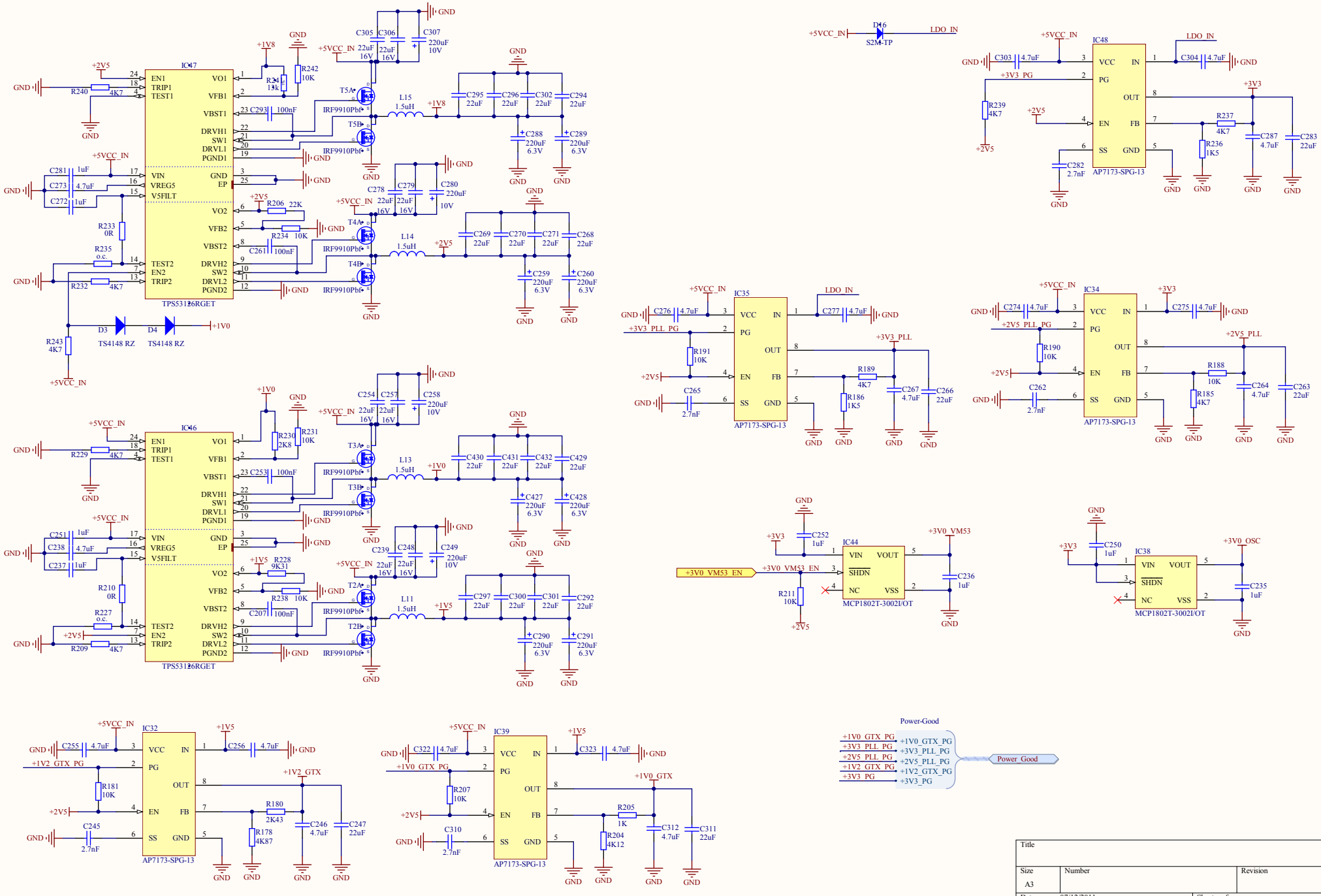
IC47
TPS53126RGET
IC46
TPS53126RGET
D16
S2M-TP
LDO_IN
IC48
AP7173-SPG-13
IC35
AP7173-SPG-13
IC34
AP7173-SPG-13
IC44
MCP1802T-3002I/OT
IC38
MCP1802T-3002I/OT
IC32
AP7173-SPG-13
IC39
AP7173-SPG-13
D3
TS4148 RZ
D4
TS4148 RZ
Power-Good
Power_Good
Title
Size
A3
Number
Revision
Date:
07/12/2011
Sheet of
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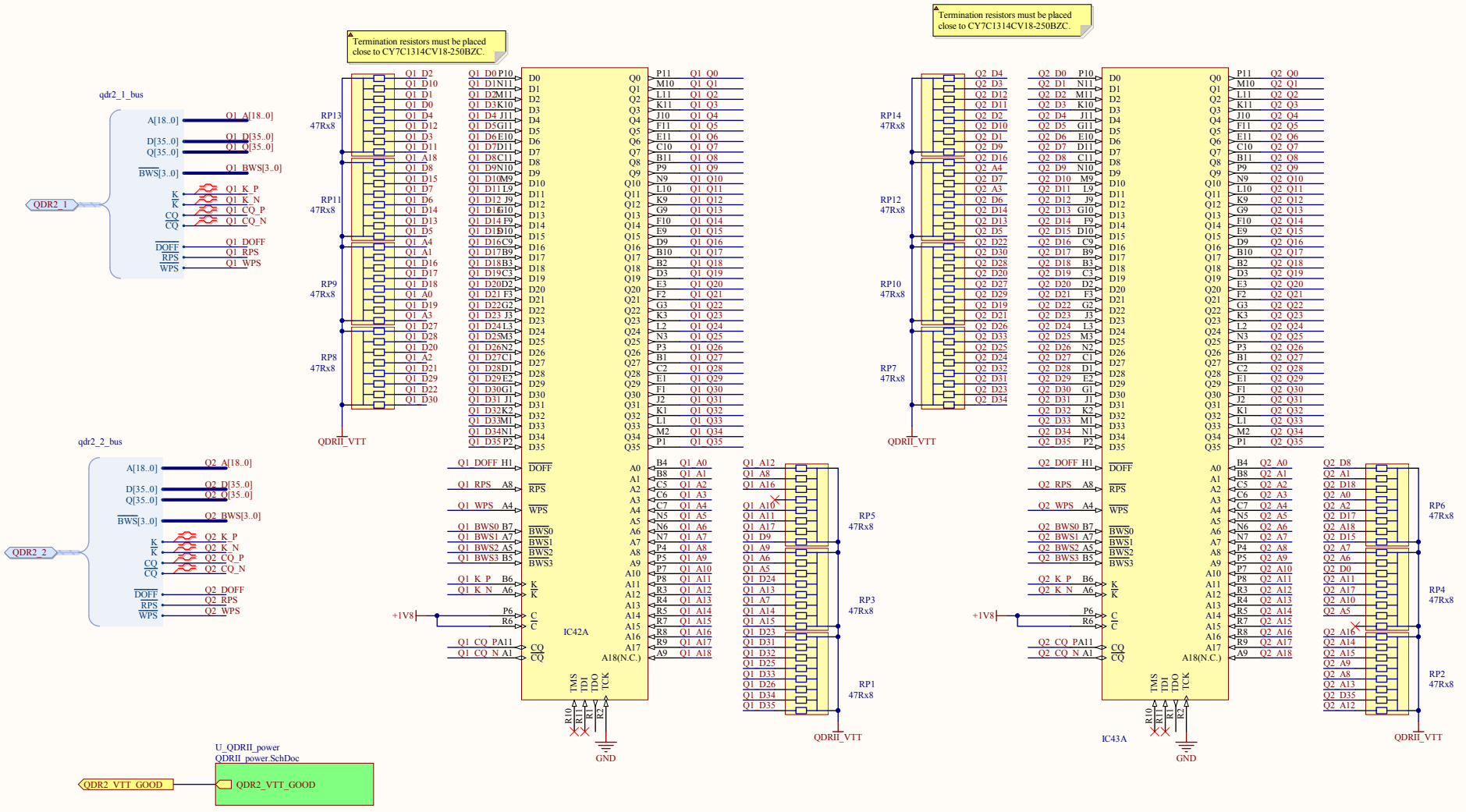

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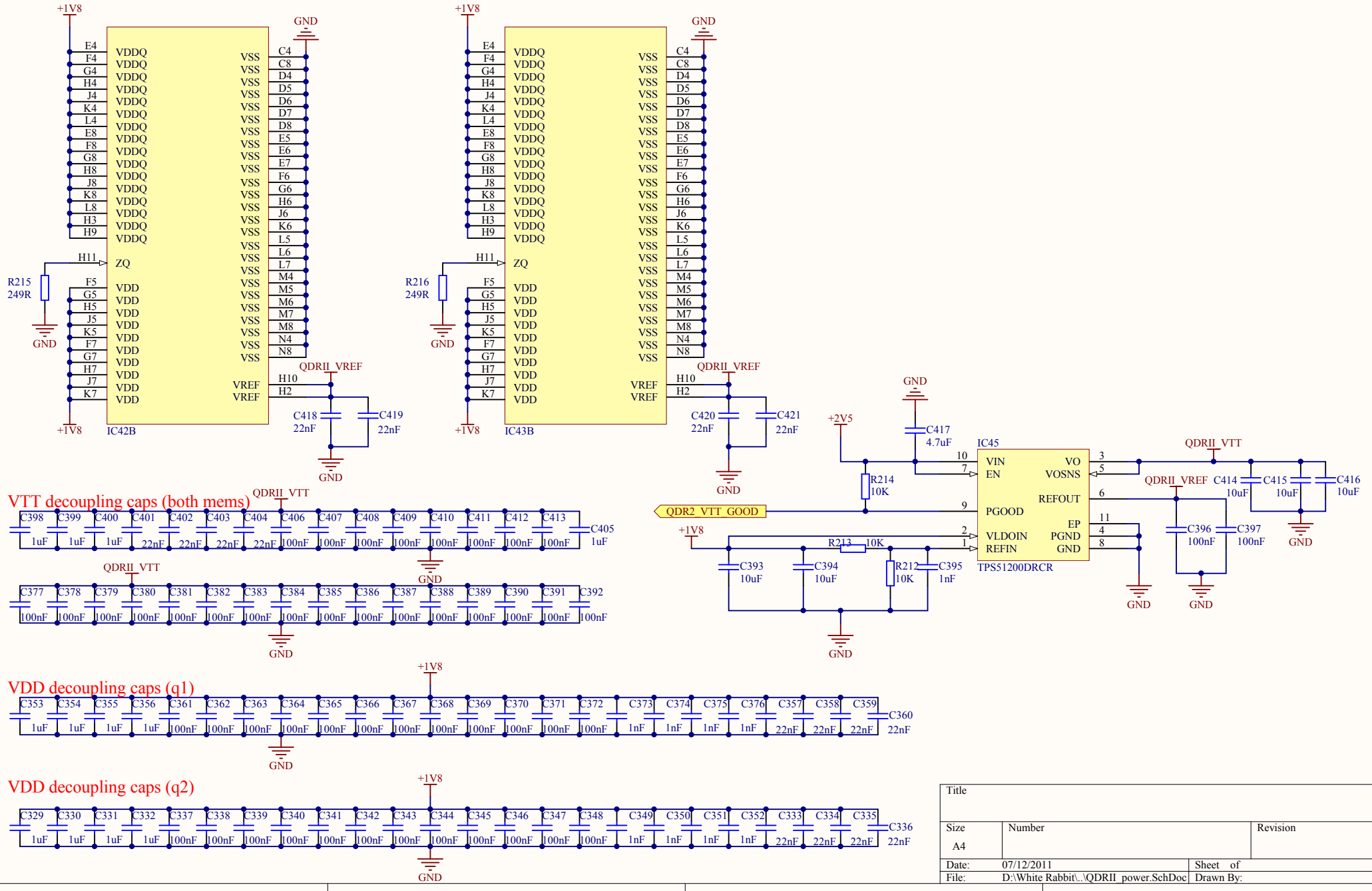
Size A3	Number		Revision
Date: 07/12/2011		Sheet of	
File: D:\White Rabbit\..\QDRII_mem.SchDoc		Drawn By:	


+1V8
GND
IC42B
IC43B
R215 249R
R216 249R
ZQ
VDDQ
VDD
VSS
VREF
QDRII_VREF
C418 22nF
C419 22nF
C420 22nF
C421 22nF
IC45
TPS51200DRCR
VIN
EN
PGOOD
VLDOIN
REFIN
VO
VOSNS
REFOUT
EP
PGND
+2V5
C417 4.7uF
R214 10K
R213 10K
R212 10K
C393 10uF
C394 10uF
C395 1nF
C396 100nF
C397 100nF
C414 10uF
C415 10uF
C416 10uF
QDR2_VTT_GOOD
QDRII_VTT
VTT decoupling caps (both mems)
C398 C399 C400 C401 C402 C403 C404 C406 C407 C408 C409 C410 C411 C412 C413 C405
1uF 1uF 1uF 22nF 22nF 22nF 22nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1uF
C377 C378 C379 C380 C381 C382 C383 C384 C385 C386 C387 C388 C389 C390 C391 C392
100nF
VDD decoupling caps (q1)
C353 C354 C355 C356 C361 C362 C363 C364 C365 C366 C367 C368 C369 C370 C371 C372 C373 C374 C375 C376 C357 C358 C359 C360
1uF 1uF 1uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1nF 1nF 1nF 1nF 22nF 22nF 22nF 22nF
VDD decoupling caps (q2)
C329 C330 C331 C332 C337 C338 C339 C340 C341 C342 C343 C344 C345 C346 C347 C348 C349 C350 C351 C352 C333 C334 C335 C336
1uF 1uF 1uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1nF 1nF 1nF 1nF 22nF 22nF 22nF 22nF
Title
Size A4
Number
Revision
Date: 07/12/2011
Sheet of
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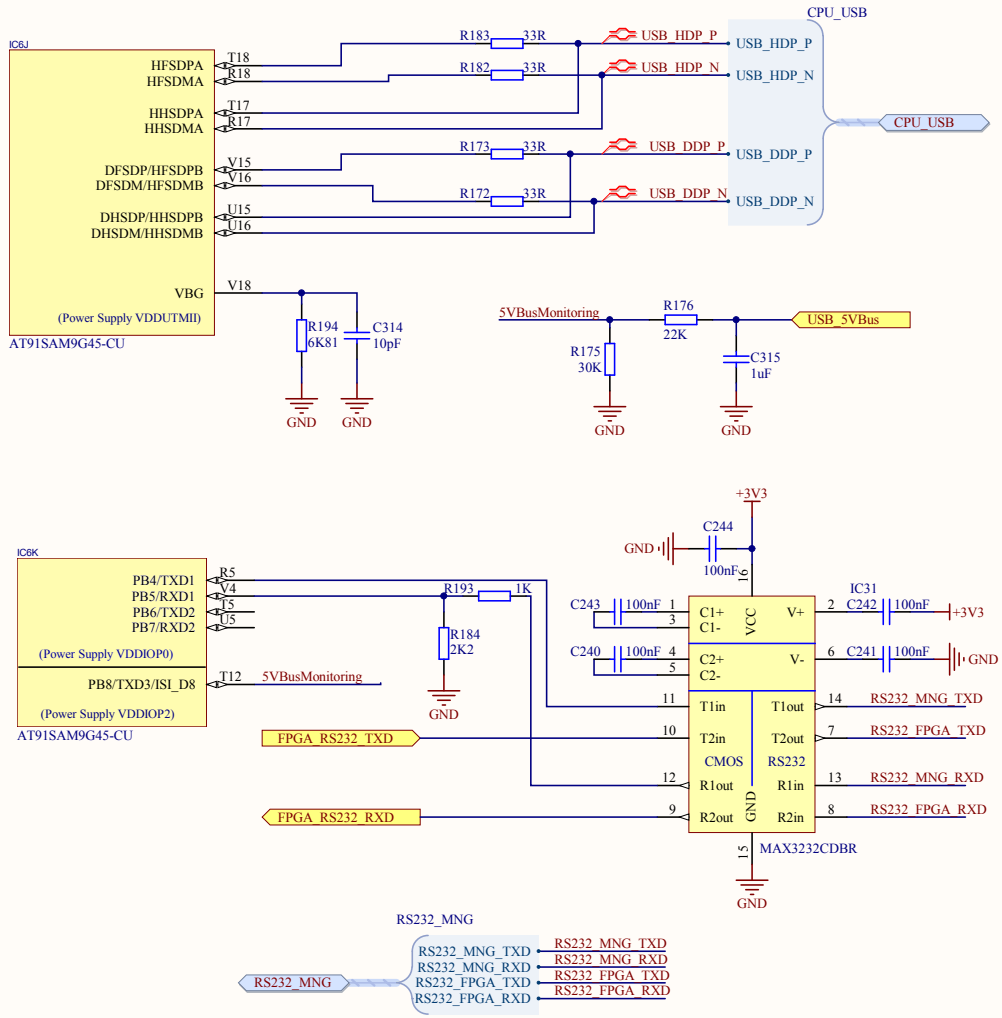
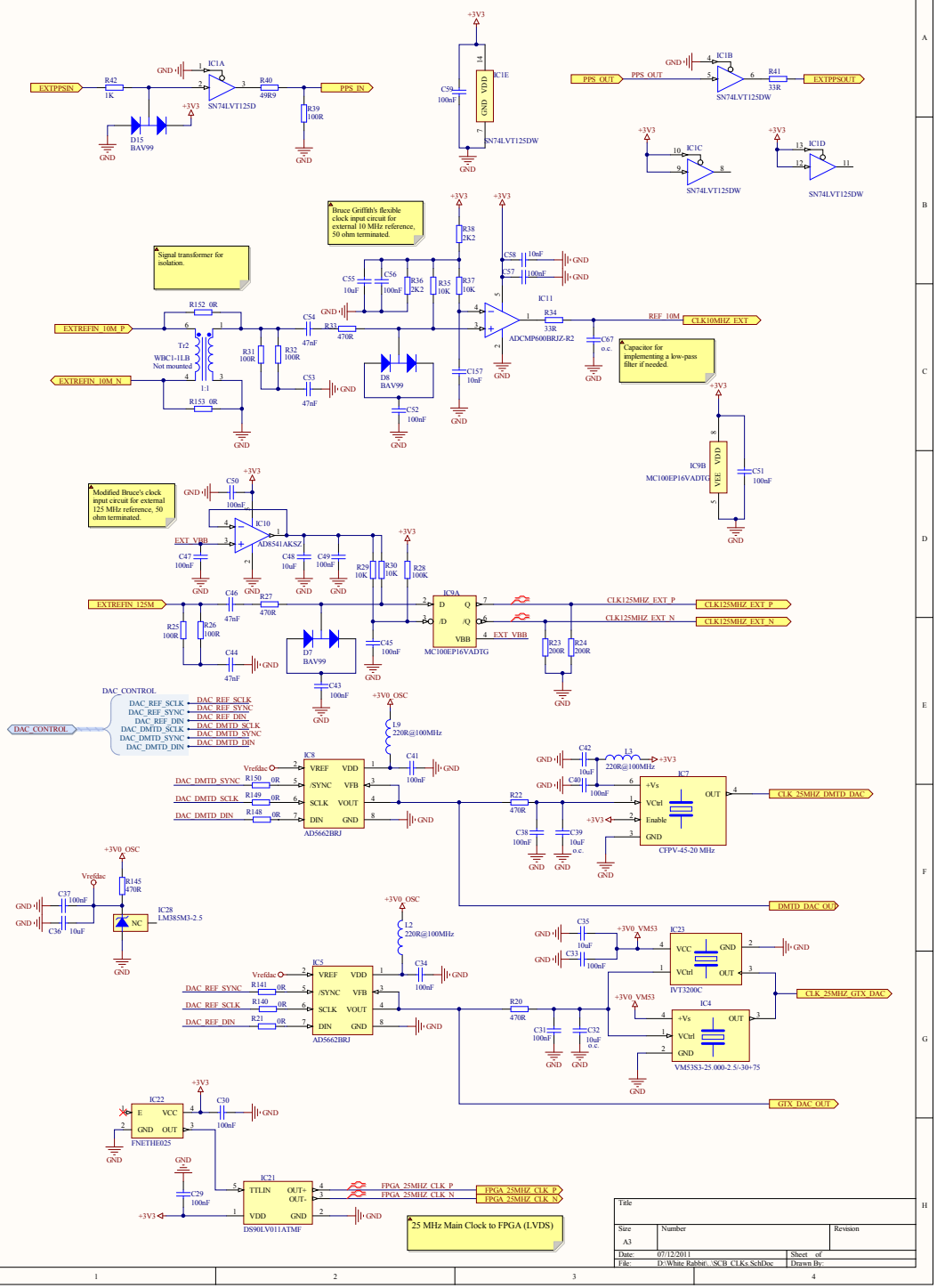


Title	White Rabbit Switch MCH - clocking mezzanine RS232 port	
Size: A	Number:	Revision:
Date: 07/12/2011	Sheet of	
File: D:\White Rabbit\..\RS232_and_USB_ports.SchDoc	Drawn By:	


EXTPPSIN
PPS_IN
SN74LVT125D
SN74LVT125DW
PPS_OUT
EXTPPSOUT
Bruce Griffith's flexible clock input circuit for external 10 MHz reference, 50 ohm terminated.
Signal transformer for isolation.
EXTREFIN_10M_P
EXTREFIN_10M_N
WBC1-1LB
Not mounted
ADCMP600BRJZ-R2
REF_10M
CLK10MHZ_EXT
Capacitor for implementing a low-pass filter if needed.
MC100EP16VADTG
Modified Bruce's clock input circuit for external 125 MHz reference, 50 ohm terminated.
AD8541AKSZ
EXTREFIN_125M
CLK125MHZ_EXT_P
CLK125MHZ_EXT_N
DAC_CONTROL
DAC_REF_SCLK
DAC_REF_SYNC
DAC_REF_DIN
DAC_DMTD_SCLK
DAC_DMTD_SYNC
DAC_DMTD_DIN
AD5662BRJ
CFPV-45-20 MHz
CLK_25MHZ_DMTD_DAC
DMTD_DAC_OUT
LM385M3-2.5
IVT3200C
CLK_25MHZ_GTX_DAC
VM53I3-25 000-2.5/-30+75
GTX_DAC_OUT
FNETHE025
DS90LV011ATMF
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
25 MHz Main Clock to FPGA (LVDS)
Title
Size
A3
Number
Revision
Date: 07/12/2011
Sheet of
File: D:\White Rabbit\...\SCB_CLKs.SchDoc
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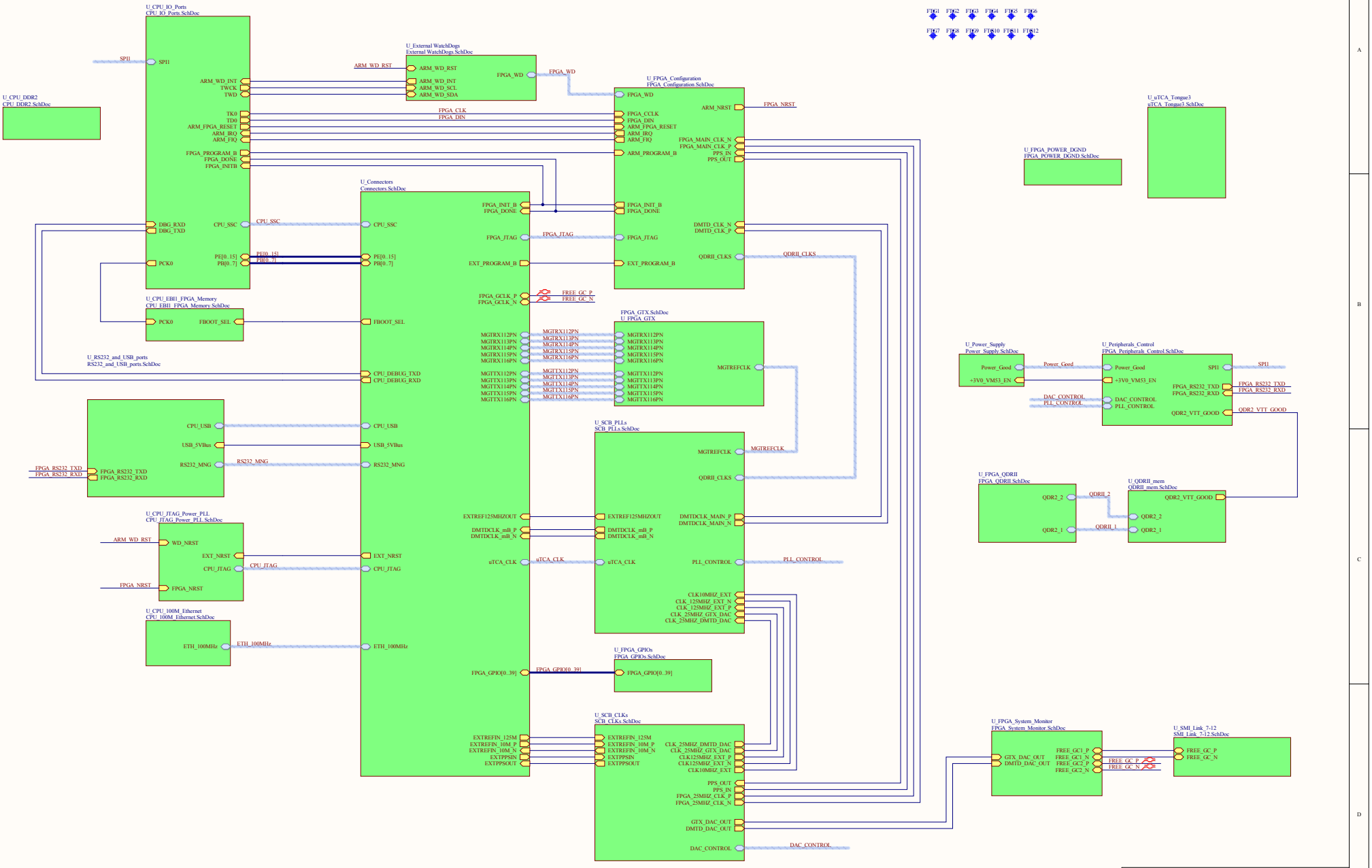
U_CPU_IO_Ports
CPU_IO_Ports.SchDoc
SPI1
ARM_WD_INT
TWCK
TWD
TDI
ARM_FPGA_RESET
ARM_IRQ
ARM_FIQ
FPGA_PROGRAM_B
FPGA_DONE
FPGA_INITB
DBG_RXD
DBG_TXD
CPU_SSC
PE[0..15]
PB[0..7]
PCK0
U_CPU_DDR2
CPU_DDR2.SchDoc
U_External WatchDogs
External WatchDogs.SchDoc
ARM_WD_RST
ARM_WD_INT
ARM_WD_SCL
ARM_WD_SDA
FPGA_WD
FPGA_CLK
FPGA_DIN
U_FPGA_Configuration
FPGA_Configuration.SchDoc
FPGA_WD
ARM_NRST
FPGA_NRST
FPGA_CCLK
ARM_FPGA_RESET
FPGA_MAIN_CLK_N
FPGA_MAIN_CLK_P
PPS_IN
PPS_OUT
FPGA_INIT_B
FPGA_DONE
FPGA_JTAG
EXT_PROGRAM_B
DMTD_CLK_N
DMTD_CLK_P
QDRII_CLKS
U_uTCA_Tongue3
uTCA_Tongue3.SchDoc
U_FPGA_POWER_DGND
FPGA_POWER_DGND.SchDoc
U_Connectors
Connectors.SchDoc
FPGA_GCLK_P
FPGA_GCLK_N
FREE_GC_P
FREE_GC_N
U_CPU_EBI_FPGA_Memory
CPU_EBI_FPGA_Memory.SchDoc
FBOOT_SEL
FPGA_GTX.SchDoc
U_FPGA_GTX
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
MGTREFCLK
U_RS232_and_USB_ports
RS232_and_USB_ports.SchDoc
CPU_DEBUG_TXD
CPU_DEBUG_RXD
CPU_USB
USB_5VBus
RS232_MNG
FPGA_RS232_TXD
FPGA_RS232_RXD
U_SCB_PLLs
SCB_PLLs.SchDoc
QDRII_CLKS
EXTREF125MHZOUT
DMTDCLK_mB_P
DMTDCLK_mB_N
DMTDCLK_MAIN_P
DMTDCLK_MAIN_N
uTCA_CLK
PLL_CONTROL
CLK10MHZ_EXT
CLK_125MHZ_EXT_N
CLK_125MHZ_EXT_P
CLK_25MHZ_GTX_DAC
CLK_25MHZ_DMTD_DAC
U_Power_Supply
Power_Supply.SchDoc
Power_Good
+3V0_VM53_EN
U_Peripherals_Control
FPGA_Peripherals_Control.SchDoc
SPI1
FPGA_RS232_TXD
FPGA_RS232_RXD
DAC_CONTROL
PLL_CONTROL
QDR2_VTT_GOOD
U_FPGA_QDRII
FPGA_QDRII.SchDoc
QDR2_2
QDR2_1
QDRII_2
QDRII_1
U_QDRII_mem
QDRII_mem.SchDoc
U_CPU_JTAG_Power_PLL
CPU_JTAG_Power_PLL.SchDoc
ARM_WD_RST
WD_NRST
EXT_NRST
CPU_JTAG
FPGA_NRST
U_CPU_100M_Ethernet
CPU_100M_Ethernet.SchDoc
ETH_100MHz
U_FPGA_GPIOs
FPGA_GPIOs.SchDoc
FPGA_GPIO[0..39]
U_SCB_CLKs
SCB_CLKs.SchDoc
EXTREFIN_125M
EXTREFIN_10M_P
EXTREFIN_10M_N
EXTPPSIN
EXTPPSOUT
CLK_25MHZ_DMTD_DAC
CLK_25MHZ_GTX_DAC
CLK125MHZ_EXT_P
CLK125MHZ_EXT_N
CLK10MHZ_EXT
PPS_OUT
PPS_IN
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
GTX_DAC_OUT
DMTD_DAC_OUT
DAC_CONTROL
U_FPGA_System_Monitor
FPGA_System_Monitor.SchDoc
FREE_GC1_P
FREE_GC1_N
FREE_GC2_P
FREE_GC2_N
U_SMI_Link_7-12
SMI_Link_7-12.SchDoc
FTE21
FTE22
FTE23
FTE24
FTE25
FTE26
FTE27
FTE28
FTE29
FTE30
FTE31
FTE32
Title
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A2
Number
Revision
Date:
07/12/2011
Sheet of
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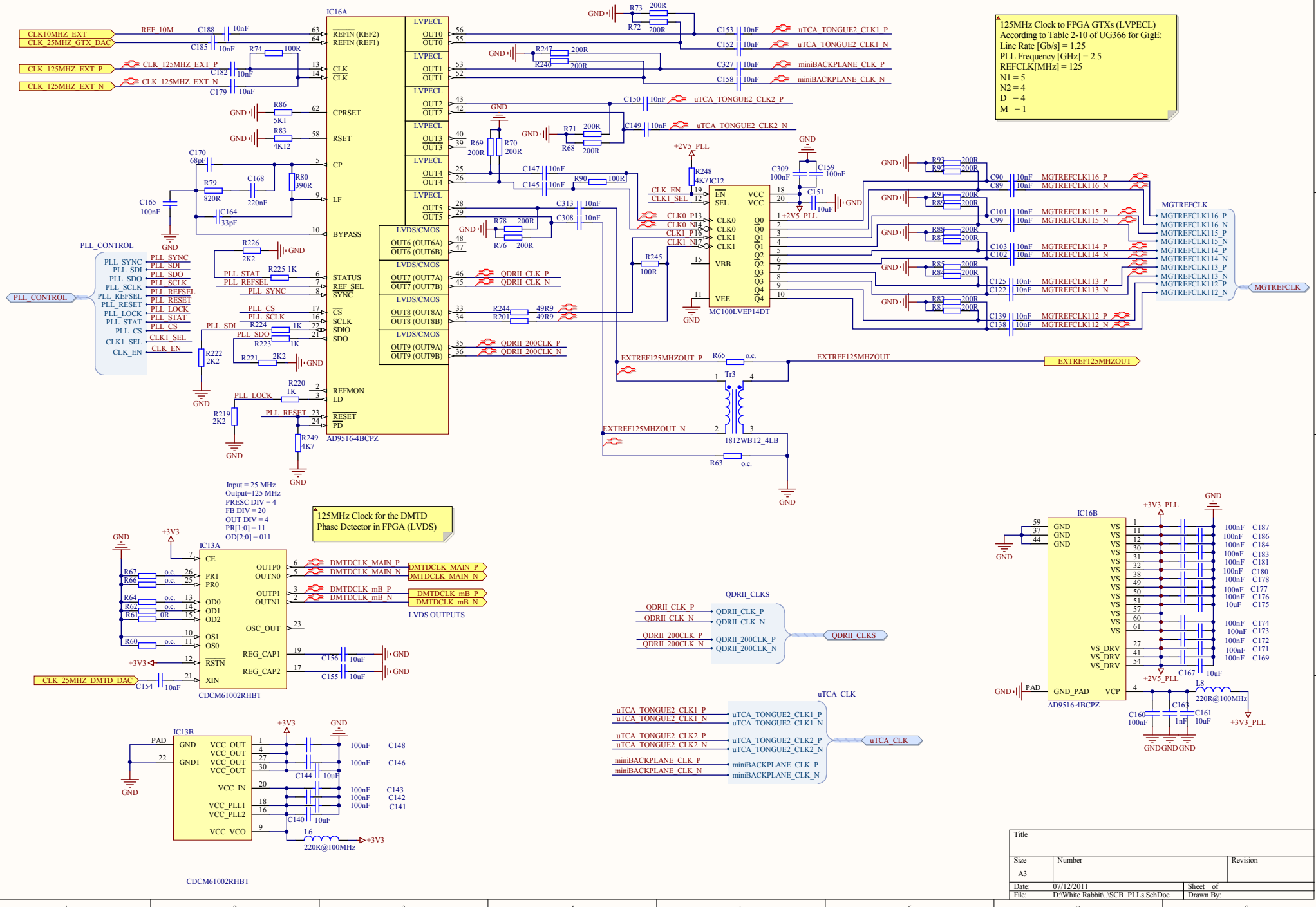
125MHz Clock to FPGA GTXs (LVPECL)
According to Table 2-10 of UG366 for GigE:
Line Rate [Gb/s] = 1.25
PLL Frequency [GHz] = 2.5
REFCLK[MHz] = 125
N1 = 5
N2 = 4
D = 4
M = 1
IC16A
AD9516-4BCPZ
PLL_CONTROL
MC100LVEP14DT
1812WBT2_4LB
MGTREFCLK
EXTREF125MHZOUT
125MHz Clock for the DMTD
Phase Detector in FPGA (LVDS)
Input = 25 MHz
Output=125 MHz
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
PR[1:0] = 11
OD[2:0] = 011
IC13A
CDCM61002RHBT
LVDS OUTPUTS
IC13B
CDCM61002RHBT
QDRII_CLKS
uTCA_CLK
IC16B
AD9516-4BCPZ
Title
Size
A3
Number
Revision
Date: 07/12/2011
File: D:\White Rabbit\..\SCB_PLLs.SchDoc
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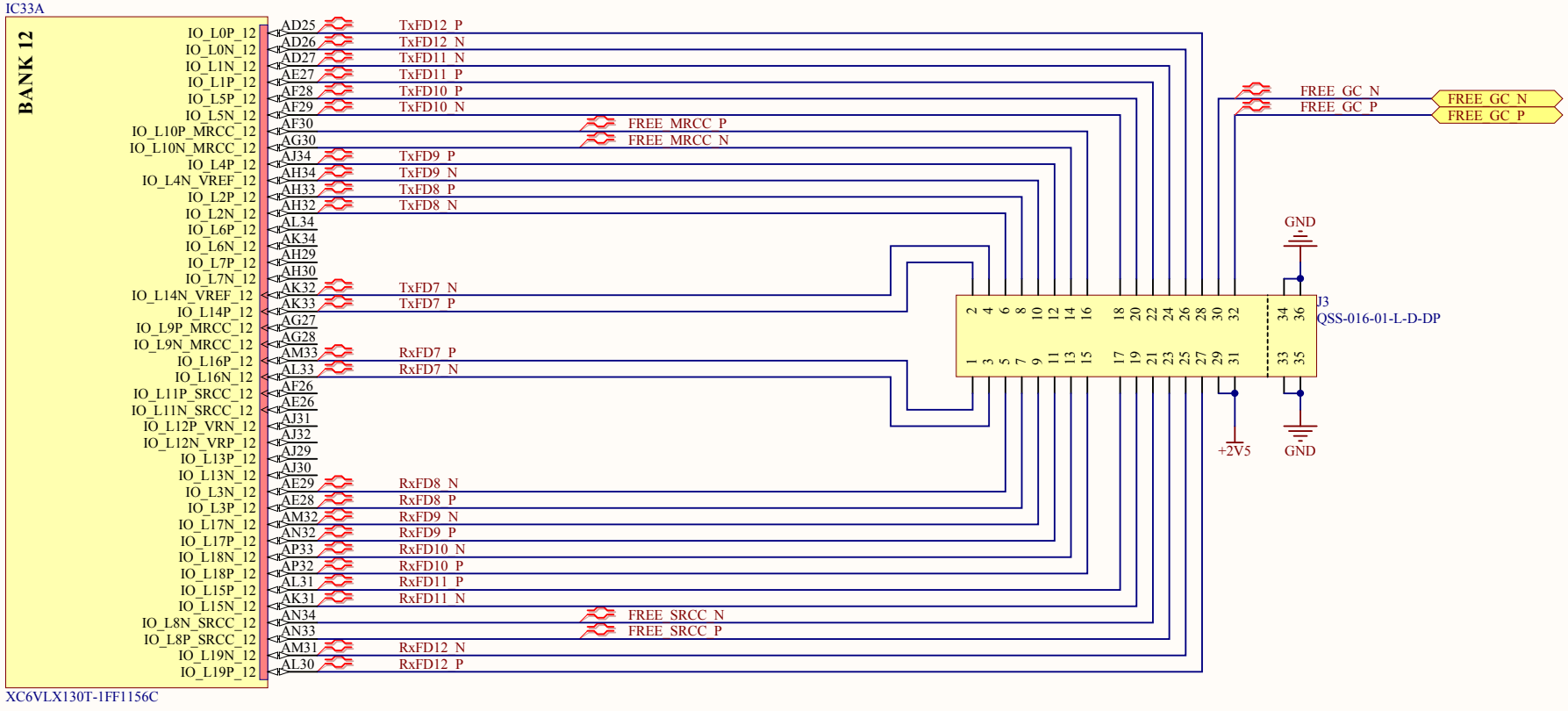

Title		
Size A4	Number	Revision
Date: 07/12/2011	Sheet of	
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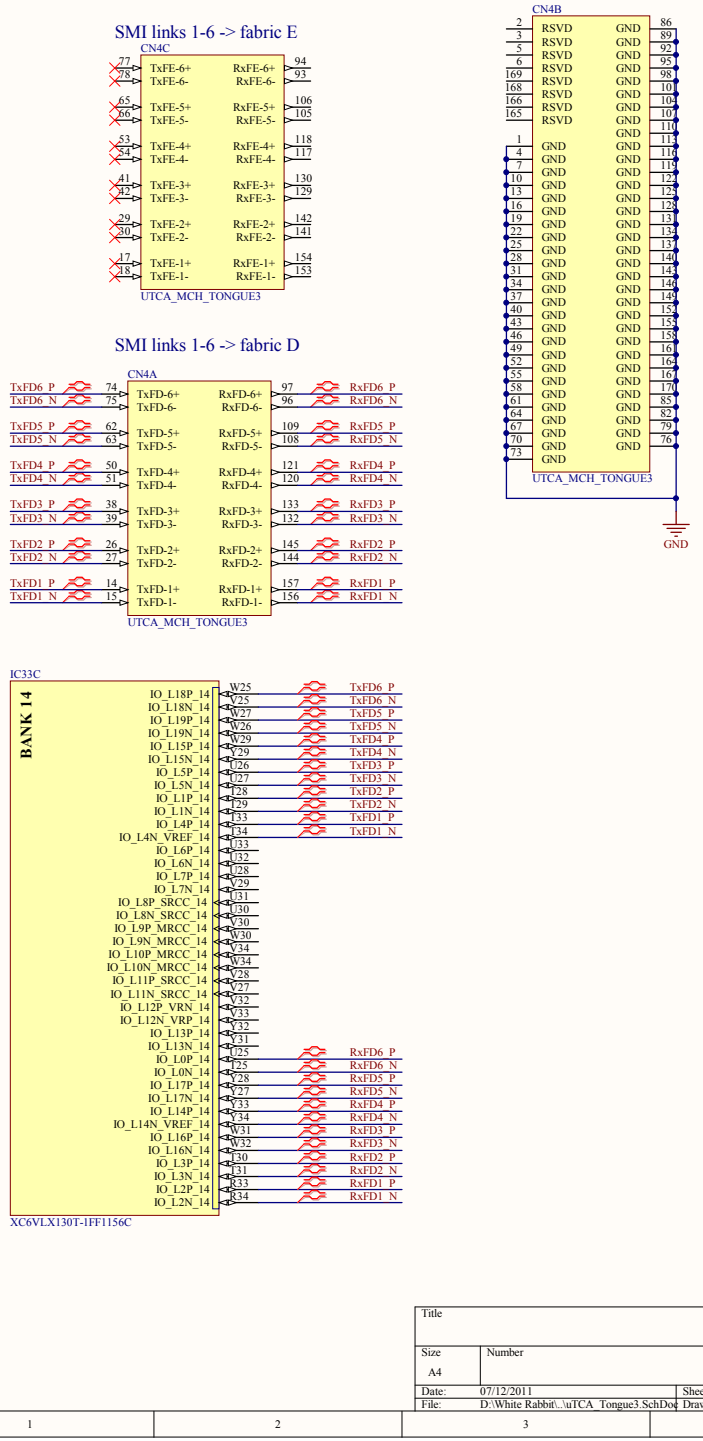
SMI links 1-6 -> fabric E
CN4C
77 TxFE-6+ RxFE-6+ 94
78 TxFE-6- RxFE-6- 93
65 TxFE-5+ RxFE-5+ 106
66 TxFE-5- RxFE-5- 105
53 TxFE-4+ RxFE-4+ 118
54 TxFE-4- RxFE-4- 117
41 TxFE-3+ RxFE-3+ 130
42 TxFE-3- RxFE-3- 129
29 TxFE-2+ RxFE-2+ 142
30 TxFE-2- RxFE-2- 141
17 TxFE-1+ RxFE-1+ 154
18 TxFE-1- RxFE-1- 153
UTCA_MCH_TONGUE3
SMI links 1-6 -> fabric D
CN4A
TxFD6_P 74 TxFD-6+ RxFD-6+ 97 RxFD6_P
TxFD6_N 75 TxFD-6- RxFD-6- 96 RxFD6_N
TxFD5_P 62 TxFD-5+ RxFD-5+ 109 RxFD5_P
TxFD5_N 63 TxFD-5- RxFD-5- 108 RxFD5_N
TxFD4_P 50 TxFD-4+ RxFD-4+ 121 RxFD4_P
TxFD4_N 51 TxFD-4- RxFD-4- 120 RxFD4_N
TxFD3_P 38 TxFD-3+ RxFD-3+ 133 RxFD3_P
TxFD3_N 39 TxFD-3- RxFD-3- 132 RxFD3_N
TxFD2_P 26 TxFD-2+ RxFD-2+ 145 RxFD2_P
TxFD2_N 27 TxFD-2- RxFD-2- 144 RxFD2_N
TxFD1_P 14 TxFD-1+ RxFD-1+ 157 RxFD1_P
TxFD1_N 15 TxFD-1- RxFD-1- 156 RxFD1_N
UTCA_MCH_TONGUE3
CN4B
2 RSVD GND 86
3 RSVD GND 89
5 RSVD GND 92
6 RSVD GND 95
169 RSVD GND 98
168 RSVD GND 101
166 RSVD GND 104
165 RSVD GND 107
GND 110
1 GND GND 113
4 GND GND 116
7 GND GND 119
10 GND GND 122
13 GND GND 125
16 GND GND 128
19 GND GND 131
22 GND GND 134
25 GND GND 137
28 GND GND 140
31 GND GND 143
34 GND GND 146
37 GND GND 149
40 GND GND 152
43 GND GND 155
46 GND GND 158
49 GND GND 161
52 GND GND 164
55 GND GND 167
58 GND GND 170
61 GND GND 85
64 GND GND 82
67 GND GND 79
70 GND GND 76
73 GND
UTCA_MCH_TONGUE3
GND
IC33C
BANK 14
IO_L18P_14 W25 TxFD6_P
IO_L18N_14 Y25 TxFD6_N
IO_L19P_14 W27 TxFD5_P
IO_L19N_14 W26 TxFD5_N
IO_L15P_14 Y29 TxFD4_P
IO_L15N_14 Y29 TxFD4_N
IO_L5P_14 Y26 TxFD3_P
IO_L5N_14 Y27 TxFD3_N
IO_L1P_14 Y28 TxFD2_P
IO_L1N_14 Y29 TxFD2_N
IO_L4P_14 V33 TxFD1_P
IO_L4N_VREF_14 V34 TxFD1_N
IO_L6P_14 V33
IO_L6N_14 V32
IO_L7P_14 V28
IO_L7N_14 V29
IO_L8P_SRCC_14 V31
IO_L8N_SRCC_14 V30
IO_L9P_MRCC_14 Y30
IO_L9N_MRCC_14 W30
IO_L10P_MRCC_14 V34
IO_L10N_MRCC_14 W34
IO_L11P_SRCC_14 V28
IO_L11N_SRCC_14 V27
IO_L12P_VRN_14 V32
IO_L12N_VRP_14 V33
IO_L13P_14 V32
IO_L13N_14 V31
IO_L0P_14 Y25 RxFD6_P
IO_L0N_14 Y25 RxFD6_N
IO_L17P_14 Y28 RxFD5_P
IO_L17N_14 Y27 RxFD5_N
IO_L14P_14 Y33 RxFD4_P
IO_L14N_VREF_14 Y34 RxFD4_N
IO_L16P_14 W31 RxFD3_P
IO_L16N_14 W32 RxFD3_N
IO_L3P_14 Y30 RxFD2_P
IO_L3N_14 Y31 RxFD2_N
IO_L2P_14 W33 RxFD1_P
IO_L2N_14 W34 RxFD1_N
XC6VLX130T-1FF1156C
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Size A4
Number
Revision
Date: 07/12/2011
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