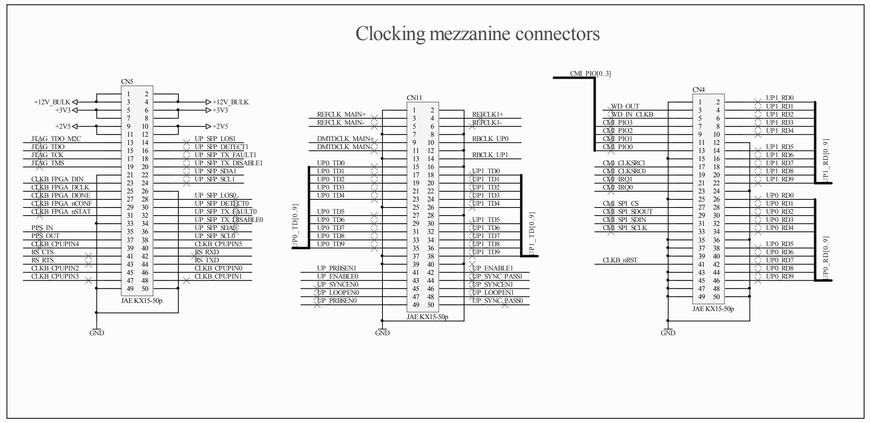
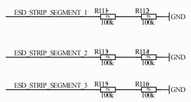
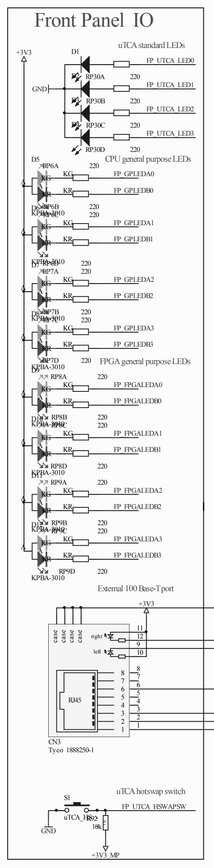
Clocking mezzanine connectors



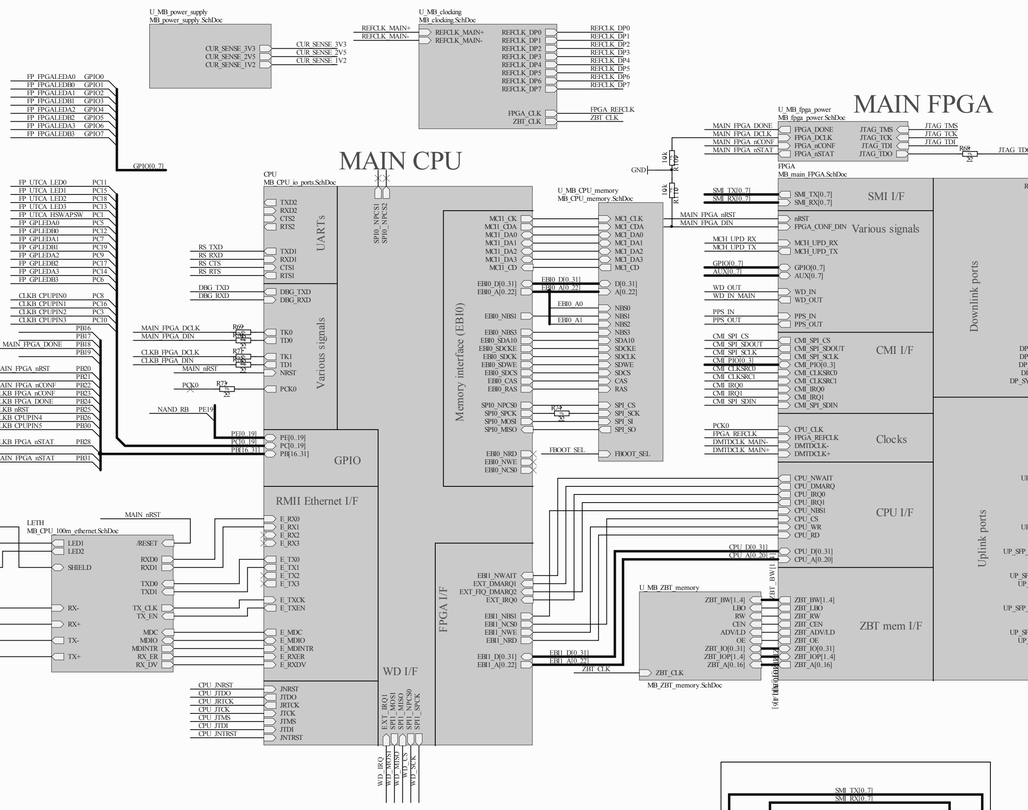
ESD strip



Front Panel IO



MAIN CPU

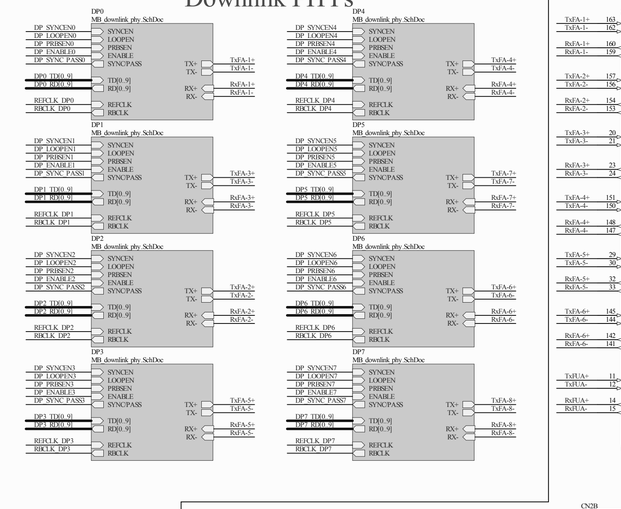


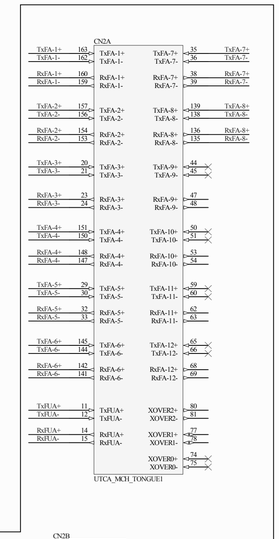
MAIN FPGA

Main System Diagram with:
- big Cyclone3-120 FPGA
- AT91SAM9263 CPU + memories + peripherals
- downlink PHYs and uTCA backplane interface

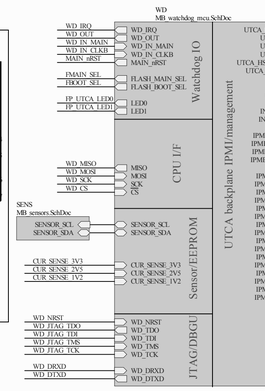
Includes all front panel controls/connectors being placed on MCH PCB1 and most important connectors (backplane, mezzanines, JTAGs)

Downlink PHYs

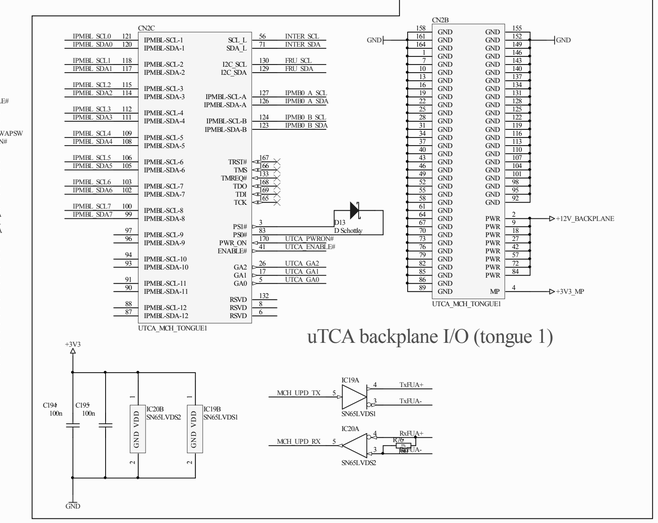




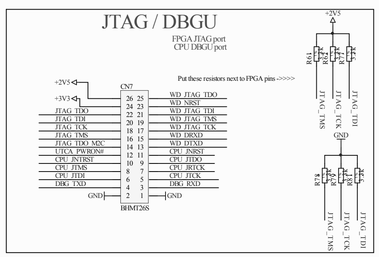
Watchdog MCU



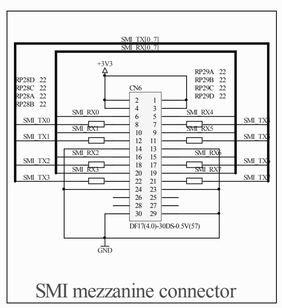
uTCA backplane I/O (tongue 1)



JTAG / DBGU



SMI mezzanine connector



Project:	White Rabbit Switch MCH - mainboard
Sheet:	Main (top-level) diagram
Version:	1.1.0
Date:	2009/11/12
Author:	Tomasz Wlostowski
License:	Open Hardware License (OHL)
Company:	CERN BE-CO-HT