Schematics and Layout Review | 07.02.2012

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Notes from Matthieu Cattin. Other comments were directly given to Nicolas Voumard.

Schematics

General:
- About the BOM reduction, we can for example put several resistor in series and/or parallel.

- There is still 22 different resistor types and 14 are only used 1 or 2 times!
- There is 2 types of 10uF capacitor and a 47uF.
- 220nF can be replaced by 2x 100nF.
- There is 1.5nF and 1nF, can't we use 1.5nF instead of 1nF?
- Can't we use the same ferrite as the P3V3_PLL for the VCO?

FMC_TDC_1ns_5Cha.SchDoc:
- Active low signal naming is not consistant (n, N, _N, with bar over).
One could use "_N" everywhere.

FMC connector.SchDoc:
- Pin d29 is reserved for JTAG TCK and can't be used as generic IO for the SPI clock (SCLK)!
SCLK can be moved to a free LA_x pin, h35, h37 or h38.
-> Remove IO expander and use free pins as discussed during the review.
- Why not using LVDS level for FPGA_TDC_REF_CLK? There is a free differential output on the AD9516.

clock_generator.SchDoc:
- Display the component reference for OSC1 and OSC2. 20MHz doesn't help much...

INPUT_LOGIC.SchDoc:
- The fuse is still there, issue 389 says:
"remove the input fuse as it is too slow to handle surge current before
the protection diodes and/or the CDCLVC1102PW dies..."
-> Update the issue on OHR.
- Termination resistors are still 3x 150ohms, issue 389 says:
"replace the three 150Ohms termination resistors (1206 case) by one 51Ohms 0.75 (2010 case).
The 2010 case takes less place than three 1206.."
-> Update the issue on OHR.

MEM.SchDoc:
- The memory looks stupid on this sheet.
-> move it to the top sheet.

Layout

Layout
- TDC_IN_FPGA1 and TDC_IN_FPGA2 are crossing P3V3_PLL plane (Signal_Int2).
- TDC_IN_FPGA5 is crossing VDD2_TDC plane (Signal_Int2).
- Some vias doesn't have solder mask tenting.
- R7A, R8A, R10A, R11A, R12A, LD1, LD2, LD3 designators (silkscreen) are under the front panel.
- Solder mask expansion is set to 0mm. It is probably wrong.
- CERN logo should be removed.
- Add corners for bar-code sticker (c.f. fmc-adc-100m-14b-4cha).
- Some designators are under the component (J1, J2, J3, J4, J5, etc...).
- Solder mask should be removed from the copper area under the front panel.