FIELDRIVE
User Reference Manual

ALS 50261 h–en

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Index letter	Date	Nature of revision
b	**04–1996**	Addition of 2.5 Mbits/s speed.
c	**09–1999**	Addition of a new diagram (Figure 15) Minor modifications
d	**08–2000**	5 Mbits/s network transmission rate
e	**10–2001**	Example of implementation of a fieldbus connection 1 Mbit/s (120 Ω characteristic impedance of network cabling)
f	**10–2002**	Modifications in Chapter 6, Examples of FIELDRIVE connections
g	**06–2003**	Updated following new production sourcing
h	**01–2004**	• New: Figure 6.3 • Modifications in Figure 6.2

Revisions

1. PURPOSE OF MANUAL AND DOCUMENTED VERSION

This manual gives FIELDRIVE component technical information. This information is useful to interface FIELDRIVE between a protocol component and an isolating transformer. FIELDRIVE is a fully integrated driver circuit.

2. CONTENT OF THIS MANUAL

Chapter 1: General presentation.

Chapter 2: Pin assignments.

Chapter 3: Functional description: describes receiver/transmitter section signals and test modes.

Chapter 4: Electrical characteristics.

Chapter 5: Physical dimensions.

Chapter 6: Examples of FIELDRIVE connections.

3. RELATED PUBLICATIONS

For more information refer to these publications:

[1] EN50170 part 3:	WorldFIP Standards
[2] FIP Network General Introduction	ALS 50249
[3] FIELDRIVE User Reference Manual	ALS 50261
[4] FULLFIP2 Component User Reference Manual	ALS 50262
[5] FIELDUAL User Reference Manual	ALS 50273
[6] FIPCODE Release 6 Software User Reference Manual	ALS 50277
[7] MICROFIP User Reference Manual	ALS 50280

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REMARKS

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Chapter 1 General presentation

The FIELDRIVE component is a fully integrated line driver circuit, dedicated providing the interface between a protocol component and an isolating transformer of a fieldbus physical medium (this function is also called MAU – Medium Attachement Unit). This connection is represented in Figure 1.1.

The FIELDRIVE component implements several profiles that the two following standards have in common:

- IEC 61158-2: Physical Layer specification and service definition.
- CENELEC EN50170: Physical Layer specification.
- AFNOR Standard NFC46-604: Baseband shielded twisted pair, Physical Layer.

STANDARD	IEC 61158-2/ CENELEC EN50170	AFNOR NFC46-604
PROFILES	31.25 kbits/s Low speed Wire / Voltage mode	CL-S1 profile
	1 Mbit/s High speed Wire / Voltage mode	CL-S2 profile
	2.5 Mbits/s High speed Wire / Voltage mode	CL-S3 profile
	5 Mbits/s High speed Wire / Voltage mode	Added in the new version of the IEC 61158-2 standard

Table 1.1 – Profiles implemented in FIELDRIVE

The FIELDRIVE component is designed using a 0,6 µm biCMOS process from XFAB. It is packaged in a 28-pin PLCC by Swindon Silicon Systems Ltd.

The transmit and receive signals are an encoded data sequence (Manchester Biphase L).

The FIELDRIVE component is designed to be connected with a protocol coprocessor (FULLFIP2 etc.) offering a MAU-MDS interface.

The implementation of complete line driving/receiving circuitry requires associating the FIELDRIVE chip with:

- an isolating transformer,
- a protection circuit,
- passive filtering elements (specific for each network bit rate).

The FIELDRIVE component integrates a line driver, a line receiver, transmit error detection circuitry, a monitoring interface and test interface circuit.

The transmit error detection device includes a line overload/underload detection and a watchdog for the jabber inhibit function.

Integrated diagnosis modes provide loopback capabilities which can be used by the application test routines.

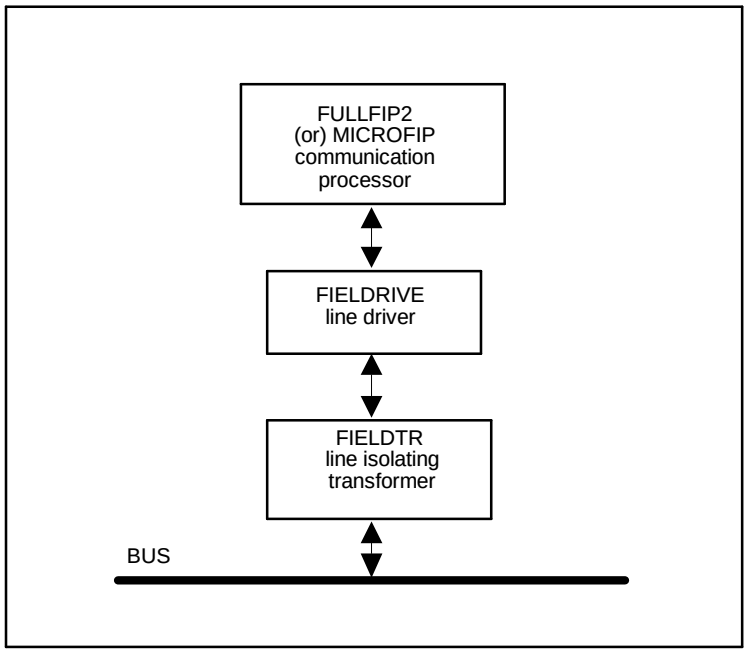

Figure 1.1 – WorldFIP fieldbus subscriber connection

Chapter 2 Pin Assignments

1. PINOUT DIAGRAM

The FIELDRIVE circuit is packaged in a 28–pin PLCC.

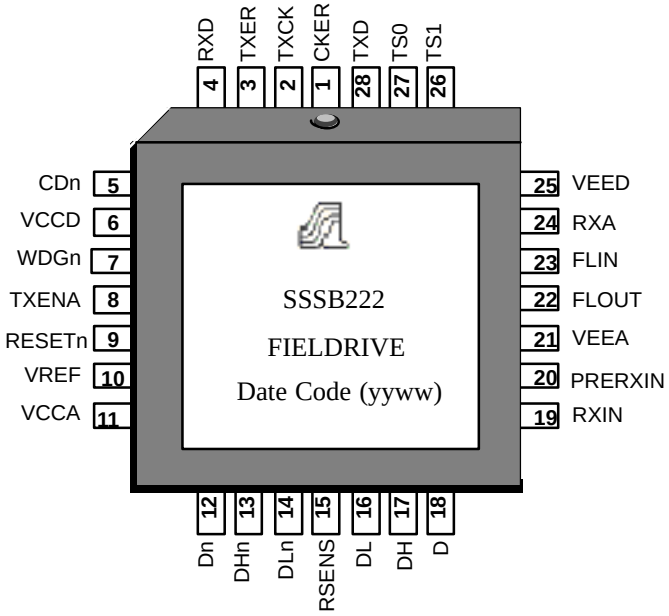

Figure 2.1 – FIELDRIVE component pinout diagram – Top view

2. PIN DESCRIPTION

Pin description is shown in Table 2.1.

No.	Pin Name	Type	Description
1	CKER	TTL Input	Transmit error detect clock
2	TXCK	TTL Input	Half bit clock
3	TXER	TTL Output	Transmit data error
4	RXD	TTL Output	Received data
5	CDn	TTL Output	Carrier detect
6	VCCD	Digital Supply	Digital positive supply +5 V
7	WDGn	TTL Output	Transmitter watchdog
8	TXENA	TTL Input	Transmit data enable
9	RESETn	TTL Input	Initialization control
10	VREF	Analog Output	Voltage reference
11	VCCA	Analog Supply	Analog positive supply +5 V
12	Dn	Analog Input	Differential data line
13	DHn	Analog Output	Differential transmitter data
14	DLn	Analog Output	Differential transmitter data
15	RSENS	Analog Supply	Driver supply
16	DL	Analog Output	Differential transmitter data
17	DH	Analog Output	Differential transmitter data
18	D	Analog Input	Differential data line
19	RXIN	Analog Input	Analog comparators
20	PRERXIN	Analog Output	Received, filtered and adapted data
21	VEEA	Supply	Analog ground
22	FLOUT	Analog Output	Active filter output
23	FLIN	Analog Input	Active filter input
24	RXA	Analog Output	Differential amplifier output
25	VEED	Supply	Digital ground
26	TS1	TTL Input	Test
27	TS0	TTL Input	Test
28	TXD	TTL Input	Transmit data

Table 2.1 – FIELDRIVE line driver pin description

Chapter 3 Functional description

The circuit can be operated at any one of the following data rates: 31.25 kbits/s, 1 Mbit/s, 2.5 Mbits/s and 5 Mbits/s.

The chip is composed of two parts:

- an analog portion,
- a digital portion.

The analog portion consists of a line driver, a line receiver, several comparators and a voltage reference. The digital portion provides control of the line driver and line receiver. In addition, it provides digital processing of the transmitted signal to identify various error conditions and allows for implementation of local test modes.

The receiver section of the chip receives signals differentially. These analog signals are filtered with a filter which is built with external components. The filtered signal is then compared to fixed DC levels to produce a digital signal. The resulting signal is then digitally processed to generate the carrier detect and the received data outputs.

The transmitter section of the chip consists of a push–pull stage driving a defined load, for instance a WorldFIP line through an isolating transformer. The driver may be tri–stated, so as to present a high impedance to the transmission line when the FIELDRIVE is operating as a receiver. During transmission, various errors are detected: these error states are used to allow a high level of transmission grade.

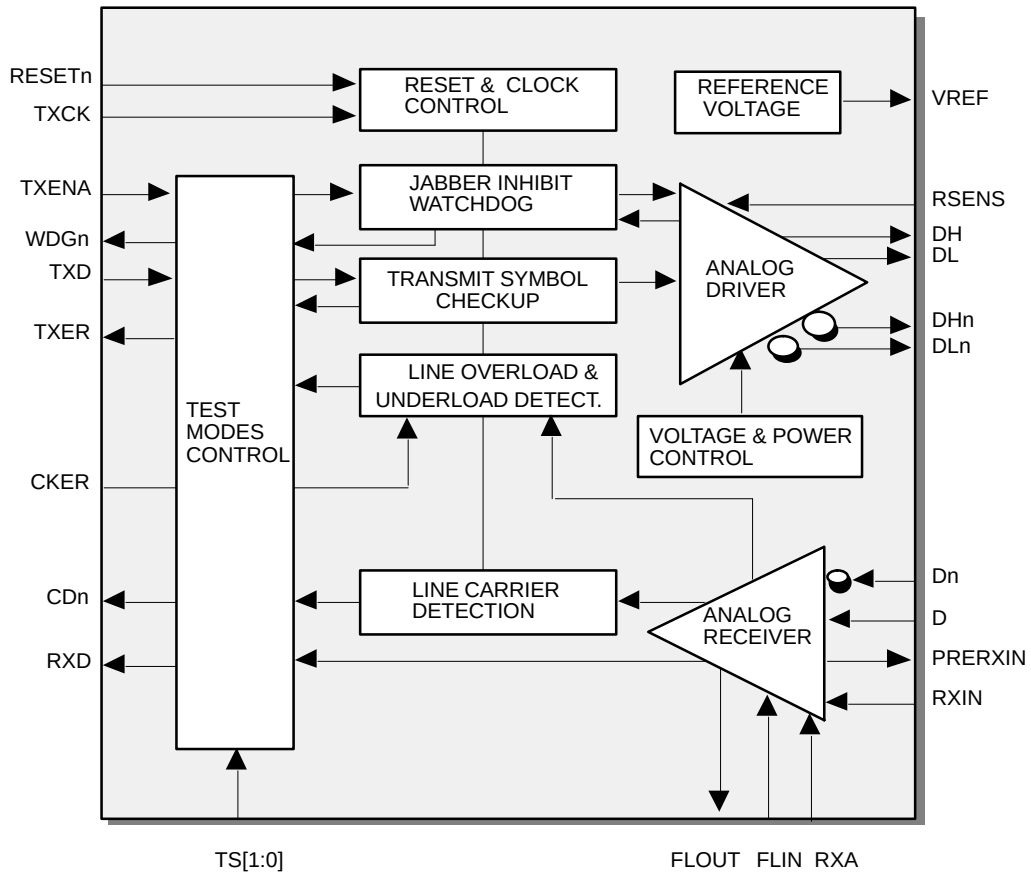

Figure 3.1 – Functional diagram

1. RECEIVER SECTION

The receiver block consists of analog circuitry, comparators to translate the signals to digital levels and digital circuitry to determine the validity of the received signals.

The input to the receiver is a differential signal from the line transformer. This signal is centered around a reference and is symmetrical. The signal is filtered by a device which is implemented with passive external components. The filtered signal is then compared with on chip reference levels; the comparator outputs are then processed digitally to produce a carrier detect signal. The filtered signal is also passed through a hysteresis comparator to the received data output pin.

Digital processing of the received signal consists in sampling the received signal on alternate asynchronous clock edges in order to determine if the incoming signal is a valid signal or if it is a glitch. A valid signal will produce a carrier detect output or a delayed carrier detect output as determined by the mode selected by the Test control pins.

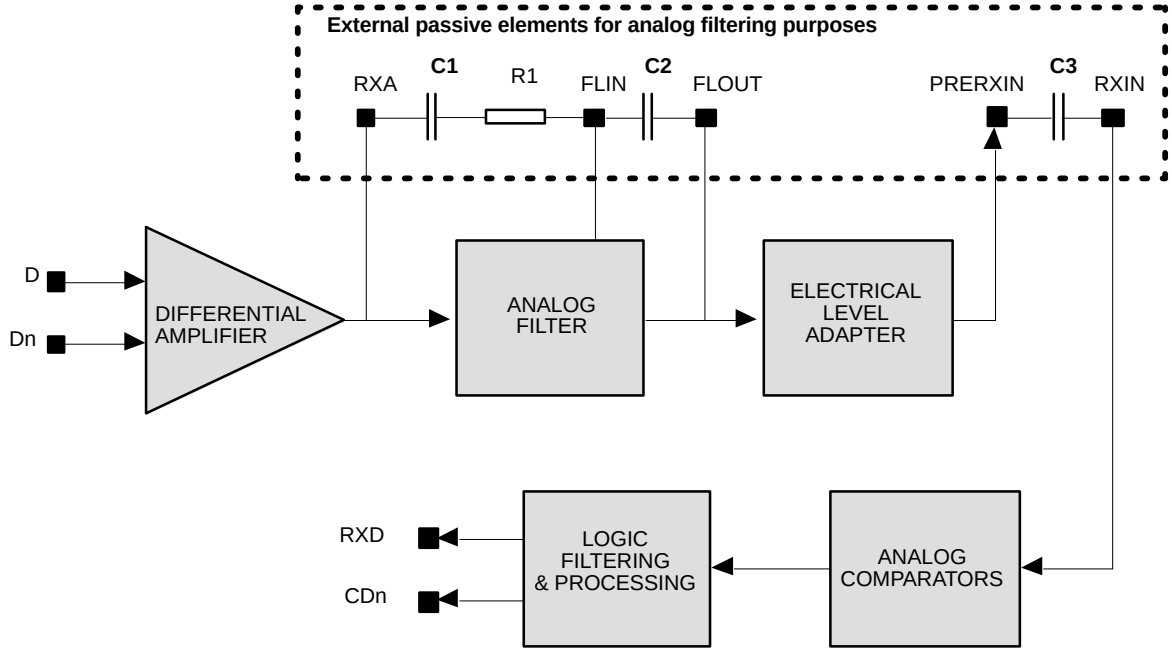

Figure 3.2 – Receiver section functional diagram

	NETWORK DATA RATE				
	31.25 kbits/s	31.25 kbits/s	1 Mbit/s	2.5 Mbits/s	5 Mbits/s
R1	330 Ω	1 kΩ	820 Ω	820 Ω	820 Ω
C1	22 nF	100 nF	100 pF	33 pF	22 pF
C2	1 nF	470 pF	47 pF	27 pF	10 pF
C3	100 nF	100 nF	3.3 nF	1.5 nF	1.5 nF

Table 3.1 – Proposed values of the external passive elements

The main logical function of the receive section is to manage the receiver output and the carrier detect signals. The carrier detect signals indicate if there is activity on the line. Referring to the schematic of the receiver section, RXIN is the filtered analog signal from the line. This signal is converted to a digital signal by a window comparator. The digital signal is sampled and filtered in order to eliminate glitches. The output of the sampling filter (Set–CD) is active when the threshold level is exceeded by time tCDL. The Set–CD signal sets ICDn and ILCDn. ICDn will become inactive when no Set–CD signal has been detected in the last tCDh time period. Time tLCDh later, ILCDn will become inactive. This causes a check for Set–CD activation again.

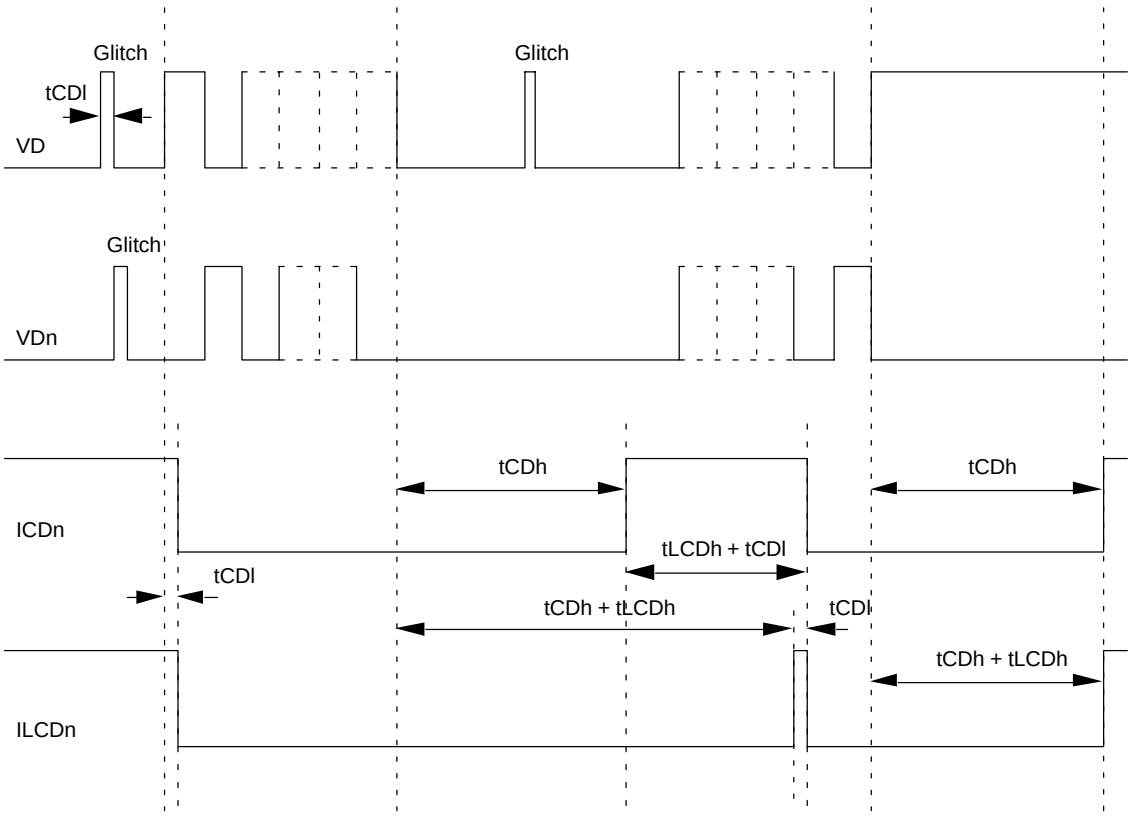

Figure 3.3 – Receiver section timing diagram

2. TRANSMITTER SECTION

The transmitter section consists of a differential line driver which is tri–stateable. This driver is required to drive a low impedance load and provides maximum output voltage swing. The transmitter output signal is edge–controlled so as to minimize EMI and distortion of the transmitted signal. Load current monitoring is provided to determine if the drivers are in overload state or underload state. This information is provided in the form of an error flag.

The transmitter section handles four basic monitoring functions. These are:

- Tri–stated output drivers are controlled by the TXENA input signal. When TXENA is inactivated the drivers must become tri–stated to prevent the chip from interfering with the line.
- A TXER signal is generated when the symbol duration exceeds tDsymb, which indicates a “stuck at fault” condition.
- A TXER signal is generated when an overload state or an underload state is monitored from the driver outputs.
- A watchdog signal WDGn is generated when the frame length exceeds tDjab, the jabber time. This signal is kept active until re–initialization of the chip with the RESETn input signal.

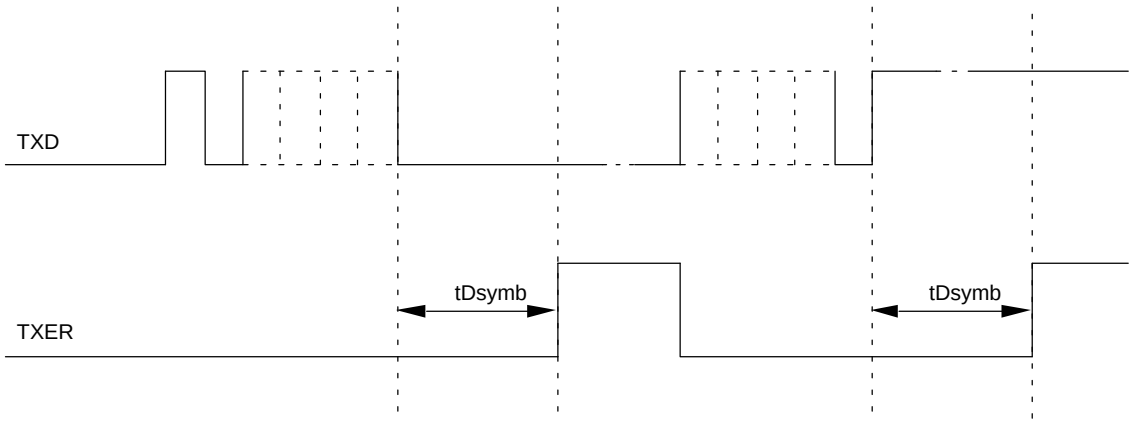

Figure 3.4 – Symbol error timing diagram

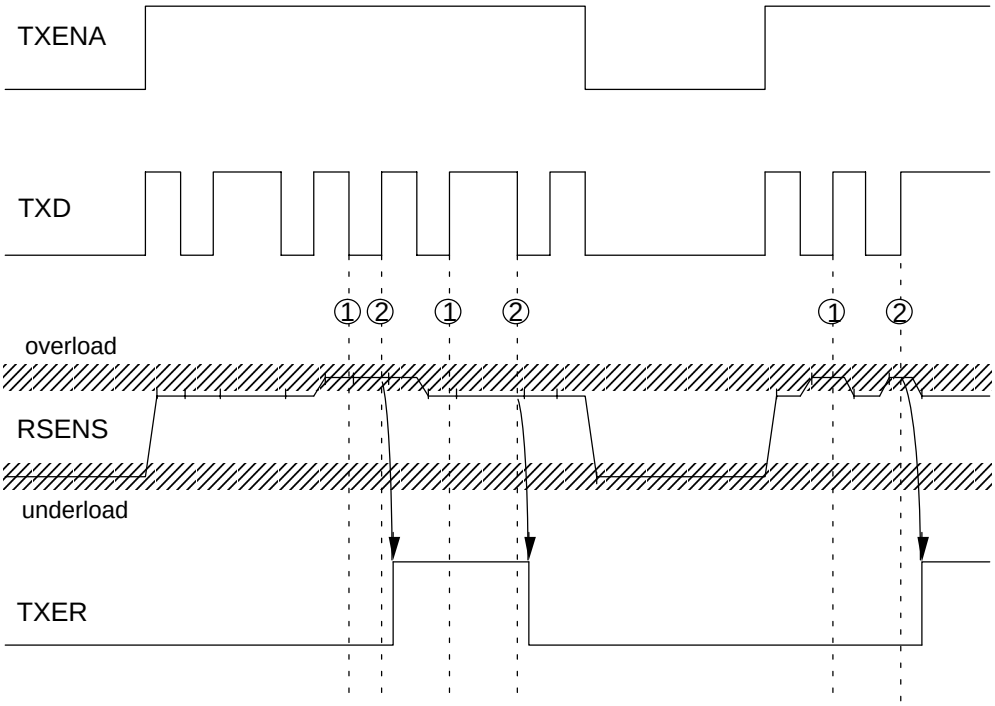

Figure 3.5 – Overload detection timing diagram

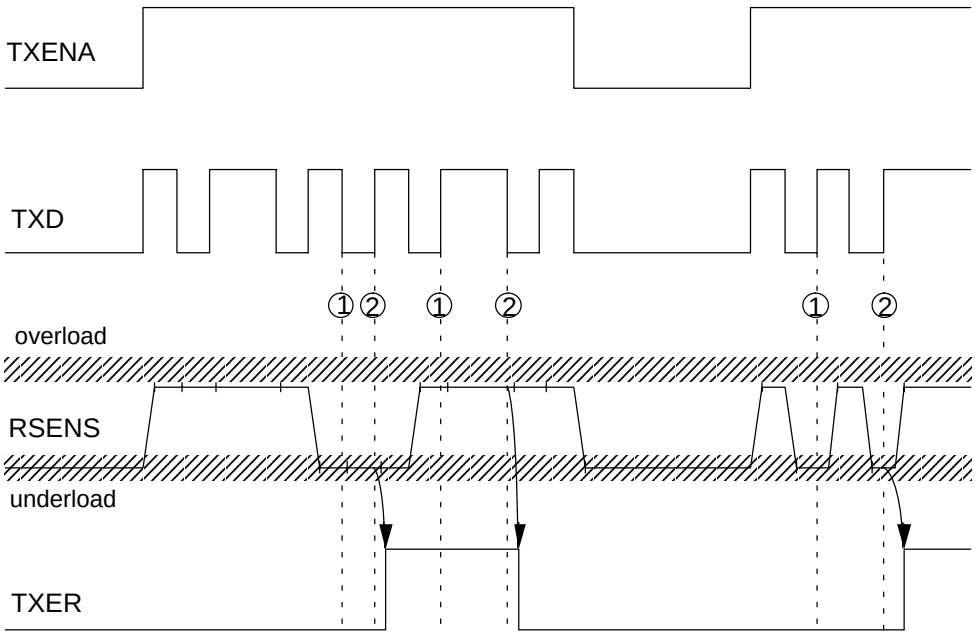

Figure 3.6 – Underload detection timing diagram

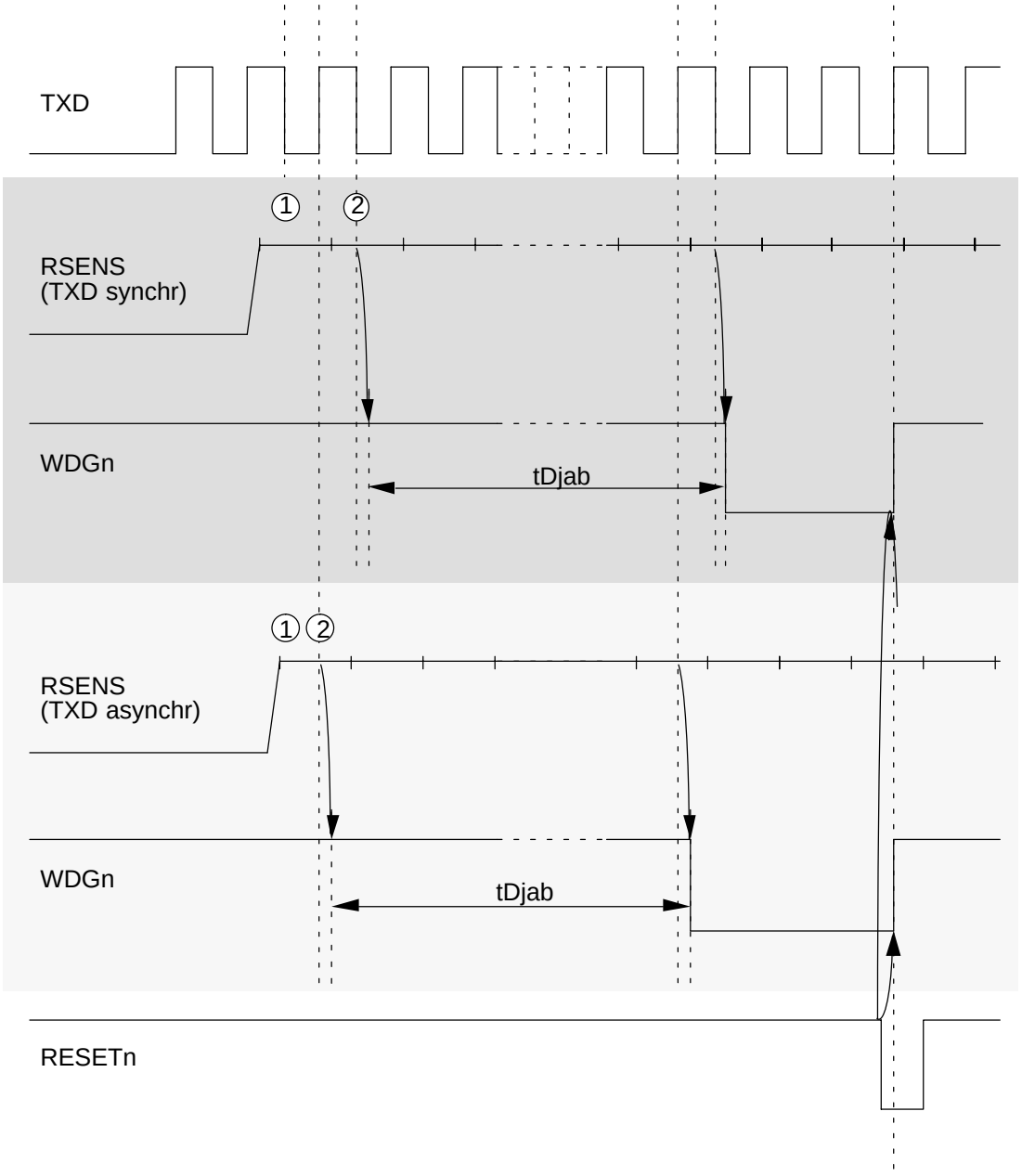

Figure 3.7 – Jabber error timing diagram

3. TEST MODES

There are two dedicated test pins available on the FIELDRIVE chip. They participate in the testing of the component and exercises FIELDRIVE in certain special loopback and diagnosis modes. The test modes are summarized in Table 3.2.

TS0	TS1	Type	Function
Low	Low	User	Normal mode.
Low	High	User	Normal mode with CDn delayed by 6 Tbits.
High	Low	User	Local loopback mode: TXD –> RXD TXENA –> CDn
High	High	User	Local loopback mode with TXER forced active high and WDGn forced active low.

Table 3.2 – FIELDRIVE component test modes

Chapter 4 Electrical characteristics

Parameter	Comments	Min	Typ	Max	Unit
Input voltage	Any pin to VEEA unless otherwise specified	–0.5		+12	V
Input voltage (D, Dn)		–10		+12	V
Input voltage (DH, DHn)		–10		Vcc	V
Storage temperature		–65		+150	°C

Table 4.1 – Absolute maximum ratings(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vcc	Supply voltage		4.75	5.0	5.25	V
Icc	Supply current	No transmission, 5 Mbits/s		40		mA
Icc	Supply current	With transmission, 5 Mbits/s		120		mA
Operating free–air temperature			–40		+85	°C

Table 4.2 – Functional characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vop(VDH–VDLn)	Output voltage	Z(DH,DLn) = 35 Ω, VTXENA = Vcc	3.9		4.8	V
Von(VDHn–VDL)	Output voltage	Z(DH,DLn) = 35 Ω, VTXENA = Vcc	3.9		4.8	V
Vob(DH–DLn)	Differential output balance	Z(DH,DLn) = 35 Ω, Z(DHn,DL) = 35 Ω |[V(DH–DLn)–V(Dn–DL)]/V(DHn–DL)|	47		53	% Vp–p
Tr(VDH–VDLn)	Rise time	10% – 90% Vp–p, Z(D,Dn) = 35 Ω	14		40	ns
Tf(VDH–VDLn)	Fall time	90% – 10% Vp–p, Z(D,Dn) = 35 Ω	14		40	ns
TphTXENA (VDH–VDLn)	Transmit enable propagation delay time	90% (VDH–VDLn)			100	ns
TplTXENA (VDH–VDLn)	Transmit disable propagation delay time	10% (VDH–VDLn)			100	ns
Drd	Temporal distortion	Z(DH,DLn) = 35 Ω		4		ns

Table 4.3 – Transmitter section

[1] Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note

Characterization is made on the basis of the test conditions provided in the schema of Figure 4.1 where a standard resistive load Z is connected to D and Dn.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V(D–Dn)	Differential input voltage (received signal voltage range valid)		±0.20		±3	V
VCMRR(RXA)	Input common mode voltage rejection ratio	Vcm(D–Dn) = 150 mVp–p @ 6.25 MHz	20			dB
CD, Dn	Input capacitance	Transmitter Tri–state Fd = 3.125 MHz, 0 < Vcc < 5.25 V			4	pF
Rin(D–Dn)	Input resistance	Vcc = VEE = 0 V, V(D–Dn) = ±3 V	17.5	25	32.5	kΩ
Dtr(RXD)	Temporal distortion			4	8	ns

Table 4.4 – Receiver section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vinh	Input voltage high	All TTL inputs	2			V
Vinl	Input voltage low	All TTL inputs			0.8	V
Voh	Output voltage high	All TTL outputs, Ioh = –4 mA	2.4			V
Vol	Output voltage low	All TTL outputs, Iol = 2 mA			0.4	V
tDjab	Fault jabber time			8192		Tbit
tDsymb	Fault symbol time			4		Tbit
tCDl	CDn low threshold time		0.25		0.5	Tbit
tCDh	CDn high threshold time		3	3.5	4	Tbit
tLCDh	ICDn high threshold time			6		Tbit
FCLK	Clock frequency				10	MHz

Table 4.5 – Logic section

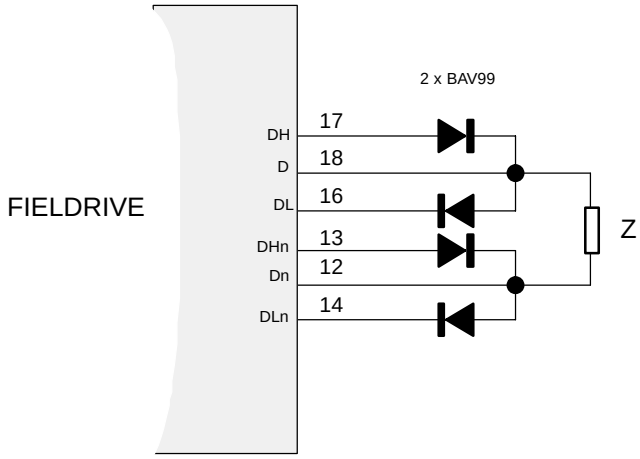

Figure 4.1 – Transmitter stage test conditions

Chapter 5 Physical dimensions

Figure 5.1 gives package outlines. Figure 5.2 and Figure 5.3 zoom on package details A and B. Package dimensions are given in millimeters. Dimensions in inches are put in brackets.

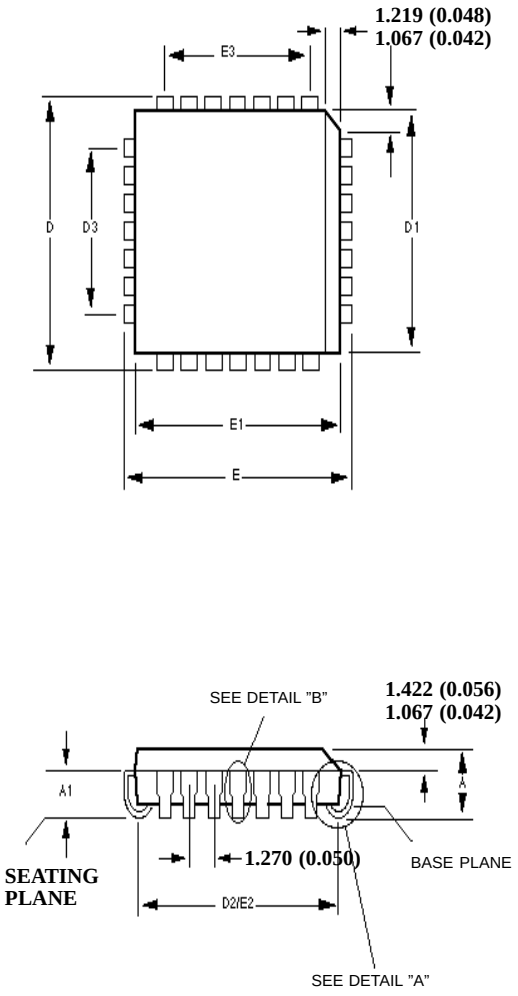

Figure 5.1 – Package outlines

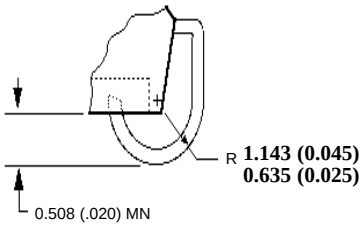

Figure 5.2 – Package outlines – Terminal detail A

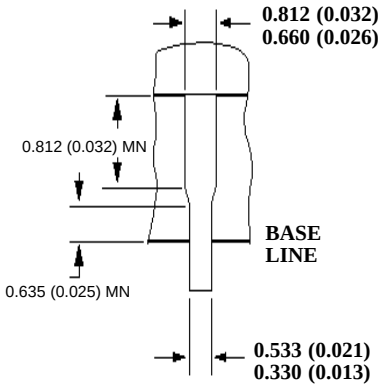

Figure 5.3 – Package outlines – Terminal detail B

Symbol	Minimum dimensions mm (inch)	Maximum dimensions mm (inch)
A	4.19 (0.165)	4.57 (0.180)
A1	2.29 (0.090)	3.05 (0.120)
D	12.32 (0.485)	12.57 (0.495)
D1	11.38 (0.448)	11.58 (0.456)
D2	9.91 (0.390)	10.92 (0.430)
D3	7.62 REF (0.300 REF)	
E	12.32 (0.485)	12.57 (0.495)
E1	11.38 (0.448)	11.58 (0.456)
E2	9.91 (0.390)	10.92 (0.430)
E3	7.62 REF (0.300 REF)	
N	28 pins	
ND	7 pins	
NE	7 pins	

Table 5.1 – Package dimensions

Chapter 6 Examples of FIELDRIVE connections

Protection of the FIELDRIVE line driver input/output against overvoltage generated on the bus outside the nominal range is proposed in the examples shown below.

Equipment	Connection	Function
FIELDRIVE Line driver	with FULLFIP2 communication processors	adapts the logical signal of the communication processor inputs/ outputs with the signal of the WorldFIP bus
FIELDTR Transformer	between the WorldFIP bus and FIELDRIVE	• ensures galvanic isolation • avoids transformer saturation by an eventual continuous current component (bus powered networks)
9–pin male* connector J9	between the subscriber and the WorldFIP bus	

* described in the physical layer standard.

Figures 6.1 to 6.7 describe the low level common element for a FIP connection at 31.25 kbits/s, 1 Mbit/s, 2.5 Mbits/s and 5 Mbits/s. The wiring to the upper component (Protocol management) is made with FULLFIP with or without FIELDUAL and MICROFIP.

For the definition see the User Reference Manuals [4], [5] and [7].

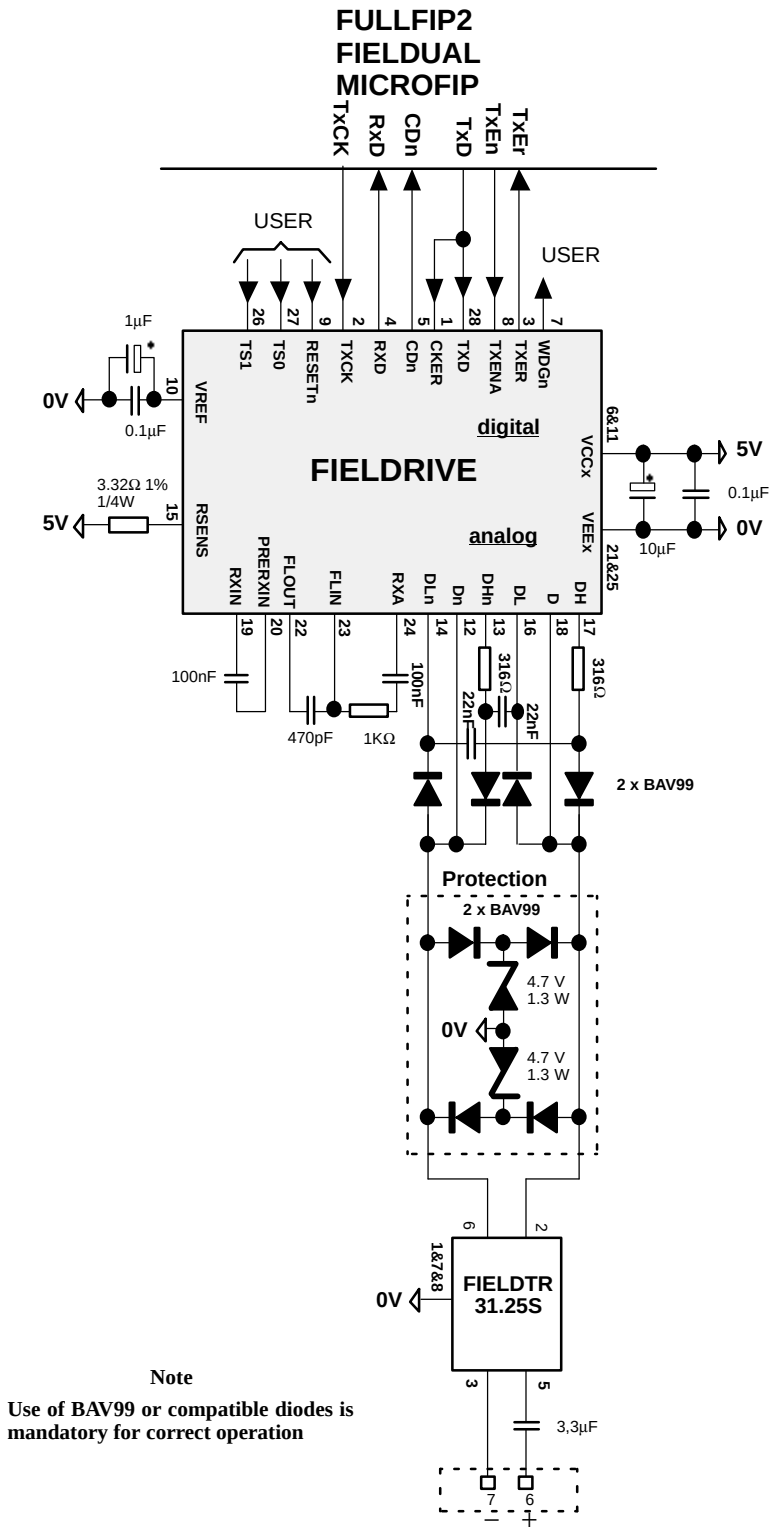

Figure 6.1 – Example of implementation of a fieldbus connection – 31.25 kbits/s (low level, 100 Ω impedance cable)

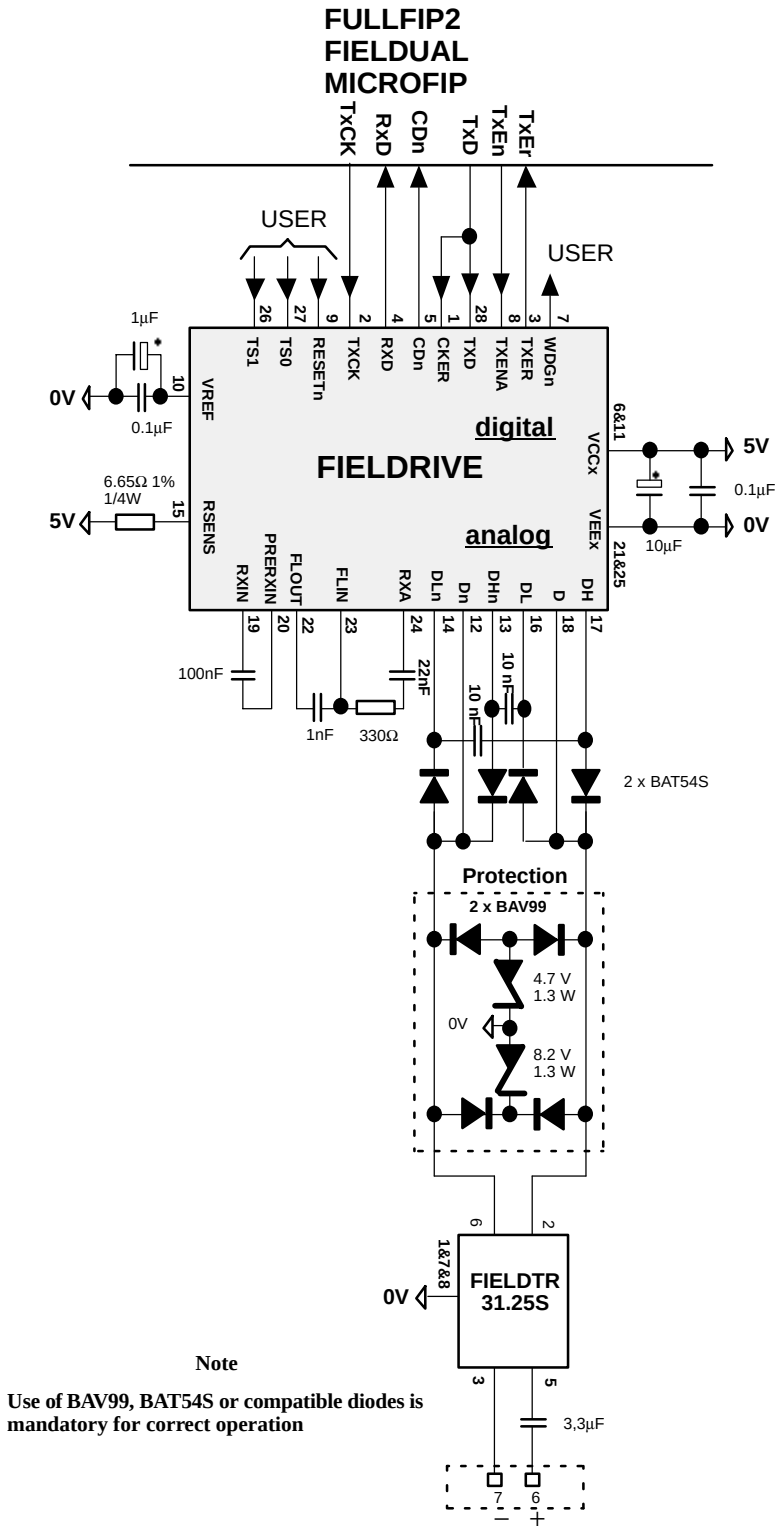

Figure 6.2 – Example of implementation of a fieldbus connection – 31.25 kbits/s (high level – long distance, 150 Ω impedance IBM Type cable)

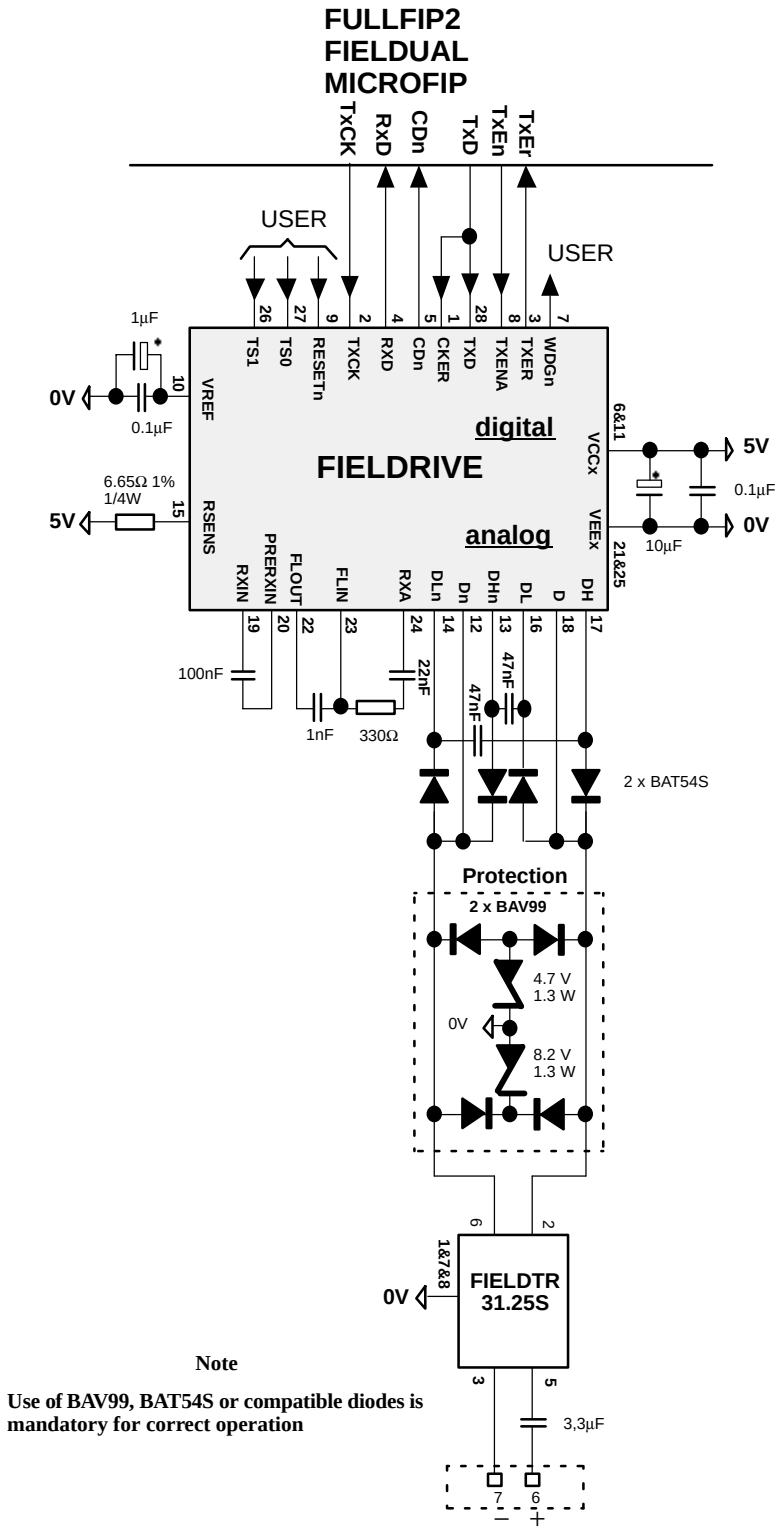

Figure 6.3 – Example of implementation of a fieldbus connection – 31.25 kbits/s (high level – long distance, 150 Ω impedance Serie 93 cable)

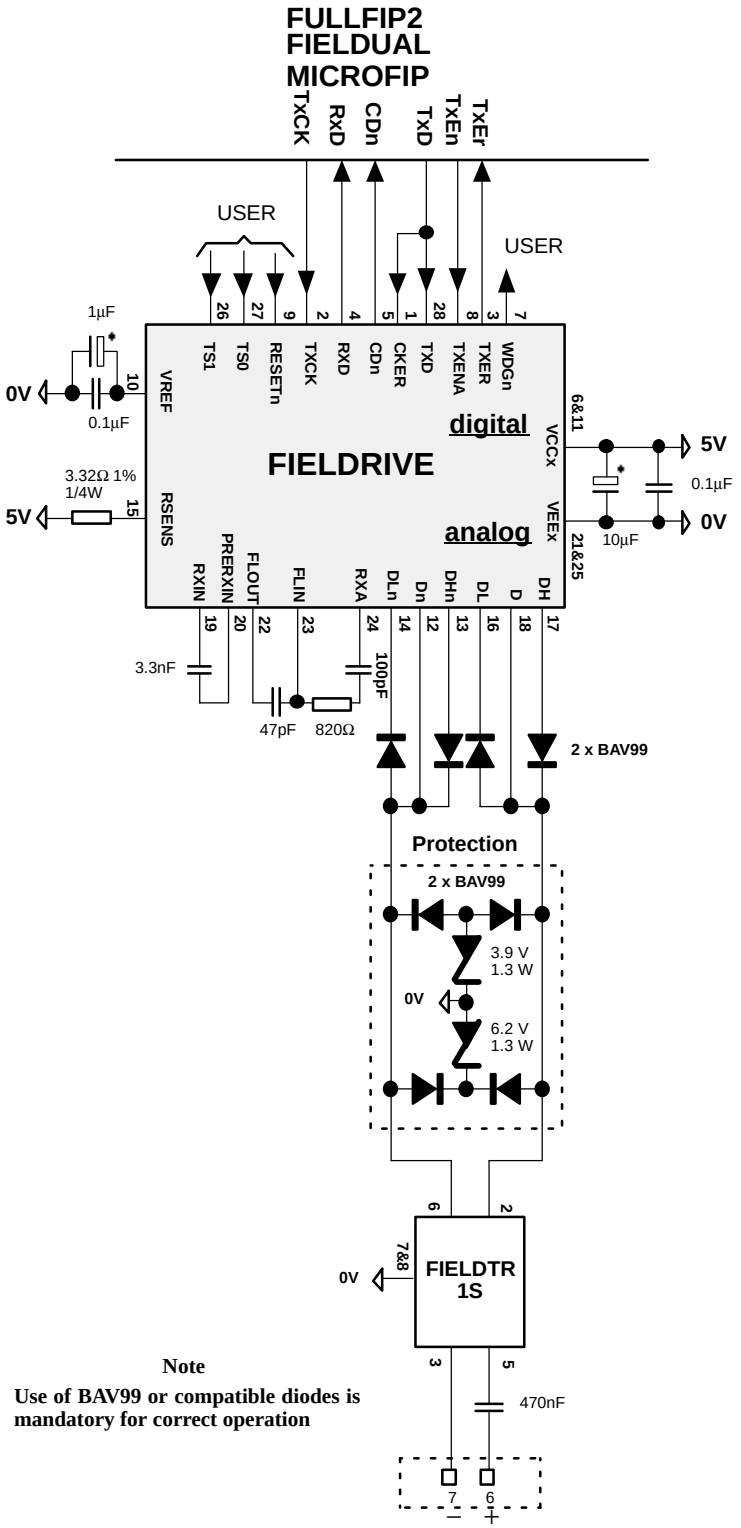

Figure 6.4 – Example of implementation of a fieldbus connection – 1 Mbit/s (150 Ω characteristic impedance of network cabling)

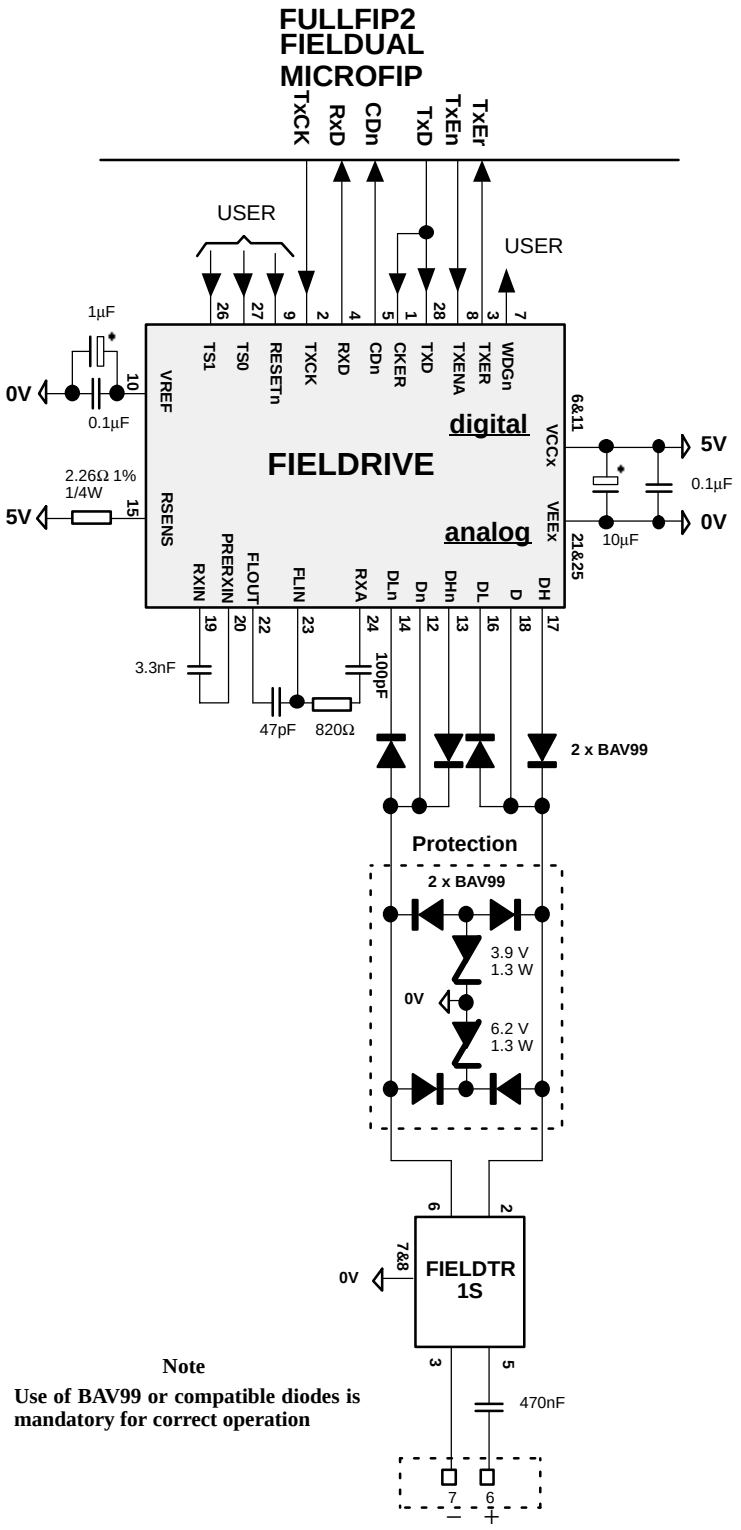

Figure 6.5 – Example of implementation of a fieldbus connection – 1 Mbit/s (120 Ω characteristic impedance of network cabling)

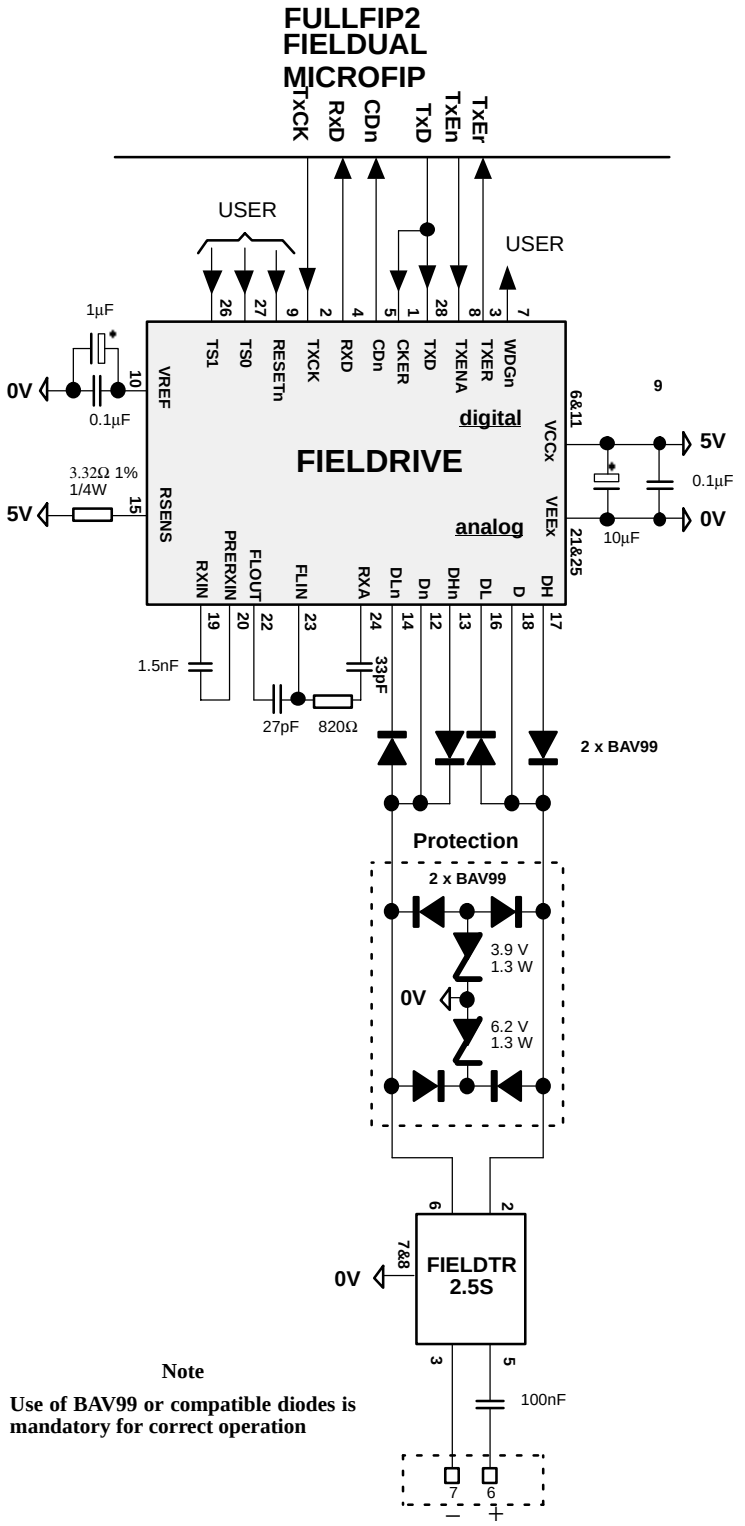

Figure 6.6 – Example of implementation of a fieldbus connection – 2.5 Mbits/s (150 Ω characteristic impedance of network cabling)

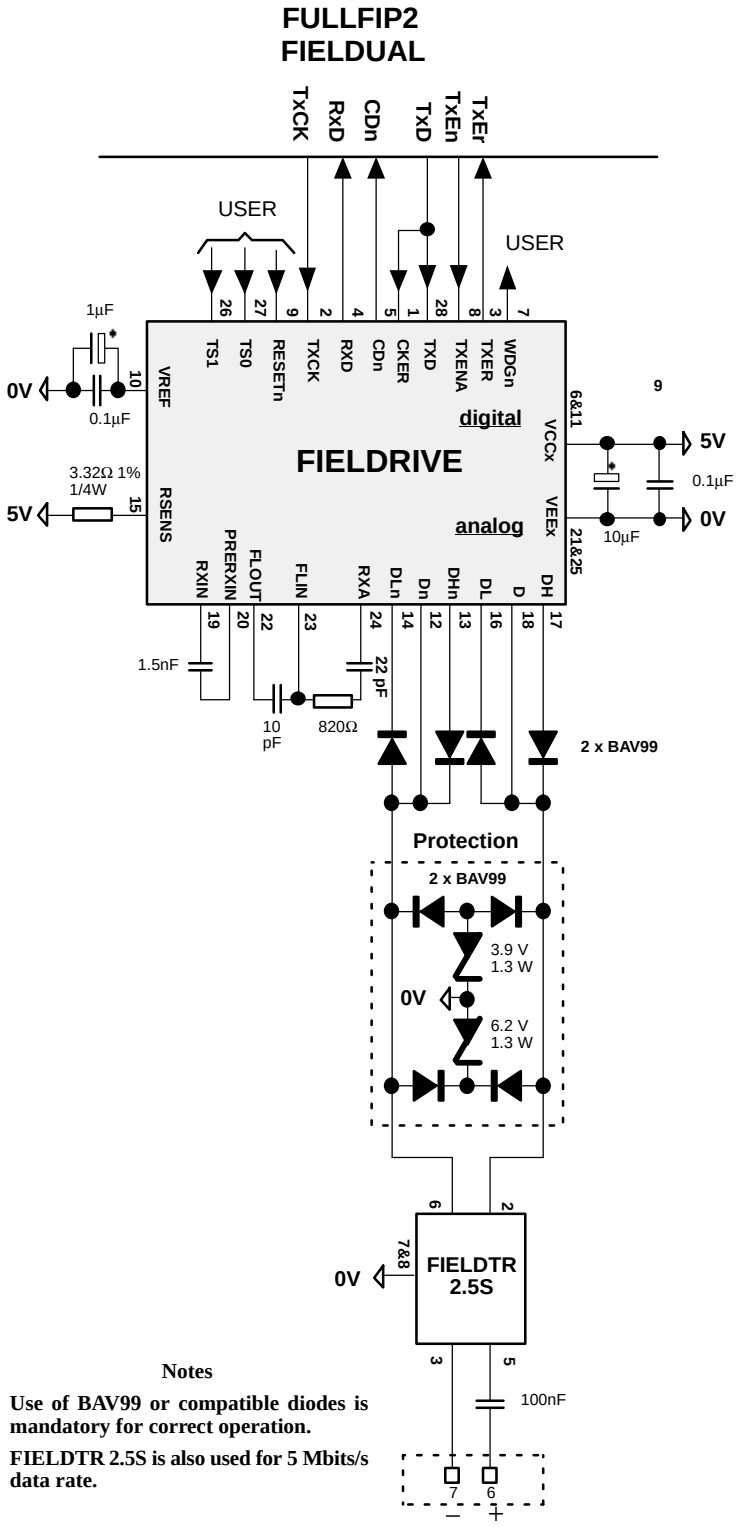

Figure 6.7 – Example of implementation of a fieldbus connection – 5 Mbits/s (150 Ω characteristic impedance of network cabling)