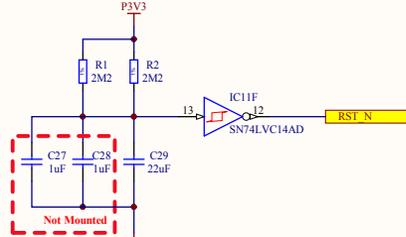
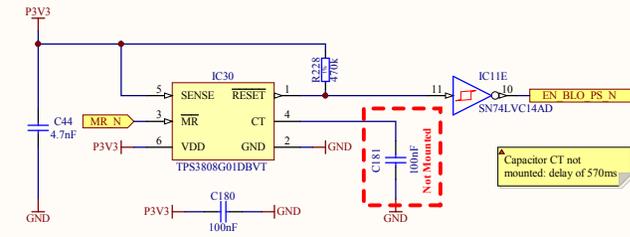
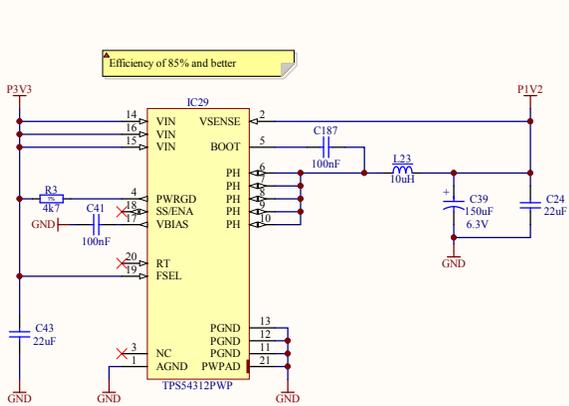
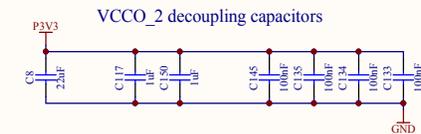
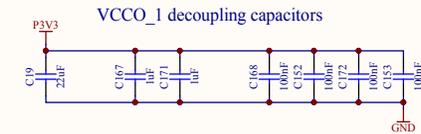
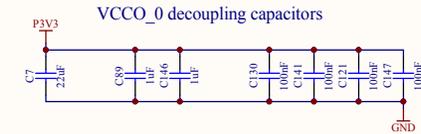
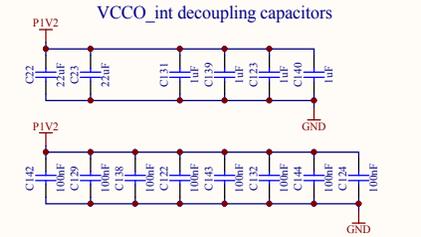


Project/Equipment		Standard Blocking Pulse Repeater	
Document	Conv-TTL-Blo TOP		Designer
			Drawn by
	European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Check by
Print Date			File
22/10/2012 17:27:17	ConvTtlBlo_TOP.SchDoc	Sheet	1 of 14
EDA-02446-V2-0		A3	1

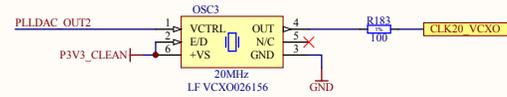
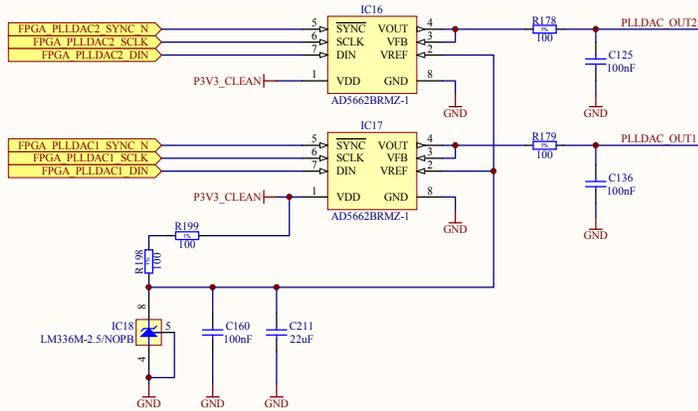


Voltages are:

*** FPGA	
VCC0_0	3V3
VCC0_1	3V3
VCC0_2	3V3
VCC0_3	3V3
VCCaux	3V3
VCCint	1V2
*** PROM	
VCCaux	3V3

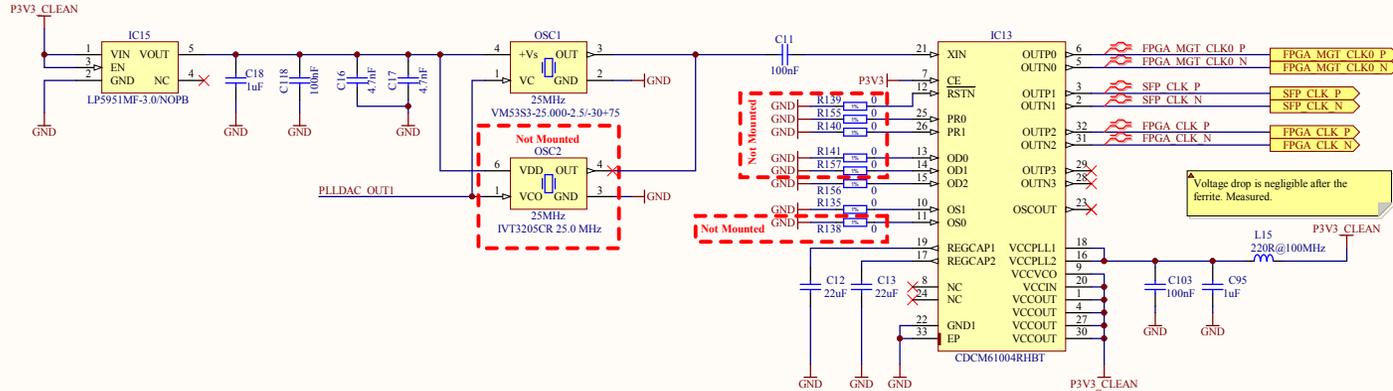


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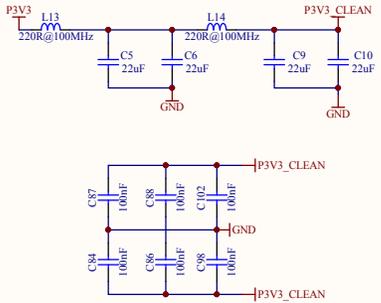


Control voltage is $\pm 1.5V \pm 1V$.
 Min. pull range is ± 10 ppm for $\pm 1V$.
 Positive slope (Positive voltage for positive frequency shift).

CDCM61004 configuration:
 LVDS outputs
 PRESC DIV = 4
 FB DIV = 20
 OUT DIV = 4
 All config inputs have internal pull-ups.
 Input = 25 MHz
 Output = 125 MHz

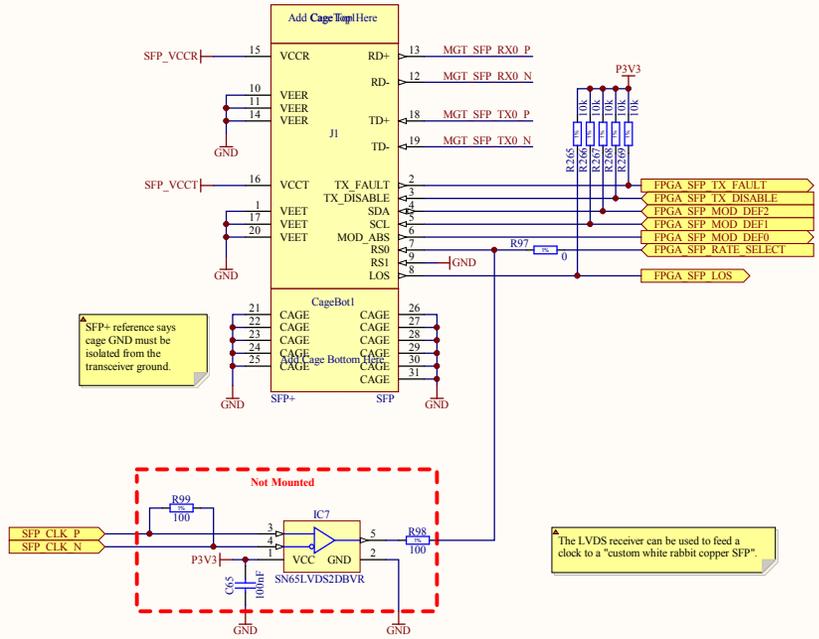
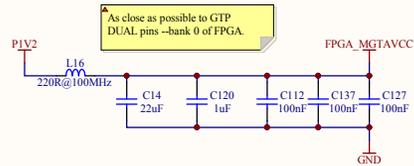
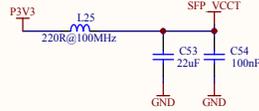
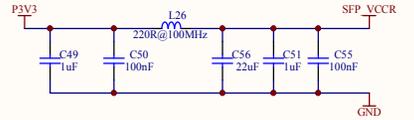


A voltage drop is negligible after the ferrite. Measured.

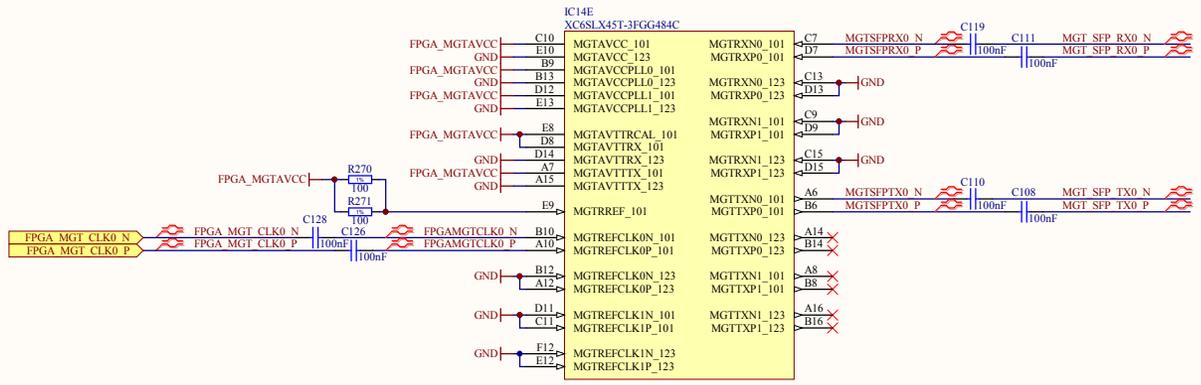


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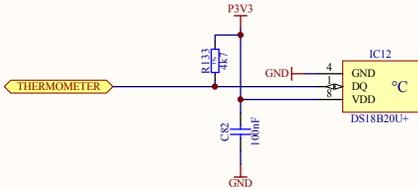
SFP+ module.
 Please refer to "SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+" to full understanding of the capabilities.



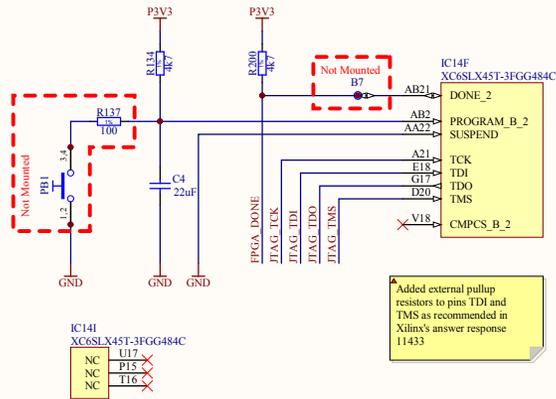
The trace length from the resistor pins to the FPGA pins MGTREF and MGTVTRCAL must be equal in length and geometry



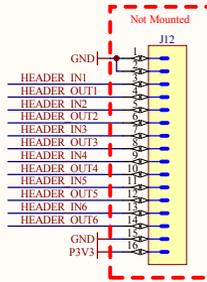
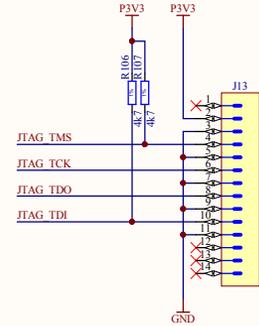
Thermometer will be used to have a FPGA unique ID



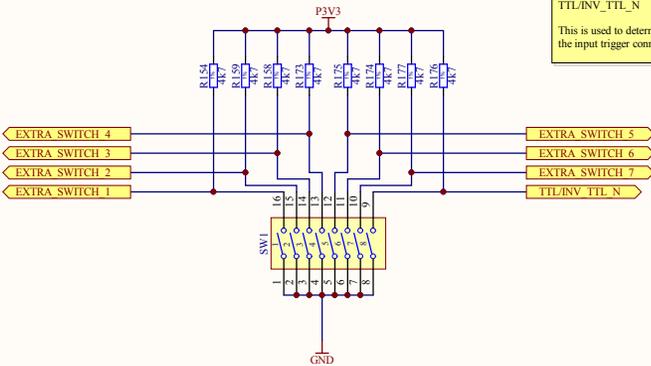
PROGRAM_B must be asserted low for more than 500ns



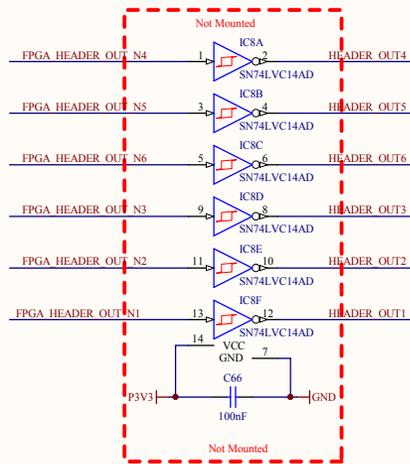
Added external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433



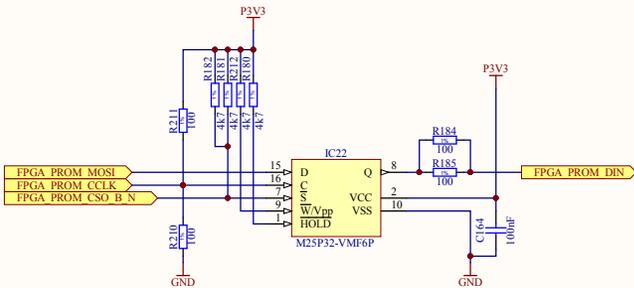
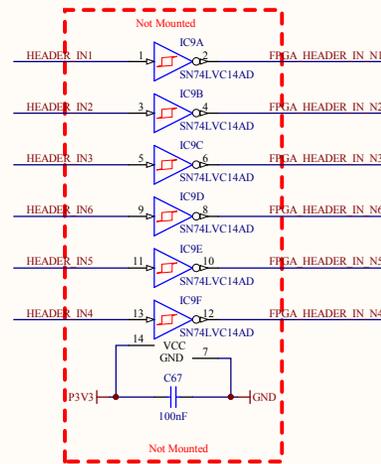
TTL/INV_TTL_N
 This is used to determine the level of the input trigger connector



FPGA HEADER OUT N[6..1]

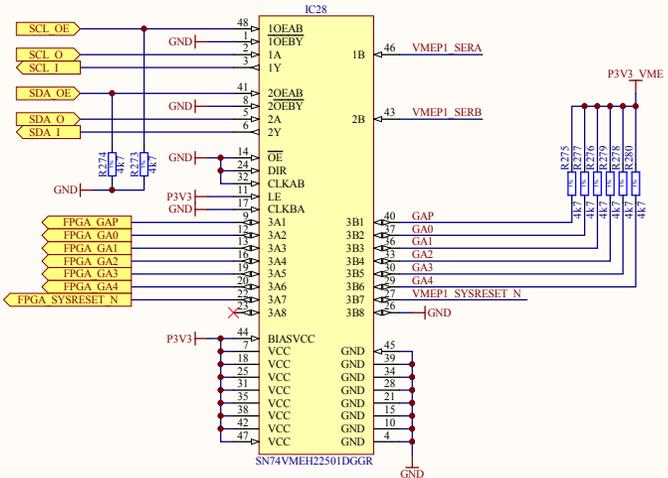
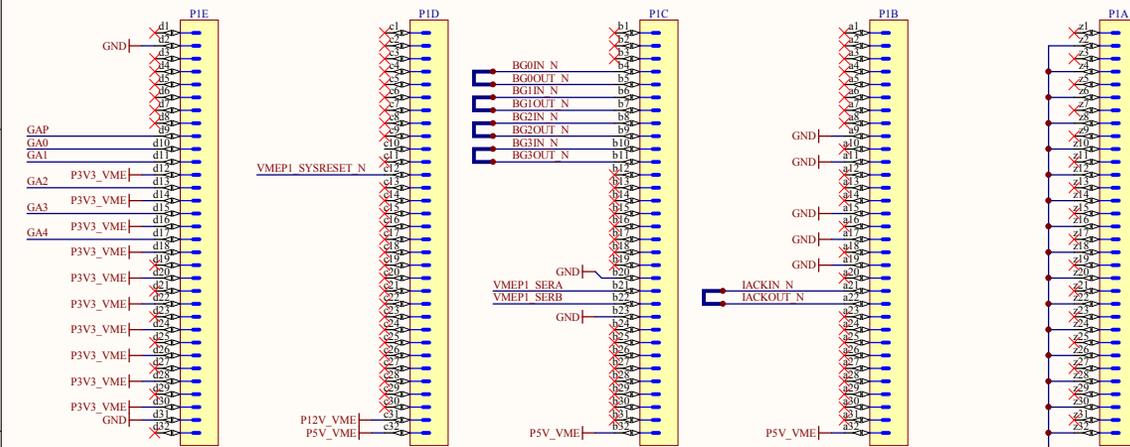


FPGA HEADER IN N[6..1]



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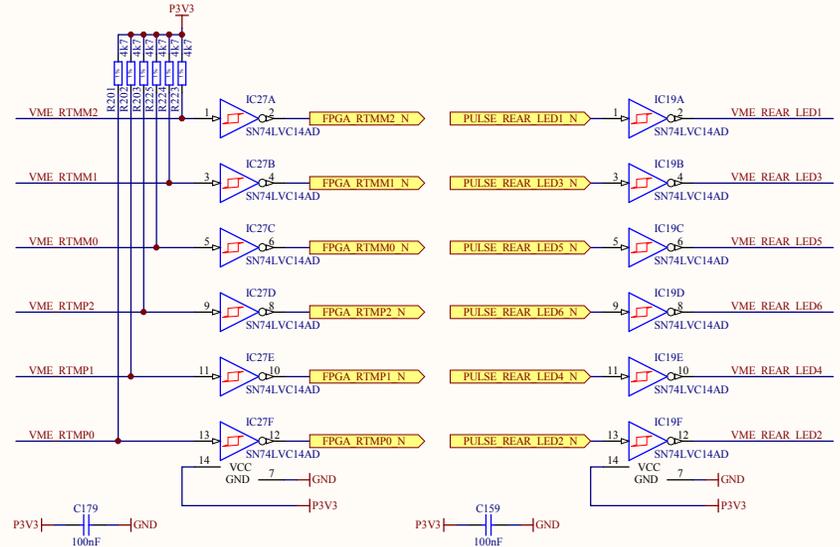
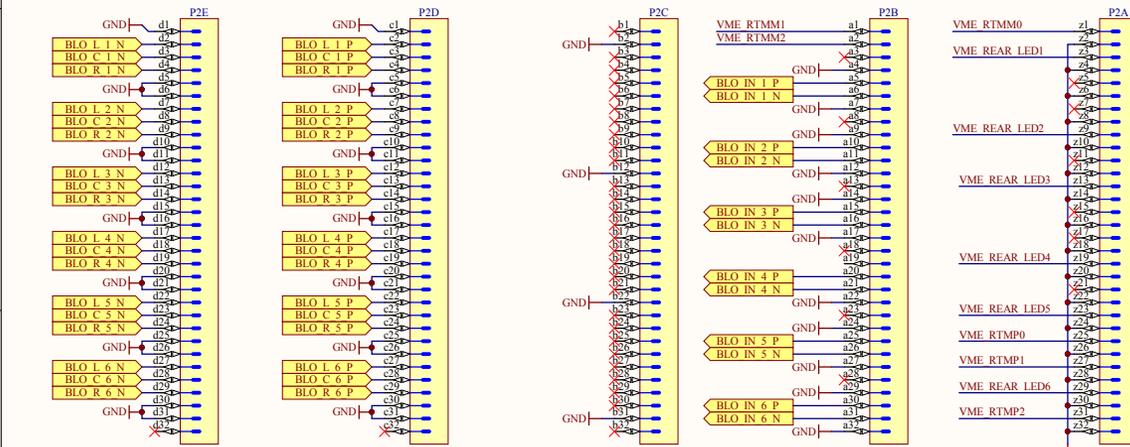
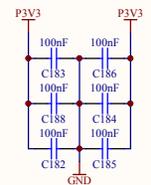
Utility Bus Signal: see page 199
 ANSI/VITA 1-1994
 Output configurations in page 230
 SYSRESET_N
 Open collector



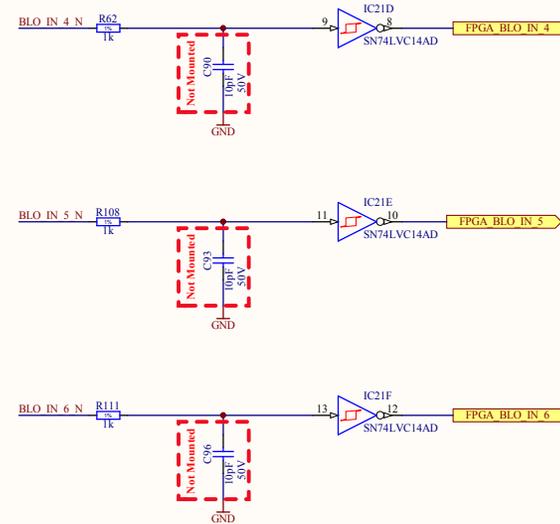
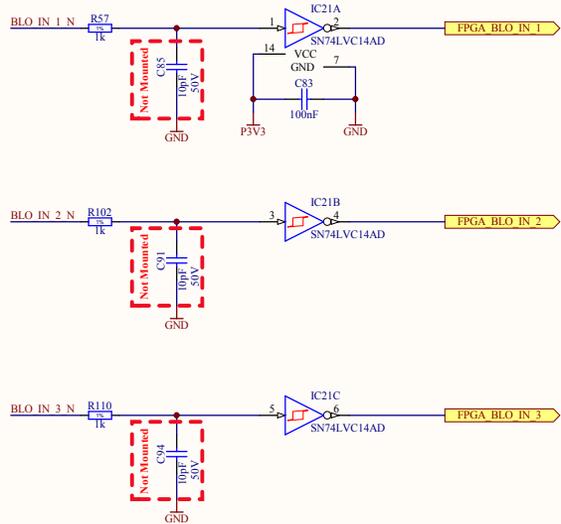
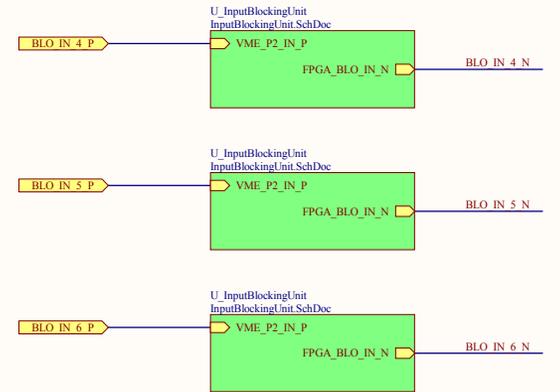
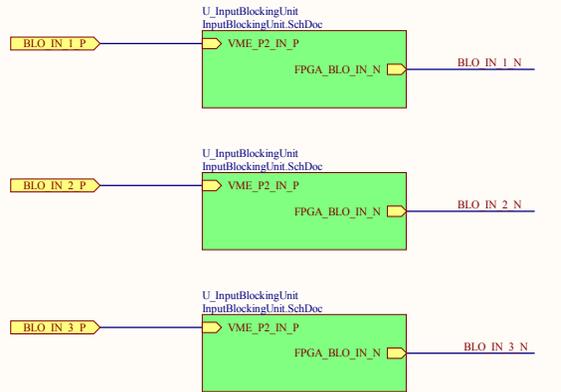
As each block of BLO+ [X]_n, where X=L, C, R] will be triggered at the same time, cross talk should not be so critical. However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo. Signals with more spectral power in higher frequencies should be routed more carefully, so it is better to leave the easiest paths to them. In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used. Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

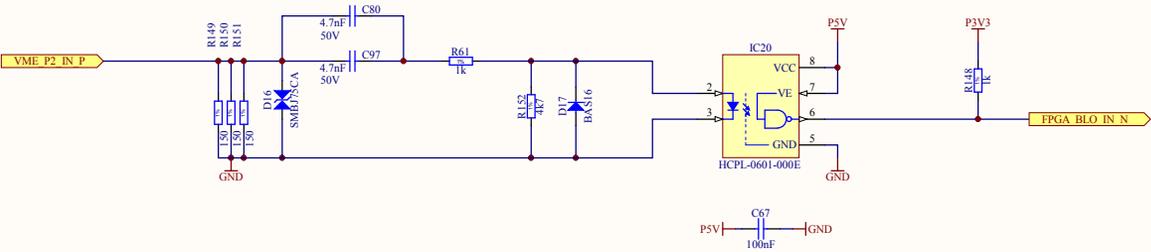


Project/Equipment		Standard Blocking Pulse Repeater	
Document		Conv-TTL-Blo VME64X	
Designer		Carlos Gil Soriano	03/10/2012
Drawn by		Carlos Gil Soriano	
Check by		EVB, MC, TW	
Last Mod.			22/10/2012
File		VME64xConn_SchDoc	
Print Date		22/10/2012 17:27:19	Sheet 8 of 14
EDA-02446-V2-0		A3	1

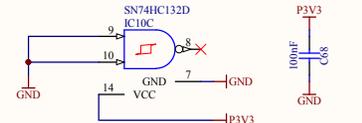
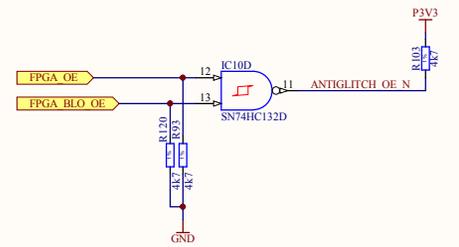
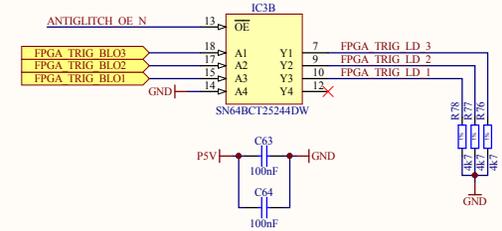
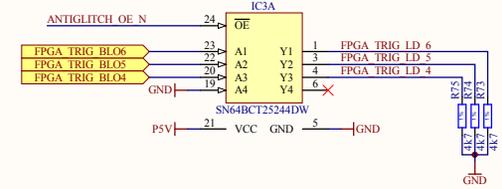
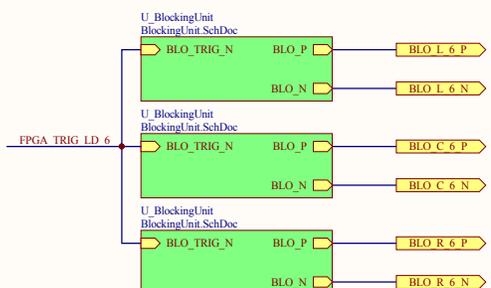
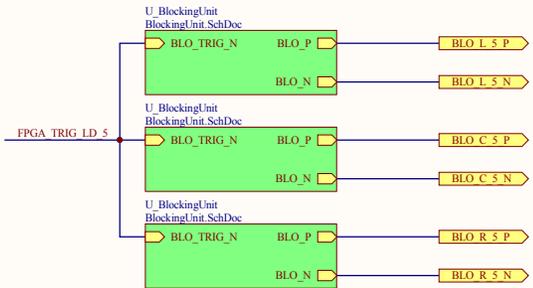
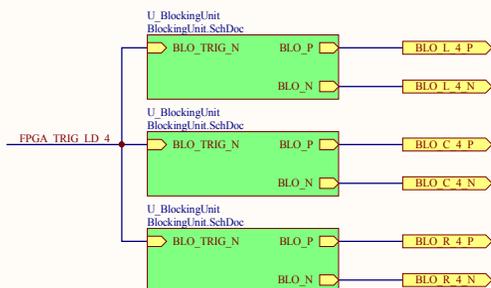
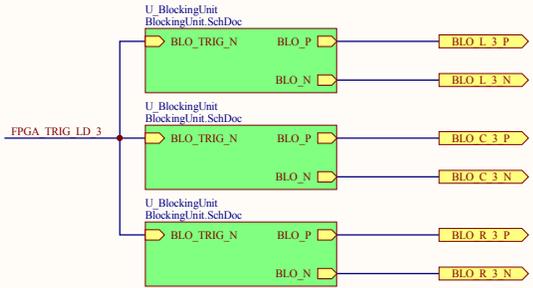
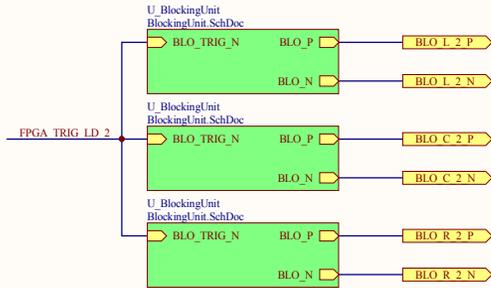
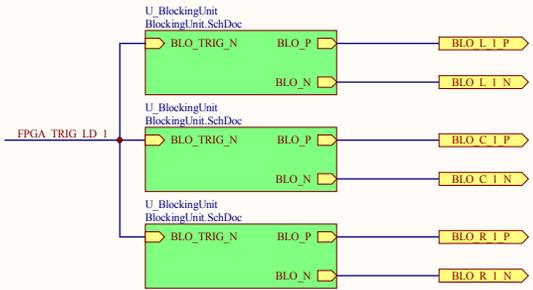
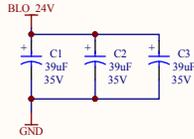


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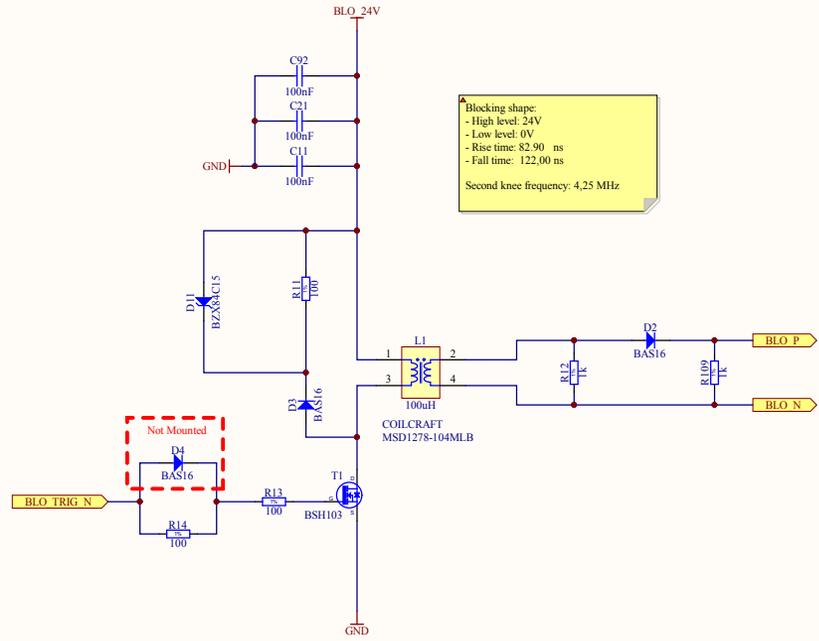
Input waveforms:
 nominal 24V Std.Blocking
 minimum 5V Std.Blocking



Project/Equipment		Standard Blocking Pulse Repeater	
Document		Conv-TTL-Blocker INPUT UNIT	
 European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Designer	Carlos Gil Soriano
		Drawn by	Carlos Gil Soriano
		Check by	EVB, MC, TW
		Last Mod.	22/10/2012
		File	InputBlockingUnit_SchDoc
Print Date	22/10/2012 17:27:19	Sheet	10 of 14
EDA-02446-V2-0		Size	A3



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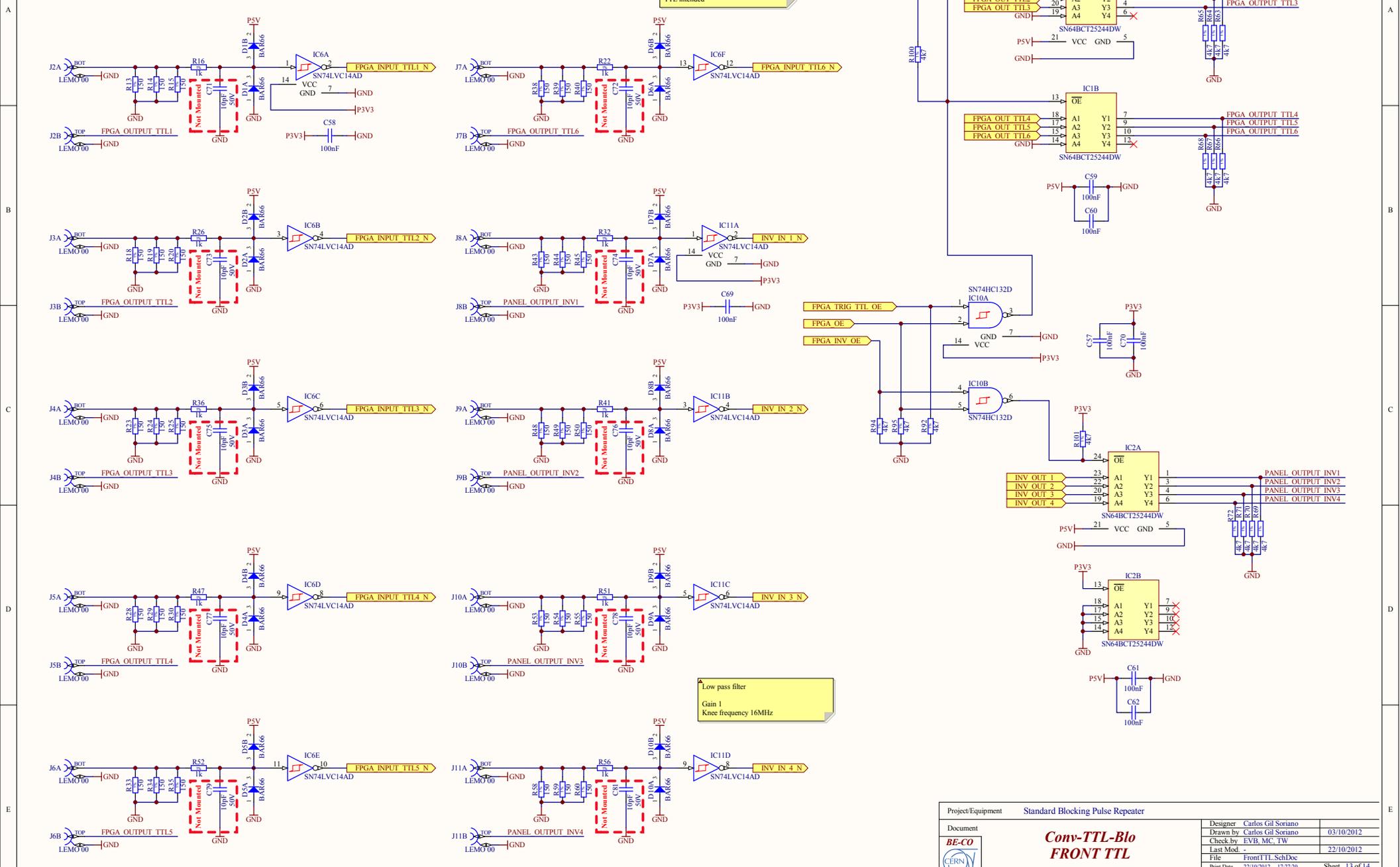
Blocking shape:
 - High level: 24V
 - Low level: 0V
 - Rise time: 82.90 ns
 - Fall time: 122.00 ns
 Second knee frequency: 4.25 MHz

Project/Equipment		Standard Blocking Pulse Repeater	
Document		Conv-TTL-Bo OUTPUT UNIT	
Designer		Carlos Gil Soriano	03/10/2012
Drawn by		Carlos Gil Soriano	
Check by		EVB, MC, TW	
Last Mod.		-	22/10/2012
File		BlockingUnit_SchDoc	
Print Date		22/10/2012 17:27:20	
Sheet		12 of 14	
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02446-V2-0	A3 1

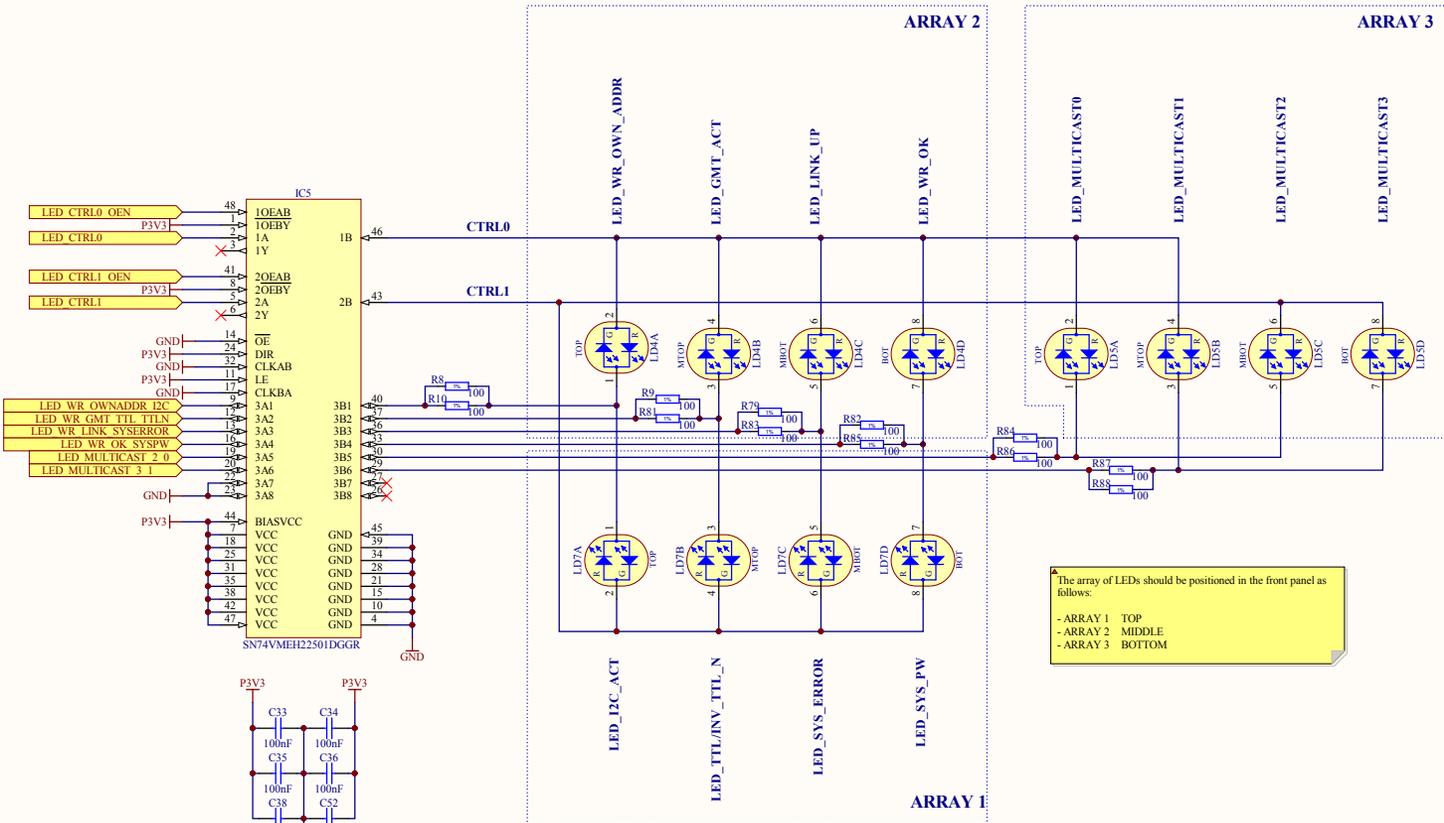
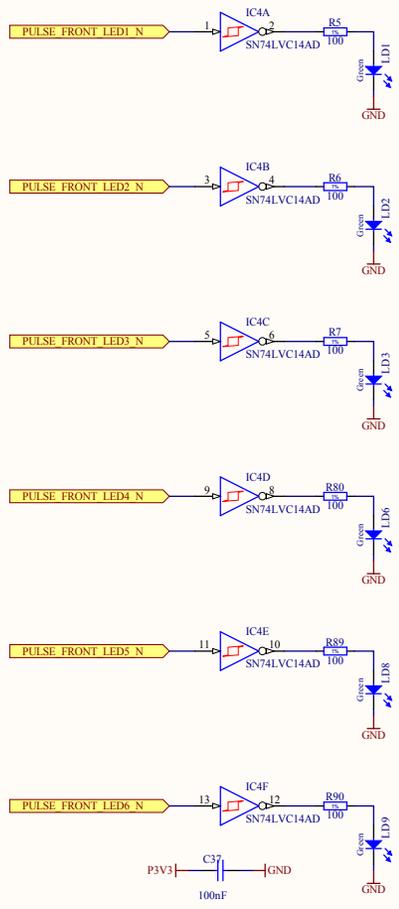
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Input voltage up to 5.5V
 TTL intended

Low pass filter
 Gain 1
 Knee frequency 16MHz

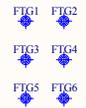
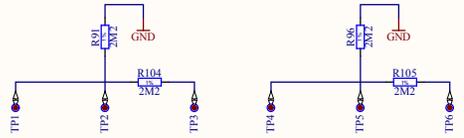


Project/Equipment		Standard Blocking Pulse Repeater	
Document		Conv-TTL-Blo FRONT TTL	
			
Designer		Carlos Gil Soriano	03/10/2012
Drawn by		Carlos Gil Soriano	
Check by		EVB, MC, TW	
Last Mod.		-	22/10/2012
File		FrontTTL_SchDoc	
Print Date		22/10/2012 17:27:20	
		Sheet	13 of 14
			A3 1
		EDA-02446-V2-0	
		European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	



The array of LEDs should be positioned in the front panel as follows:
 - ARRAY 1 TOP
 - ARRAY 2 MIDDLE
 - ARRAY 3 BOTTOM

ESD discharge strips (top and bottom of the card)



Project/Equipment	Standard Blocking Pulse Repeater		
Document	BE-CO Conv-TTL-Blo FRONT PANEL		
Designer	Carlos Gil Soriano	03/10/2012	
Drawn by	Carlos Gil Soriano		
Check by	EVB, MC, TW		
Last Mod.	-	22/10/2012	
File	FrontPanelLeds.SchDoc		
Print Date	22/10/2012 17:27:20	Sheet 14 of 14	Page 1
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland			EDA-02446-V2-0