

Report of issues in CONV-TTL-BLO v1.0

EDA-02446-V1-0

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Abstract

CONV-TTL-BLO V1-0, internally named as **EDA-02446-V1-0**, has several **bugs to be fixed in V2**. The present report covers them all.

Revision history		
HDL version	Module	Date
1.0	Initial report	October 2, 2012

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1 Power supply 24 volts

Some resistors and capacitors should be changed to achieved better stability in the 24 volts power supply rail.

OHWR issues 452, 455, 458	http://www.ohwr.org/issues/458
After carefully checking the design (against the calculations provided by TI in its datasheet and SwitcherPro Desktop for checking the gain and phase margin) some modifications are submitted for an improved control of the 24V rail.	
<p>DESIGN VALUES</p> <ul style="list-style-type: none"> • Switching Frecuency: 475Khz • Crossover Frecuency: 23.75KHz • Vin : 12V • Vout : 24V • Feedback network: R_{high} 50K, R_{low} 1K51 • Compensation network: R_{comp} 13K35, C_{comp} 4.7μF, C_{pole} 68μF (upto 100μF) • RC network: R_{RC} 335K, C_{RC} 100pF 	

Table 1: Issue 458: 24 volts power supply

CHANGES OF COMPONENTS

R_{high}	
Resistor	Value
R231	not changed (10K)
R232	not changed (10K)
R233	not changed (10K)
R235	not changed (10K)
R234	4K7 changed to 10K

R_{low}	
Resistor	Value
R229	100 changed to 510R
R230	4K7 changed to 1K

\mathbf{R}_{comp}	
Resistor	Value
R254	10K changed to 4K7
R255	10K changed to 4K7
R256	10K changed to 1K
R257	10K changed to 100R
R258	not changed (10K)

\mathbf{C}_{comp}	
Capacitor	Value
C45	not changed (4.7 μ F)

\mathbf{C}_{pole}	
Capacitor	Value
C190	100pF removed
C191	100pF changed to 68pF (100pF can be used, as well)

\mathbf{R}_{RC}	
Resistor	Value
R261	470K changed to 100K
R262	not changed (470K)
R263	not changed (470K)

\mathbf{C}_{RC}	
Capacitor	Value
C196	not changed (100pF)

\mathbf{R}_{isns}	
Resistor	Value
R259	100R changed to 1K

Output ceramic capacitors	
Capacitor	Value
C192	removed
C193	removed
C189	removed

2 Power line filter to be added

OHWR issue 517	http://www.ohwr.org/issues/517
<p>In CONV-TLL-BLO v1 no power supply filters are mounted. Due to the logic families used in the design, noise in the vicinity of 60MHz to 150MHz was expected. Spectral measurements in the power rails and FFT null-magnetic tests checked the presence of this noise. Thus, a filter schema for this band is needed. The following simple solution consisting of a one-stage pi filter with the following values:</p> <ul style="list-style-type: none">• Capacitor to external power rails: 22μF ceramic• Capacitor to board input power rails: 150μF OSCON• Inductor: Murata BLM41PG181SN1L <p>This filter stage is mounted in CONV-TTL-RS485, as well.</p>	

Table 2: Issue 517: Power line filter

3 Optoisolator resistor

OHWR issue 520	http://www.ohwr.org/issues/520
<p>Blocking input should change the value of one resistor to reduce degradations of diode in the optoisolator. Taking EDA schematics document as reference and going to page 10. R222 resistor, which is 100R must be replaced for 1K. Thus, a maximum value of 22 mA is driven into the LED of the optoisolator. Do the same for R227,R219, R217, R215 and R226.</p>	

Table 3: Issue 520: Optoisolator resistor

CHANGES OF COMPONENTS

Resistor	Value
R215	100R changed to 1K
R217	100R changed to 1K
R219	100R changed to 1K
R222	100R changed to 1K
R226	100R changed to 1K
R227	100R changed to 1K

4 Bad VME64x connections

It represents a problem when other boards try to use the bus granted pins or interrupt acknowledge lines.

OHWR issue 502	http://www.ohwr.org/issues/502
Some VME64 lines are misconnected. Daisy-chain <i>BGxIN_N</i> , <i>BGxOUT_N</i> and <i>IACKIN_N</i> , <i>IACKOUT_N</i> .	

Table 4: Issue 502: VME64x misconnections

5 Blocking driver stage

5.1 Misconnection of output enable pin

OHWR issue 463	http://www.ohwr.org/issues/463
In IC3, there's a bad net name yielding into an unwanted floating pin (pin 13). The net name in the corresponding schematic page must be changed.	

Table 5: Issue 463: bad net name in IC3

CHANGES IN SCHEMATICS

IC3	
Pin number	Value
13	OE_N_ANTIGLITCH changed to ANTIGLITCH_OE_N

6 Blocking module

7 Square LED array

OHWR issue 570	http://www.ohwr.org/issues/570
<p>The front panel three LED array will be changed by a Dialight 568 model.</p> <p>This model is a bicolour (red-green) 4-LEDs array, which will be driven by a VME buffer to reduce BOM.</p> <p>Already done in CONV-TTL-RS485.</p>	

Table 6: Issue 570: square LED array

8 Other issues

8.1 Board Test Points

OHWR issue 449	http://www.ohwr.org/issues/449
Test points should not be mounted in production boards.	

Table 7: Issue 449: Test points

8.2 White Rabbit connector in front panel

It has been detected in different boards (such as WR repetitors) that the WR hole in the front pannel was not properly designed.

It seems that the current size and spacing of the WR connector is OK in V1, however the issue is reported below:

OHWR issue 450	http://www.ohwr.org/issues/450
WR connector socket should be rechecked for better plugging quality.	

Table 8: Issue 450: WR connector in front panel

8.3 Components not to be mounted

OHWR issue 501	http://www.ohwr.org/issues/501
Resistor R98 should not be mounted. Resistor R137 should not be mounted.	

Table 9: Issue 501: not to be mounted resistors

8.4 Protection for misconnections of the inputs

A double control mechanism must be added in the FPGA to avoid damage in the Blocking output stage.

OHWR issue 503	http://www.ohwr.org/issues/503
<p>If the all the input channels of the board are connected to a high level and the RTM outputs are all parallel terminated to 50 Ohms the 24V power supply will blow up. To avoid this, some control must be added in the FPGA, first to detect and then to report via I2C. A protection fuse is currently not installed in the 12V rail. It's needed.</p>	

Table 10: Issue 503: Protection for misconnections of the inputs

The proposal is to trigger event upon edge detection, and measure the level of the inputs to report problems back through the I2C connection.

8.5 12 volts fuse to be added

OHWR issue 504	http://www.ohwr.org/issues/504
<p>After writing down a list of test to be performed, it was found that some configurations can harm the board. If all the inputs are connected to '1', the FPGA is programmed to generated a periodic signal of 3us with 50% duty cycle. If all the outputs are terminated with 50 Ohms, irreversible damage will be caused to the 24V Power Supply. The power supply is able to provide 2.5 A (and up to 3.5A) in 24V. A fuse targeted to solve that problem must be placed in the 12V rail.</p>	

Table 11: Issue 504: 12 volts fuse to be added

8.6 Add silkscreen for fuses

OHWR issue 505	http://www.ohwr.org/issues/505
It should be added an easy to read silkscreen for every fuse in next V2 board.	

Table 12: Issue 505: add silkscreen for fuses