

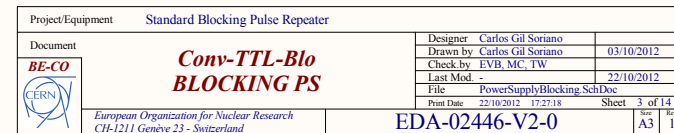
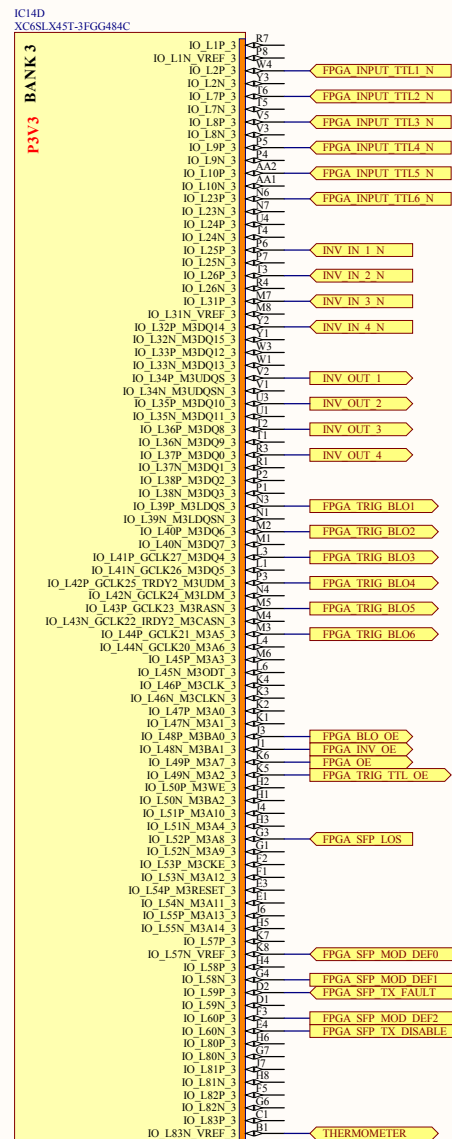
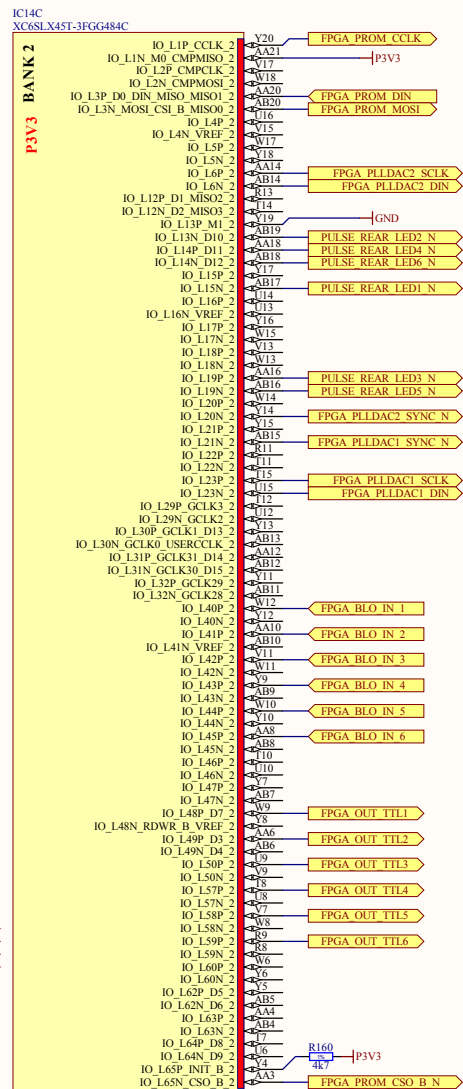
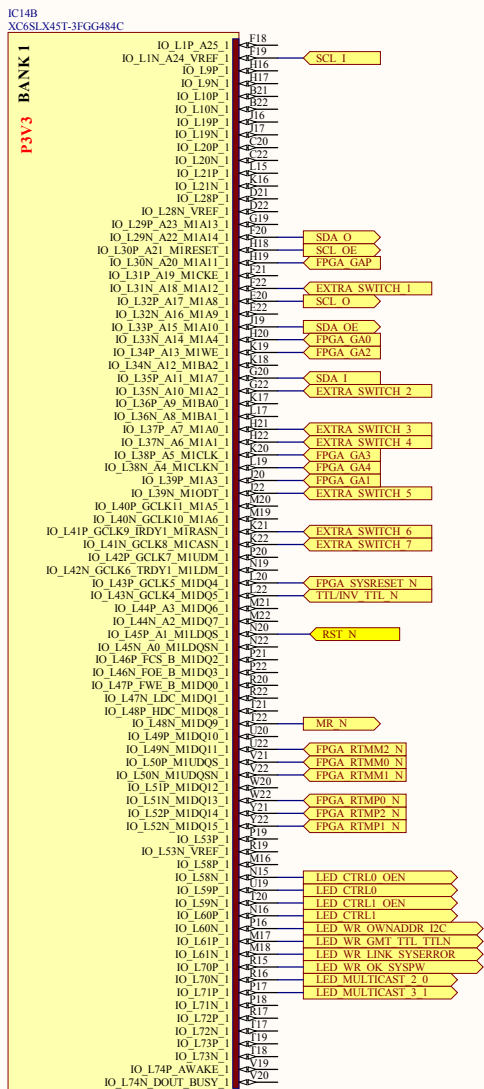
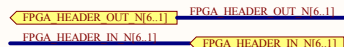
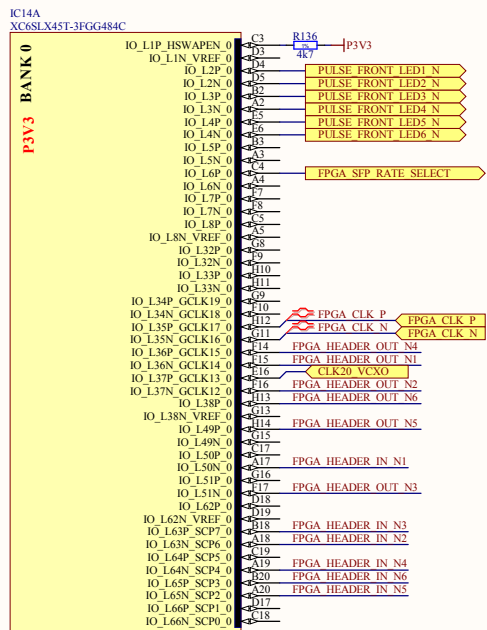


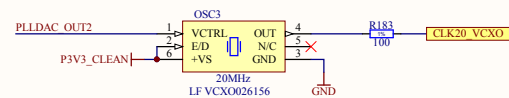
Project/Equipment		Standard Blocking Pulse Repeater	
Document		Designer	Carlos Gil Soriano
 <div style="text-align: center;"> <h1 style="color: red;">Conv-TTL-Blo FPGA PS</h1> </div>		Drawn by	Carlos Gil Soriano
		Check by	EVJB, MC, TW
		Last Mod.	22/10/2012
		File	FPGAsps SchDoc
 European Organization for Nuclear Research CH-1211 Geneva 23, Switzerland		Print Date	22/10/2012 17:27:17
		Sheet	2 of 14



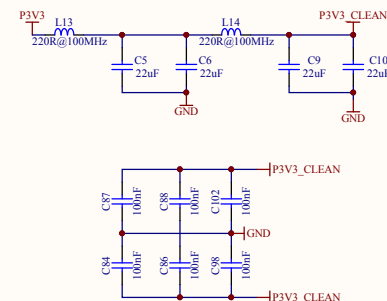
▲ To allow high SerDes ratios, leave all the trigger inputs and outputs in _P pins.

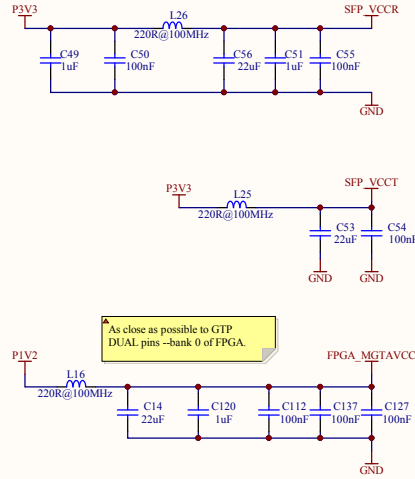
See Xilinx's document UG381, chapter 3 for further information.





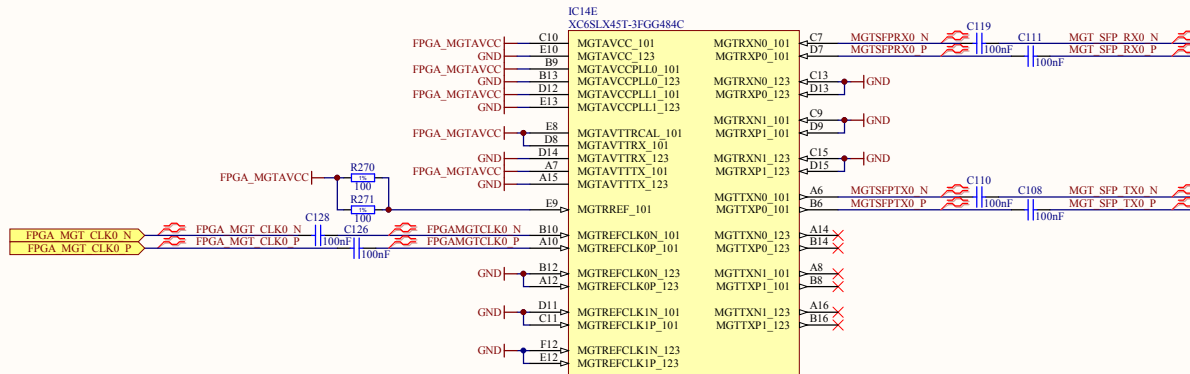
CDCM61004 configuration:
 LVDS outputs
 PRESC DIV = 4
 FB DIV = 20
 OUT DIV = 4
 All config inputs have internal
 pull-ups.
 Input = 25 MHz
 Output = 125 MHz



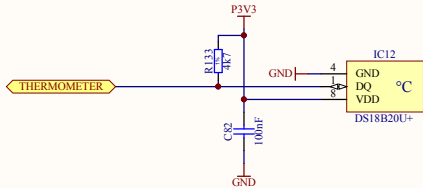


As close as possible to GTP
DUAL pins -bank 0 of FPGA.

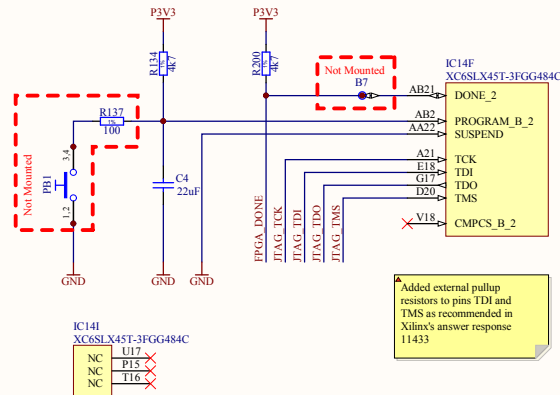
The trace length from the resistor pins to the FPGA pins MGTREF
and MGTITRCL must be equal in length and geometry



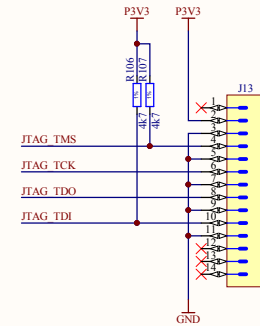
Thermometer will be used to have a FPGA unique ID



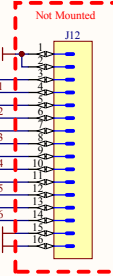
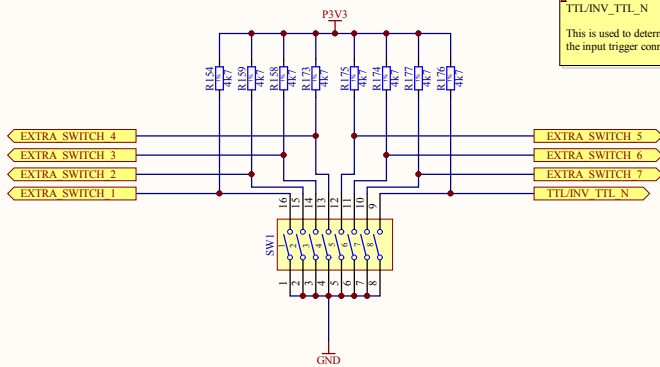
PROGRAM_B must be asserted low for more than 500ns



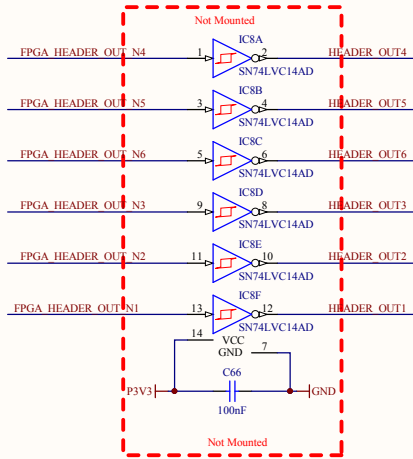
Added external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433



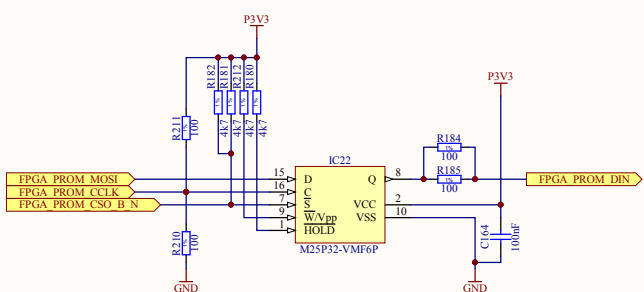
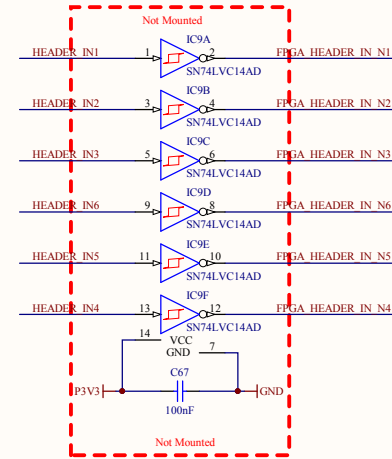
TTL/INV_TTL_N
This is used to determine the level of the input trigger connector

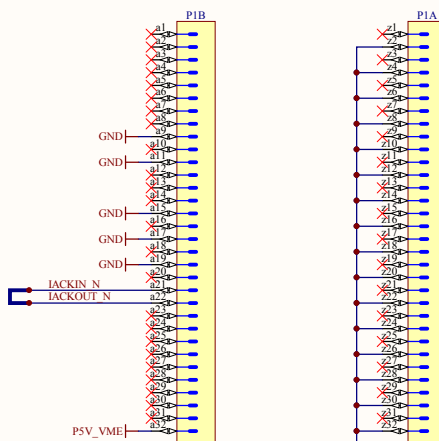
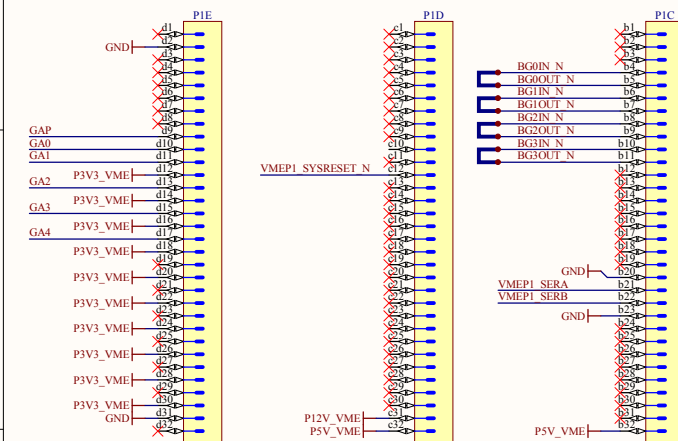


FPGA HEADER OUT N[6..1] FPGA HEADER OUT N[6..1]



FPGA HEADER IN N[6..1] FPGA HEADER IN N[6..1]

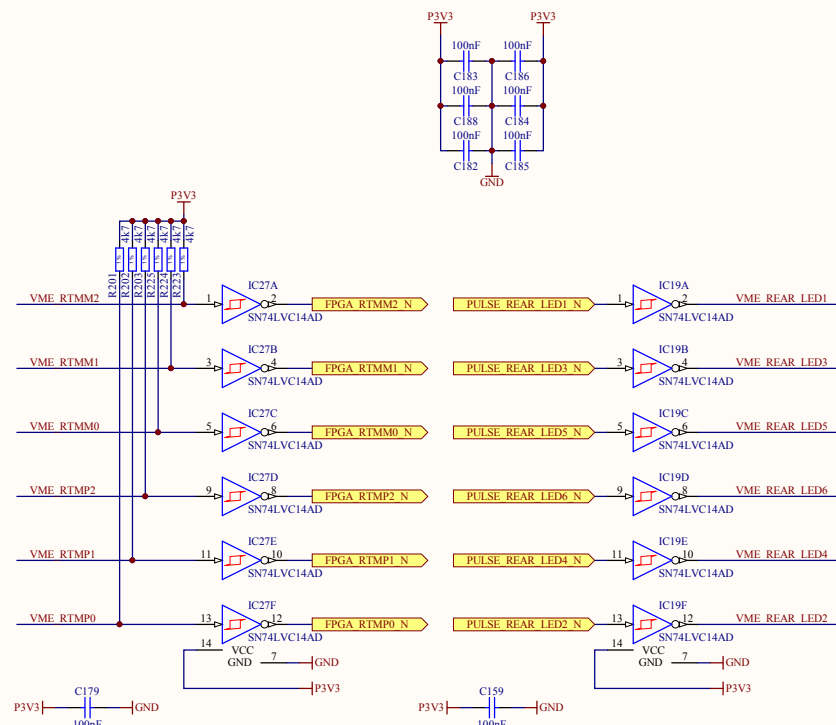
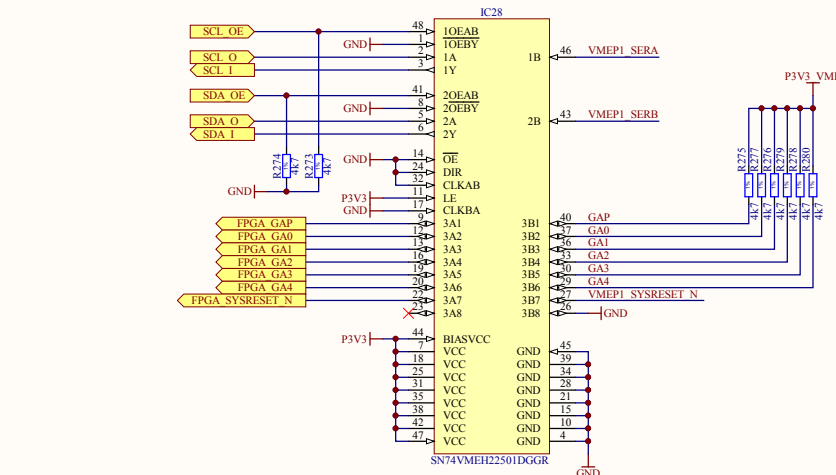
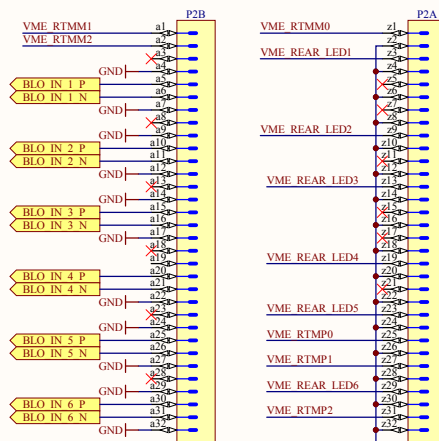
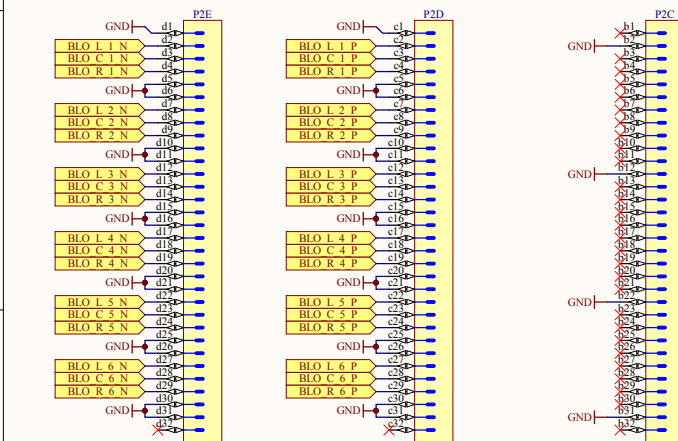


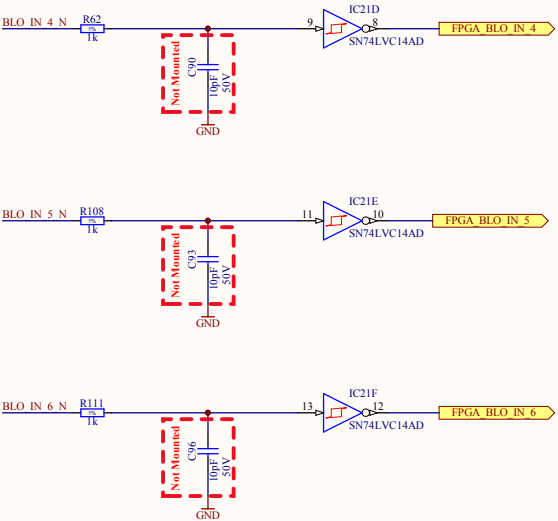
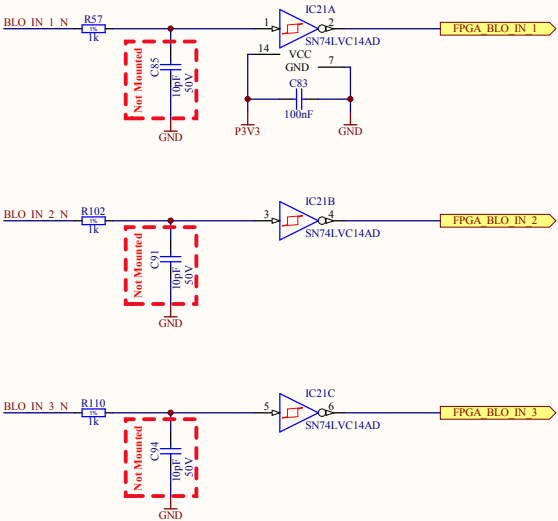
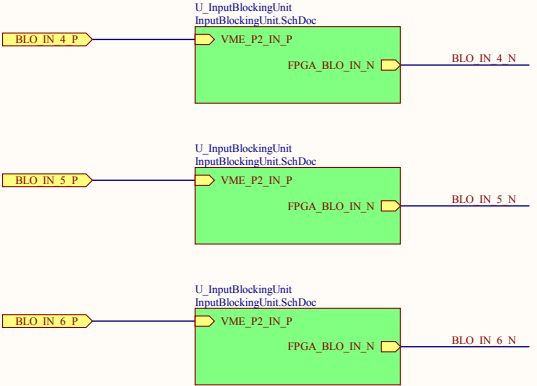
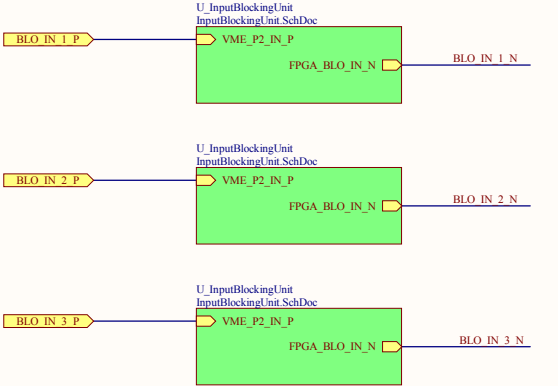


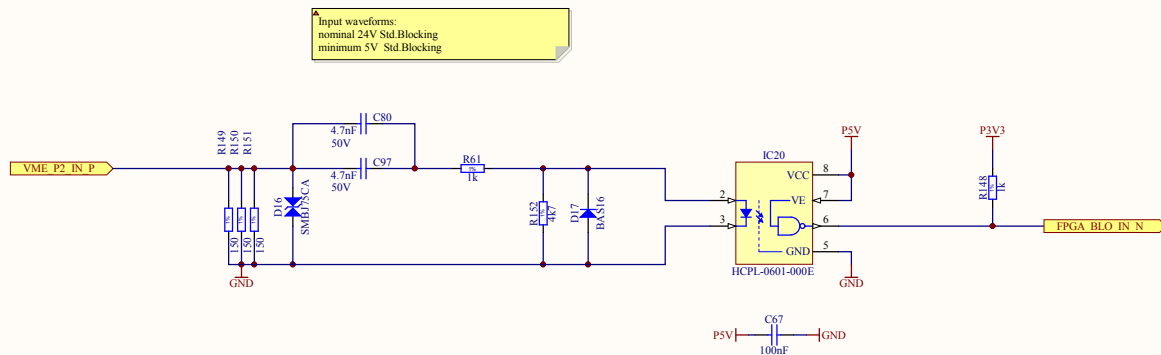
As each block of BLO+ [X]_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical. However, it would be better group the signals as it is shown and leave group between sets of signals triggered by different sources.


As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo. Signals with more spectral power in higher frequencies should be routed more carefully, so it is better to leave the easiest paths to them. In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used. Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.







Project/Equipment		Standard Blocking Pulse Repeater	
Document		Designer	Carlos Gil Soriano
 Conv-TTL-Blo INPUT UNIT		Drawn by	Carlos Gil Soriano
		Check by	EVB, MC, TW
		Last Mod.	-
		File	InputBlockingUnit.SchDoc
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