Input connection for the Standard Blocking Repeater: CTARA and CTDAH

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History of changes

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Date	Pages	Changes
August 29, 2011	All	Initial submission
September 21, 2011	All	Added references to Standard Blocking
September 23, 2011	All	Modified chapter 1

System Description and Purpose This brief document describes the reflection problem when an input signal is passed to the Standard Blocking Repeater formed by CTARA and CTADH VME64x boards. Reflections must be carefully studied when the input signal is daisy-chained so as to avoid signal degradation.

Contents

1 Input connection

One of the desired functionalities of the Standard Blocking Repeater formed by CTARA and CTDAH boards is loopbacking the input signal between two o more channels. When a signal is daisy-chained special care must be taken to have control on the reflections that are happening in the input. For instance, in old 8 and 16 Channel Repeaters the picture is as follows:

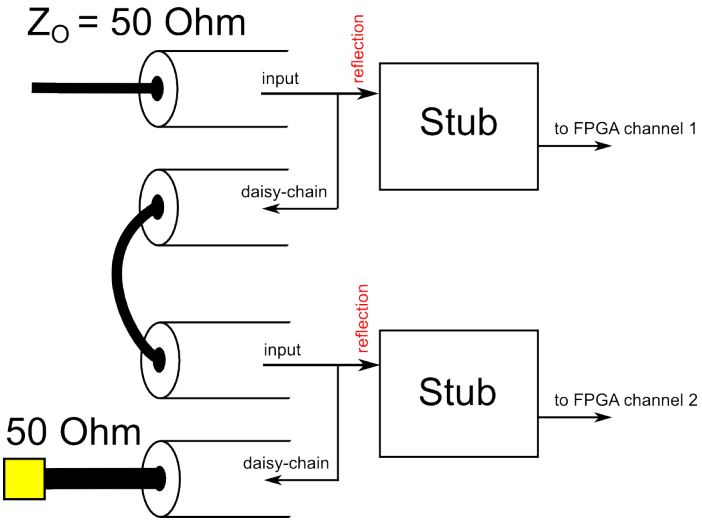

Figure 1: Daisy-chain in old Channel Repeaters

it can be seen that every channel that bypasses the signal represents a stub that produces reflections.

1.1 Line termination

The main issue affecting the integrity of the bypassed signal is reflection. Reflections should be taking into account when transmission line theory can be applied to a circuit. As stated in [1] or [2] a line should be better considered as a transmission line when the electrical distance of the cable -or trace- is higher than one sixth of its electrical distance:

$$L_{trace} \geq \frac{L_{electrical}}{6} = \frac{v_{prop} t_{rise}}{6} \tag{1}$$

In our design, the three input signals that can be applied with its relevant reflections parameters are shown below:

	t_{rise}	$L_{electrical_{threshold}}$
TTL	5 ns	16.6 cm
TTL/bar	5 ns	16.6 cm
Standard Blocking	150 ns	5 m

Even in the best electrical lenght case -which corresponds to Standard Blocking [3]-, it is necessary to apply a transmission line approach. Hence, properly termination of lines is highly recommended so as to avoid reflections.

2 Standard Blocking Repeater Daisy-Chain Configurations

The image below shows the conversion path of the pulse input to the Standard Blocking output.

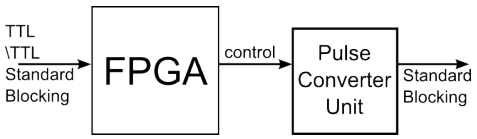

Figure 2: Pulse conversion schema

An input signal is received in the FPGA after conditioning. Then a control signal is generated in the FPGA to the Pulse Converter Unit, which will output a Standard Blocking compliant pulse. Thus, as the generation of the pulse depends either on the input signal or the input control, two daisy-chain strategies are:

- **Copying input signal: FPGA not bypassed**
- **Copying control signal: FPGA bypassed**

The table summarizes the properties of every layout:

Stubs	Daisy-chain signal	Channel interconnection	Added
FPGA not bypassed			
YES	Input signal	Any order	-
FPGA bypassed			
Option A			
NO	Control signal	Any order	Less reflections FPGA control
Option B			
NO	Control signal	Contiguous	Less reflections FPGA control Higher channel integration

2.1 Copying input signal

This was the technique used in 8 and 16 Channel Repeaters. The input pin was directly connected to the daisy-chain output of the same channel.

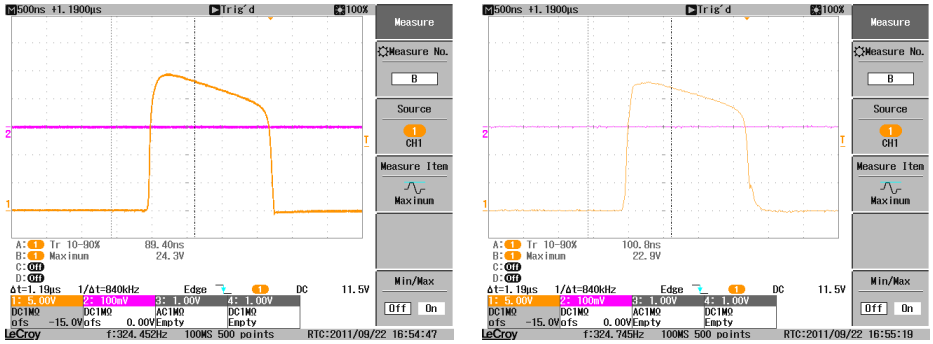

Figure 3: Standard Blocking input when no daisy-chained -left- and after 6 daisy-chain stages -right-

2.1.1 Signal degradation in Channel Repeaters boards

So as to better understand the effects of this kind of daisy-chaining, a set of measures where taken in a 16 Channel Repeater board.
A Standard Blocking pulse signal was taken from the Pulse Generator -*boite d'impulsions*-, routed to the 16 Channel Repeater and the signal was analyzed in a Lecroy WaveJet 324A oscilloscope.
The cables used were 50 Ω cables of different lengths. To connect the Pulse Generator with the first channel a 16 *ns* delay cable was used. For the rest of daisy-chain connections 1 *ns* delay cables were attached. Finally, a 6 *ns* cable is connected to the oscilloscope.

Standard Blocking input

In this case, bypassing a slow signal, such a Standard Blocking, is not affecting dramatically to the signal integrity. In the next page two images are attached. The first one shows the output of a 50 Ω terminated channel which is not daisy-chained. The second one shows the signal after daisy-chaining six channels and 50 Ω termination in the last one.

As it can be seen for the case of Standard Blocking, the most noticeable effect is a degradation of the rise time and a expected lower high level.

Fast TTL inputs

In this case, so as to obtain fast TTL inputs, the signal was taken from CTRV board. As the input pulses have a rise time of 5 ns, a higher degradation of the signal is expected. Experimental results point out that no significant difference is observed when the signal is daisy-chained.

No daisy-chained input captures

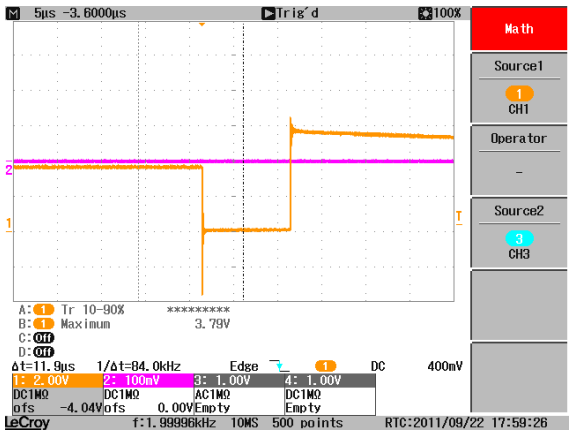

Figure 4: Fast TTL when no daisy-chained

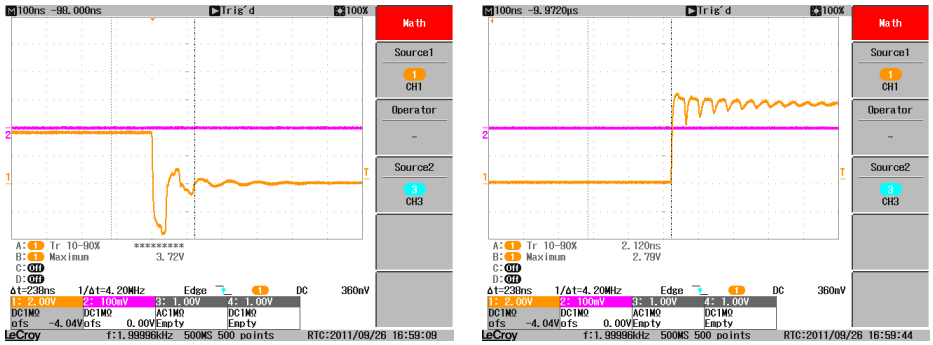

Figure 5: No terminated line: Detail of the fall and rise edge

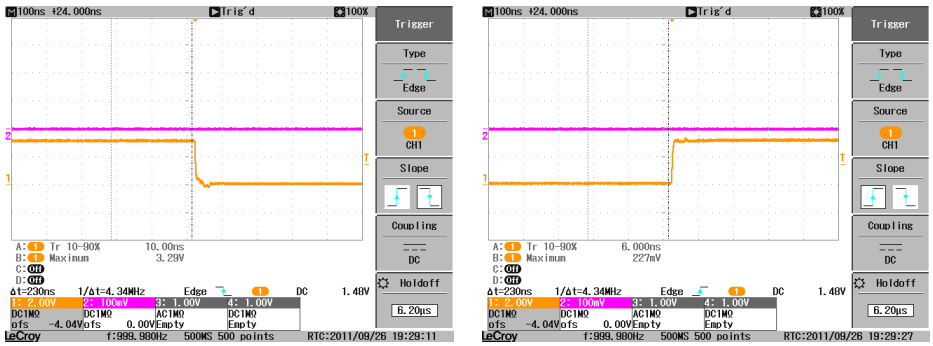

Figure 6: 50Ω terminated line: Detail of the fall and rise edge

6 daisy-chained channels input captures

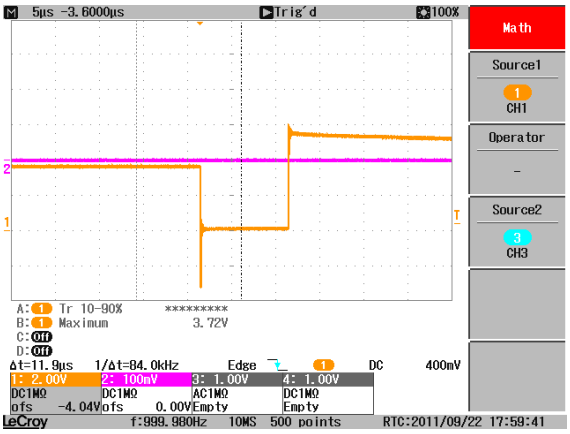

Figure 7: Fast TTL input after 6 daisy-chain stages

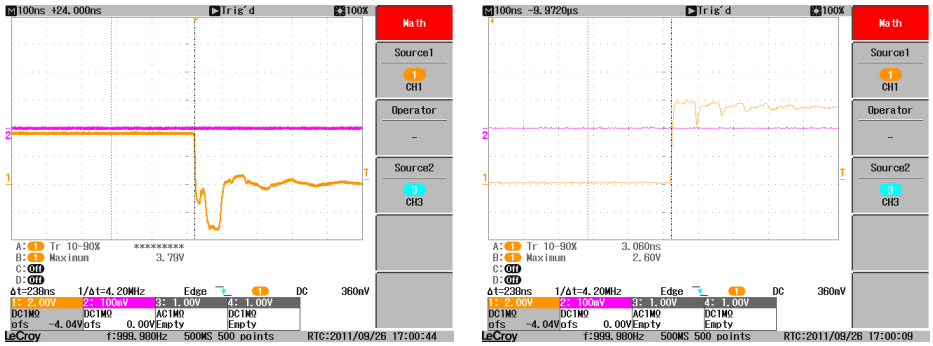

Figure 8: Detail of the fall and rise edge

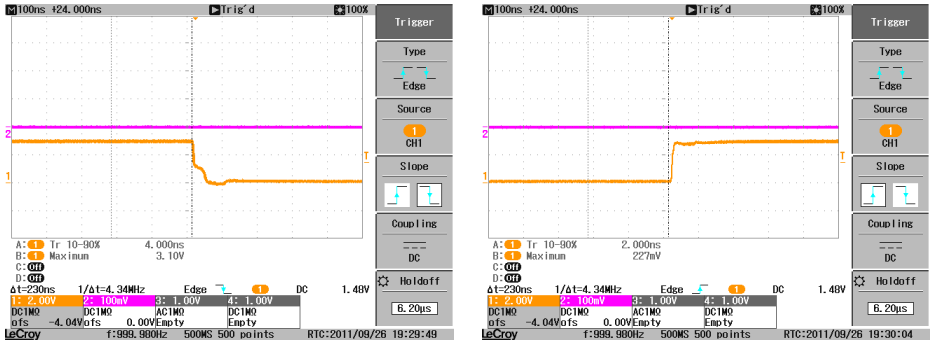

Figure 9: 50Ω terminated line: Detail of the fall and rise edge

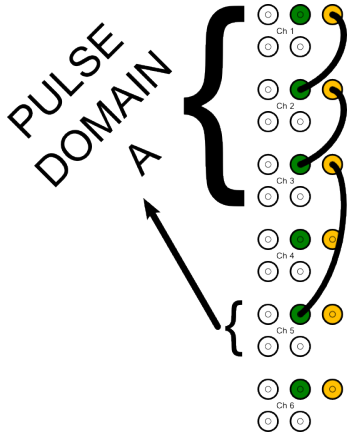

Figure 10: Daisy-chain: Option A

2.2 Copying control signal

With this different approach, the FPGA internally daisy-chain the control signal that generates the Standard Blocking pulses. By doing this, the input signal is never daisy-chained, theoretically improving signal integrity. Two options are offered as suitable solutions for bypassing control signal between channels, but the main idea beyond them is the same: detecting the daisy-chained channels and internally copy the control signal between them.

Copying control signal improvements over copying input signal

- *Less reflections*: as no stubs are added to the line for every daisy-chained channel, reflection effects are lesser.
- *FPGA control*: the daisy-chain topology of a card can be easily known by the FPGA. Thanks to this, more complete control techniques can be implemented to detect where a failure is happening throught the signal repetition path.

In **Option A** there are two connectors used for daisy-chain. One of this connectors is a daisy-chain input, the other is a daisy-chain output. So as to enable the daisy-chain operation, the operator must connect one daisy-chain output of one channel with a daisy-chain input of a different channel. It is not necessary that the channels are contiguous, thus providing more flexibility to the operator when it comes to the installation process.

After the installation, a daisy-chain detection process must be carried out by the FPGA. Instead of outputting the signal through the daisy-chain connectors, it is internally loopbacked between the detected daisy-chained channels. By internally loopbacking, the associated delay is reduced. A

maximum FPGA bypassing delay must be specified.
Option B represents a different approach to the same problem. Instead of having two dedicated daisy-chain connectors, there is a switch in every channel. This switch allows loopbacking the signal of the current channel to, and only to, the next channel.
After setting up the switch in the desired position, the FPGA will detect its state and will proceed -or not- to internally loopback the signal to the next channel.

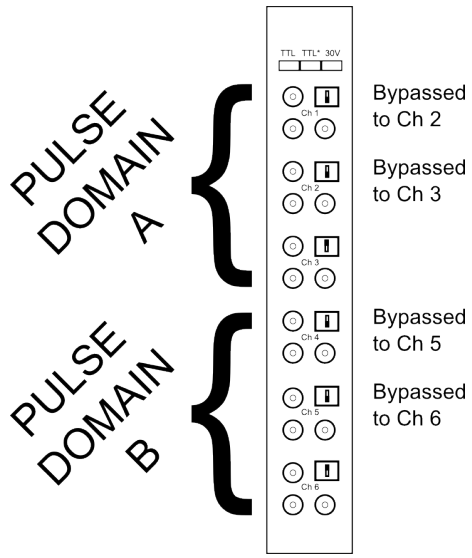

Figure 11: Daisy-chain: Option B

Option B improvements over Option A

- *Higher channel integration*: due to the fact that less connectors are needed to daisy-chain, a higher integration of channel can be made in CTARA board.

References

[1] H.W. Johnson and M. Graham. *High-speed digital design: a handbook of black magic*. Prentice Hall PTR Signal Integrity Library. Prentice Hall, 1993.

[2] E. Bogatin. *Signal and power integrity–simplified*. Prentice Hall Modern Semiconductor Design Series. Prentice Hall, 2009.

[3] C. Gil Soriano. Standard Blocking Output Signal Definition for CTDAH board, September 2011. `http://www.ohwr.org/documents/109`.