Flyback circuit outputting Standard Blocking for CTDAH

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System Description and Purpose A flyback circuit topology is exposed as a feasible solution for the Pulse Converter Unit. The document shows the theoretical analysis, simulation and measurements done of a flyback circuit to be employed in the Pulse Converter Unit. The present solution offered takes a starting point from Level Conver board by C. Dehavay [1] and improves it so as to comply with Standard Blocking requirements [2].

History of changes

This document version has been checked by:

This document version has been approved by:

Date	Pages	Changes
September 16, 2011	All	Initial submission
September 21, 2011	All	Revised to comply with Standard Blocking Definition[2]

Contents

1 Introduction

A flyback circuit configuration consist on a Power MOSFET that can open or shortcuit one pole of the primary winding of a transformer to ground. By doing this, the primary inductance of the transformer experiences a voltage virtually copied from the voltage supply it has in the other pole of the primary winding.

When the Power MOSFET is conducting, the secondary winding of the transformer outputs the voltage to the load. Thus, the load forces a current along each of the windings of the transformer. Apart from this current, a magnetizing current is present in the primary winding. The magnetizing current ramps up with a factor scale dependent on the primary inductance and the voltage along it. Depending on the R_{ON} value of the Power MOSFET, the voltage along the primary inductance can experience a small tilt, yielding that the magnetizing current will not built up linearly. We will assume now on that R_{ON} effect is negligible on the magnetizing current ramp –then, it will increase linearly.

Attention should be paid to the saturation current of the transformer to avoid irreversible damage. Because of this, it will be clearly stated in this document the maximum pulse width it can be outputted and the time it will take to the recovery phase to drain enough magnetizing current.

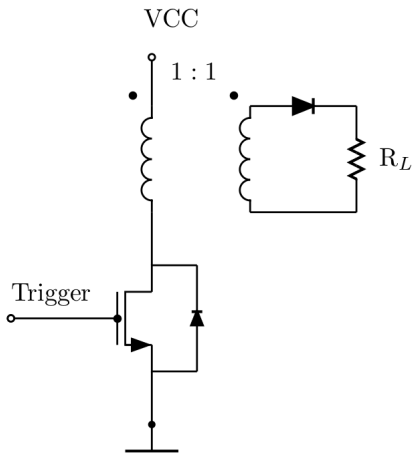

Figure 1: Basic Flyback circuit

Furthermore, the Power MOSFET should comply with power requirements as well as a slow rise and fall times to avoid reflections. This can be

easily achived for both rise and fall edges with an appropiate triggering sub-circuit and an addition of a parallel diode with a resistor, serially connected to the ground gate of the Power MOSFET.

2 Theoretical analysis

2.1 On phase

During the on phase, the Power MOSFET is conducting and the transformer experience a voltage near to V_P. The equivalent circuit is:

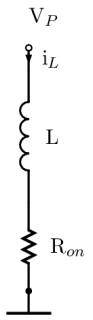

Figure 2: Equivalent ON state circuit

Kirchoff's equations

The electrical relationships in the circuit are:

$$V_P - V_{R_{on}} = L\frac{di_L(t)}{dt} \tag{1}$$

$$V_{R_{on}} = R_{on} i_L(t) \tag{2}$$

Differential equation

which form a non-homogeneous linear differential equation:

$$\frac{di_L(t)}{dx} L + i_L(t) R_{on} = V_P \tag{3}$$

Let's assume that at the beginning of the ON state, the inductor has no remaining current. The initial conditions are:

$$i_L(0^+) = 0$$

$$i_L(+\infty) = \frac{V_P}{R_{on}}$$

and the solution is:

$$i_L(t) = \frac{V_P}{R_{on}}(1 - e^{-\frac{t}{L/R_{on}}}) \tag{4}$$

It will always be, at the beginning of the ON state, a small remaining current in the inductance, I_{L_R}:

$$i_L(0^+) = I_{L_R}$$

A more accurate solution is:

$$i_L(t) = \frac{V_P}{R_{on}}(1 - e^{-\frac{t}{L/R_{on}}}) + I_{L_R}e^{-\frac{t}{L/R_{on}}} \tag{5}$$

I_{L_R} can be treated as zero if it is small. A dangerous situation is met when I_{L_R} reaches a level of saturation:

$$i_L(t_{SAT}) = I_{L_{SAT}}$$

Results

The time-to-saturation under no load or ***maximum pulse width under no load*** is:

$$t_{P_{max}oc} = t_{SAT} = \frac{L}{R_{on}} ln(\frac{\frac{V_P}{R_{on}} - I_{L_R}}{\frac{V_P}{R_{on}} - I_{SAT}})$$

however, if a load is connected in the second winding of the transformer, a $I_{R_{load}}$ is added to $i_L(t)$. Then, the time-to-saturation under load or ***maximum pulse width under load*** is:

$$t_{P_{max}loaded} = t_{SAT} = \frac{L}{R_{on}} ln(\frac{\frac{V_P}{R_{on}} - I_{L_R}}{\frac{V_P}{R_{on}} - (I_{SAT} - I_{load})})$$

The most restrictive maximum pulse width occurs when there is a load. Thus, the ***maximum pulse width*** corresponds to:

$$t_{P_{max}} = t_{P_{max}loaded} \tag{6}$$

2.2 Recovery phase

When the Power MOSFET is open, the equivalent circuit is:

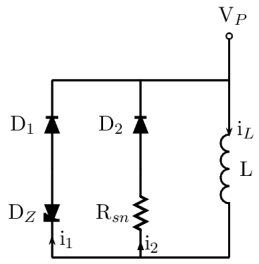

Figure 3: Equivalent circuit in Recovery Phase

which has two snubber nets. This snubber has two behaviours when draining the current off the inductance:

- Linear: the two snubber nets are active.
- Exponential: the resistive net is the only one active.

2.2.1 Linear Decrease

At the beginning of the recovery phase the current of the inductance is, from the on state:

$$i_L(0^-) = i_L(t_P) = I_{L_0}$$

where we have changed the temporal reference to the beginning of the recovery phase for easing notation.

Kirchoff's equations
As the two net are conducting:

$$i_L(t) = I_{L_0} - (\frac{V_{D_Z} + V_{D_1}}{L} + \frac{V_{D_Z}}{R_{sn}})t \tag{7}$$

this stage ends when zenner diode is not conducting, hence the boundary condition:

$$i_{L_{Lin,end}} = \frac{V_{D_Z}}{R_{sn}}$$

Results
The linear decrease ends at $t_{L_{end}}$ from the beginning of the recovery phase:

$$t_{L_{end}} = (I_{L_0} - \frac{V_{D_Z}}{R_{sn}})(\frac{V_{D_Z} + V_{D_1}}{L} + \frac{V_{D_Z}}{R_{sn}})^{-1} \tag{8}$$

2.2.2 Exponential Decrease

In this case the net formed by the zenner diode, D_Z and D_1, is open. Then, due to the input capacitance of the primary winding of the transformer, C_1, a parallel RLC circuit appears.

Kirchoff's equations
The highest value of R_{sn} to avoid overshoot is:

$$R_c = \frac{1}{2}\sqrt{\frac{L}{C_1}}$$

As it was done in [**?**] thanks to [3], given a targeted remaining current -I_{L_0}- in the inductance, a maximum value for the recovery time can be expressed.

Results
The ***maximum recovery time*** from the beginning of the recovery phase is:

$$t_{recovery} = f(I_{L_0}) < \frac{V_P}{V_{D_Z}} t_P + \frac{L}{R_{sn}}[ln(\frac{V_P}{R_{sn} I_R}) - 1] = t_{recovery,max} \tag{9}$$

2.2.3 Off state

The circuit is considered to enter in the off state when it is able to be triggered again without risk of damage. This happens when the recovery time ends, which means that the remaining current flowing through the magnetizing inductance is less than I_{L_0}.

2.3 Trigger circuit

A trigger circuit based on the shown below is used.

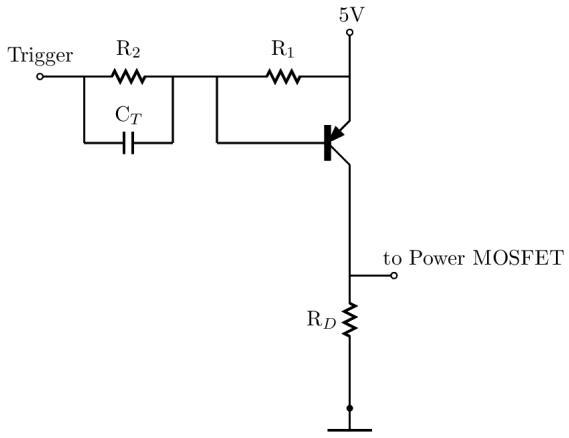

Figure 4: Fast trigger circuit

The voltage of the BJT base with regard to ground in a steady state is:

$$V_{base,GND_{steady}} = v_i \frac{R_1}{R_1 + R_2} + 5\frac{R_2}{R_1 + R_2} \tag{10}$$

2.3.1 Valid resistance values

This circuit is activated when the input signal goes to ground. It must be satisfied that when the input is high in a steady-state, the transistor is not conducting. When it is low in steady-state -ground-, the transistor is conducting. The following table shows the formal relations and the last column displays the valid resistance relation for $V_{base,GND} = 0.6V$

BJT condition	$V_{base,GND}$	v_i	**Circuit parameters**
NO CONDUCTION	$> 5 - V_{EB,cond}$	$v_{i,H} = 3.3V$	$R_2 > 1.83R_1$
NO CONDUCTION	$> 5 - V_{EB,cond}$	$v_{i,H} = 2.5V$	$R_2 > 3.16R_1$
CONDUCTION	$< 5 - V_{EB,cond}$	GND	$R_2 < 7.3R_1$

By fixing $V_{EB,cond}$ to 0.6V, we can use an input signal of different voltages if properly selected R_2 and R_1 :

$\mathbf{v}_{i,H}$	**Valid resistance ratios**
3.3V	$\mathrm{R}_2 \in (1.83\mathrm{R}_1,\ 7.3R_1)$
2.5V	$\mathrm{R}_2 \in (3.16\mathrm{R}_1,\ 7.3R_1)$

2.3.2 Transients

High to Low
The transient equation of the voltage in the base of the BJT referred to ground when there is a high to low change is:

$$V_{base,GND}(t) = v_{i,H}\frac{R_1}{R_1+R_2}e^{-\frac{t}{RC}} + 5\frac{R_2}{R_1+R_2} \tag{11}$$

where:

$$R = R_1//R_2$$

Low to High
The transient equation of the voltage in the base of the BJT referred to ground when there is a low to change is:

$$V_{base,GND}(t) = v_{i,H}(1 - \frac{R_1}{R_1+R_2}e^{-\frac{t}{RC}}) + 5\frac{R_2}{R_1+R_2} \tag{12}$$

where:

$$R = R_1//R_2$$

2.3.3 Modified trigger

Figure 4 showed a common trigger circuit for Power MOSFET. One of the most important capabilities of the Power MOSFET is its sharp rise and fall edges if properly trigger. In the case of this design, a sharp rise and fall edge is a drawback because of reflections. Hence, a solution for effectively slowing down the rise edge [4] -the fall slope is slow enough- is achieved by serially adding a resistance in parallel to a diode to the base of the Power MOSFET:

An analysis of the switching features are explained in the next section.

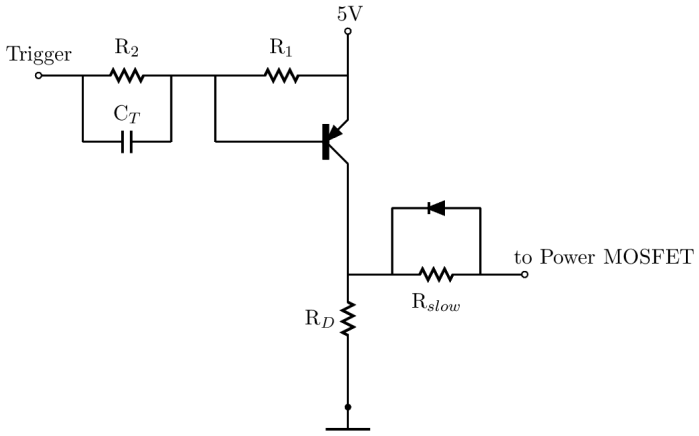

Figure 5: Slowed rising edge trigger circuit

2.4 Switching

The switching analysis of a Power MOSFET is divided in four stages. Due to the excesive complication of the switching behaviour, an in-depth demonstration of these stages should be directly consulted in [4]. The key parameter of the switching phase is the R_{slow} resistance value which modifies the slope of the rising edge. Experimental measures are taken to select the value that better suit to produce a Standard Blocking compliant [2] signal when a 50 Ω load is connected to the second winding of the transformer.

3 Circuit proposed

3.1 Schematics

A schematic of the circuit used for the testing board can be found attached at the end of this document.

4 Improvements over Level Converter board

4.1 Snubber Circuit

Previous The snubber circuit is a 1KΩ resistance in parallel to the second winding. This kind of snubber recovers slow and dissipates considerable power at the beginning, increasing the duration of the recovery phase and being candidate of damage, respectively. In case the resistor breaks, it would burnt the transformer is more pulses are received –because there is only a residual resistance for eliminating the remaining current.

Current The snubber circuit is formed by a zenner diode, a resistance activated by a diode and an optional parallel resistance to the second winding of the transformer. As it was explained beforehand, the first two nets help in draining the magnetizing current faster.

Improvement The magnetizing current is more rapidly drained off. The circuit is able to reduce the time between regenerated output pulses –the recovery phase is quicker. Apart from this, as more nets take part in draining the current in the inductance, the circuit is less liable to failure.

4.2 Adjustable Fall and Rise Time

Previous The trigger circuitry is directly connected to the ground gate of the Power MOSFET. By doing this, the fall and rise time are fixed.

Current The trigger circuitry is not directly connected to the ground gate of the Power MOSFET. In between the trigger and the ground gate a parallel connection formed by a diode and a resistor is added. The aim of this dipole is offering a resistance for the rising edge of the output pulse and a shortcircuit for the falling one. Thus, the rising time is configurable by changing one resistor.

Improvement Slowing down the rising edge reduces reflections.

4.3 Less Tilt in the Output Pulse

Previous The maximum R_{ON} value of the BUZ32 Power MOSFET is 400 $m\Omega$.

Current The R_{ON} value of the IRLML0060TRPBF Power MOSFET is 92 $m\Omega$. A lower value reduces the voltage losses in the Power MOSFET that translates to a reduction of the tilt.

Improvement Tilt is hardly noticeable when compared to previous version.

5 Simulation and Measurements

Simulations have been done to verify the following parameters:

- Top voltage of the output pulse.
- Rise time of the output pulse.
- Fall time of the output pulse.
- Smoke parameters of the circuit.

5.1 Simulations

Plots are separately attached to this document.

5.2 Measurements

Measurements of the flyback converter were taken with a LeCroy Waverunner LT364L oscilloscope. A Farnell instruments PDD3010A dual power supply was used to provide 30V and 5V. The input signal for the trigger subcircuit was taken from CTVR VME board and connected directly to the flyback converter through a 10ns cable.

Input signal	**Low time**	**Period**
inverted-TTL	10 μs	1 ms

The output pulse was measured:

$\mathbf{R}_L$	50 Ω
Initial top voltage value	24V
Tilt	$\leq$ 0.5V
Floor voltage value	0V
Pulse width	10 μs
Rise Time	1.2 μs
Fall Time	2.49 μs

References

[1] C. Dehavay. Distributeur de Timing en Chasis Europe Notice Descriptive. CERN, PS-CO-WP, Note 87-028, February 1987.

[2] C. Gil Soriano. Standard Blocking Output Signal Definition for CTDAH board, September 2011. `http://www.ohwr.org/documents/109`.

[3] P. Norman and E.J.E. Smith. The design of transistor blocking oscillators. *Proceedings of the IEE - Part B: Electronic and Communication Engineering*, 106(18):1251 –1259, may 1959.

[4] D.A. Grant and J. Gowar. *Power MOSFETS: theory and applications*. A Wiley-interscience publication. Wiley, 1989.