CTDAH Schematics Report

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Abstract

This document aims to lighten the schematics revision by providing design decisions that were taken.

Contents

1 Page 1: CTDAHalt_TOP.SchDoc

The top page shows the general schema the design was divided. The two main interconnecting blocks are the FPGA sheet and the clock sheet. The complexity of the clock sheet increased due to the inclusion of the clocking sources required to implement White Rabbit in CTDAH. Thus, SFP need is self-explained. The right side of the sheet shows the VME64x connector sheet and the power supplies. It should be noted that the power supplies are interconnected by the port EN_N_BLOPS. This interconnection was added to sequencing the power supplies boot-up as one of the measures to be glitch-free.

2 Page 2: PowerSuppliesFPGA.SchDoc

This sheet covers the 3V3 and 1V2 voltages generation for the FPGA. Each voltages were taken from the 5V an 3V3 sources, respectively. The conversion is implemented by linear regulators so as to have less noise. Selecting the FPGA decoupling capacitors was done following the Xilin's application note recommendations in UG393. The body size of the capacitors should be as small as possible for having the lowest ESL –after layouting external ESL will be added, so better to have reduced one with small body sizes.

2.1 Antiglitch measures

Special attention has been taken to avoid the generation of glitches at reset and start-up. Two approaches are implemented:

- Added control logic for open-drain nets that affect the triggering of the output signals –both in front and rear panels. This approach is explained in sheet 8.
- Power sequencing the power regulators. As can be seen in sheet two, TPS3808G01, is added to produce a low signal if the monitored voltage of 3V3 for the FPGA banks is lower than 0.405V. The low value is issued during the time the voltage is lower plus a selectable delay.

3 Page 3: PowerSupplyBlocking.SchDoc

The power supply for the Standard Blocking signal should be analysed carefully. First, it is good to take a look to the sheet 9 -BlockingUnit- main decoupling capacitor of the 24V supply.

3.1 Maximum current requested for the signal

When a pulse is generated, the coupling capacitors are the ones that provide, locally and fast, the current needed for building up the pulse. As it will be pointed out later, these capacitors should be working in the range of 1 to 15 Mhz to reduce delta-I noise in the Power Distribution Network, PDN. However, the PDN should be able to provide the current the capacitors are losing.

$$\begin{aligned} I_C &= C\frac{dV_C}{dt} \\ \frac{dV_C}{dt} &= V_{cc}e^{-\frac{t}{R_{load}C}} \\ I_{PDN}(t) &= \frac{V_{cc}}{R_{load}}(1-e^{-\frac{t}{R_{load}C}}) + \frac{V_{cc}}{L_{pri}}t \end{aligned} \tag{1}$$

It should be noted that in the capacitor discharge function the effect of the primary inductance has not been considered for having a more intuitive approach to the problem. Considering that the biggest effect corresponds to the 10μF capacitor, the set of circuit parameters are:

$$\begin{aligned} C &= 10\mu F \\ R_{load} &= 50\Omega \\ L_{pri} &= 100\mu H \end{aligned} \tag{2}$$

At the end of the pulse, the PDN is working harder:

$$t = t_{P_{max}} = 2\mu s$$
$$I_{PDN}(t_P) \approx 800mA \quad (3)$$

This is the case for one output loaded. The worst case scenario for the whole board is when the 18 outputs are loaded and daisy-chained, in which the consumption at the end of the pulse rises to 14 A. Because of this, three 24V power supplies are specified in the design. More capacitors can be added in parallel to every Standard Blocking Unit, but derating in them could end up requiring the three power supplies.

WARNING: as it can be read in Rule 5.9 of ANSI/VITA 1-1994, the power pins of the VME64 connector must be capable of carrying currents according to Figure 5-7 of the same document. Values of CTDAH are well above this bottom limit.

4 Page 4: ClocksMonitor.SchDoc

Three clocks are included: a system clock of 20MHz, a 125 MHz for Gigabit Transceivers and a I^2C programmable clock. The clock generation for WR follows the successful design of SPEC board. Additionally, a DS18B20U+ is included to provide an unique ID, as done in SPEC as well. One ADC for monitoring Blocking voltages, and two microswitches -one for input selection and a general purpose one- complete this sheet.

5 Page 5: FPGA.SchDoc

This sheet covers FPGA interconnection -four blocks and MGT-, PCA9600 -an I^2C line driver-, two general purpose buttons, JTAG and a Numonix PROM memory that can be written. Special care has been taken in the pinout assignment.

6 Page 6: VME64xConn.SchDoc

The P1 connector provides all the sources of voltages and the VME64 Utility Bus. P2 has been rearranged to reduce crosstalk, specially for the output pulses. Input pulses are in the inner part of the connector due to their lower spectral power components. EMI concerns in the P2 connector.

7 Page 7: InputBlocking.SchDoc

It consist of a 51 Ω Bourns termination resistor -2W capable in DC-, a TVS for ESD protection in the range of 24V, a DC-rejection filter, a 3V3 TVS for ESD protection and an optocoupler.

8 Page 8: BlockingOutput.SchDoc

The connection of the 18 Standard Blocking outputs is shown. Every channel -that is three outputs- is driven by a BCT25244.

8.1 Antiglitch measures

A glitch can appear in startup if the OE_N pin has a high value and there is no pull-up resistor at the output of BCT25244.By pulling up in both sides -as it was done in previous designs- the glitches are avoided.

9 Page 9: BlockingUnit

As the Flyback topology is already explained in a previous document, the tips will be mainly focused on deglitching and power requirements.

9.1 Antiglitch measures

A strong pull-up is included at the input of the Power MOSFET driver to avoid glitches. Apart from this a 330 Ω resistor is added to provide a 51 Ω termination, just in case it would be desired.

9.2 Decoupling capacitors

The key parts are the decoupling capacitors in top of the primary winding of the transformer and the shape of the signal that will need the 24V supply. Current flowing through the driver is an order of magnitude lower than the output stage and thus not prioritary. First of all, the bandwith of the generated pulse is determined by the 10 to 90rise time –which can be configured:

$$BW = \frac{0.35}{t_R} \tag{4}$$

assuming that the rise time is 25 ns, the higher frequency should be around 15 MHz. Capacitors effective in that range should be chosen. By using Altera PDN tool, it can be seen that the two capacitors chosen provide a low impedance that guaranties a 3% or lower ripple noise in the 24V net: However, a more sensible design decision is slowing down the pulses -as Standard Blocking defines- because two reasons:

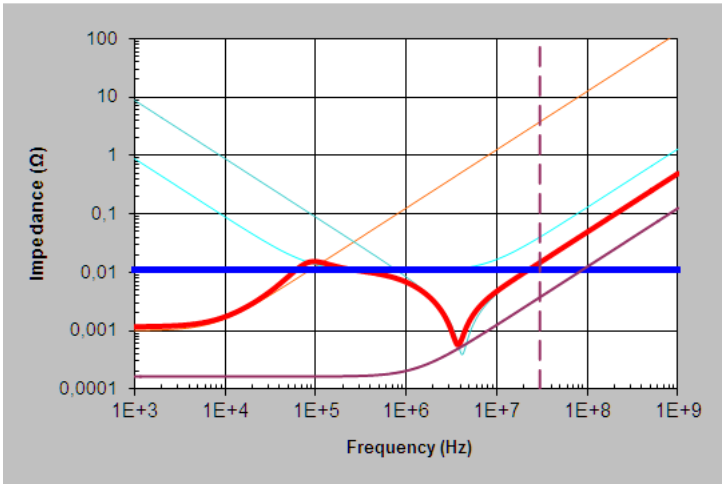

Figure 1: PDN + Decap impedance approximation

- Reducing crosstalk
- Reducing unnecessary spectral power in 15 MHz. There is no real need of that speed and due to the RC attenuation in the transmission line, this higher frequency will be much attenuated and not received.

10 Page 10: FrontTTL.SchDoc

Covers the TTL output generation and input conditioning. TVS protection is added and the pulse is regenerated by hysteresis.

10.1 Antiglitch measures

Same measures as Blocking ones.

11 Page 11: FrontPanelLeds.SchDoc

Steady LEDs are driven by a logic triggerable MOSFET and swithing, low current are directly driven by FPGA.

12 Page 12: Communications.SchDoc

A USB to UART. Should be discussed if this functionality it is worthy.

13 Page 13: SFPConnector.SchDoc

Basically same as SPEC.