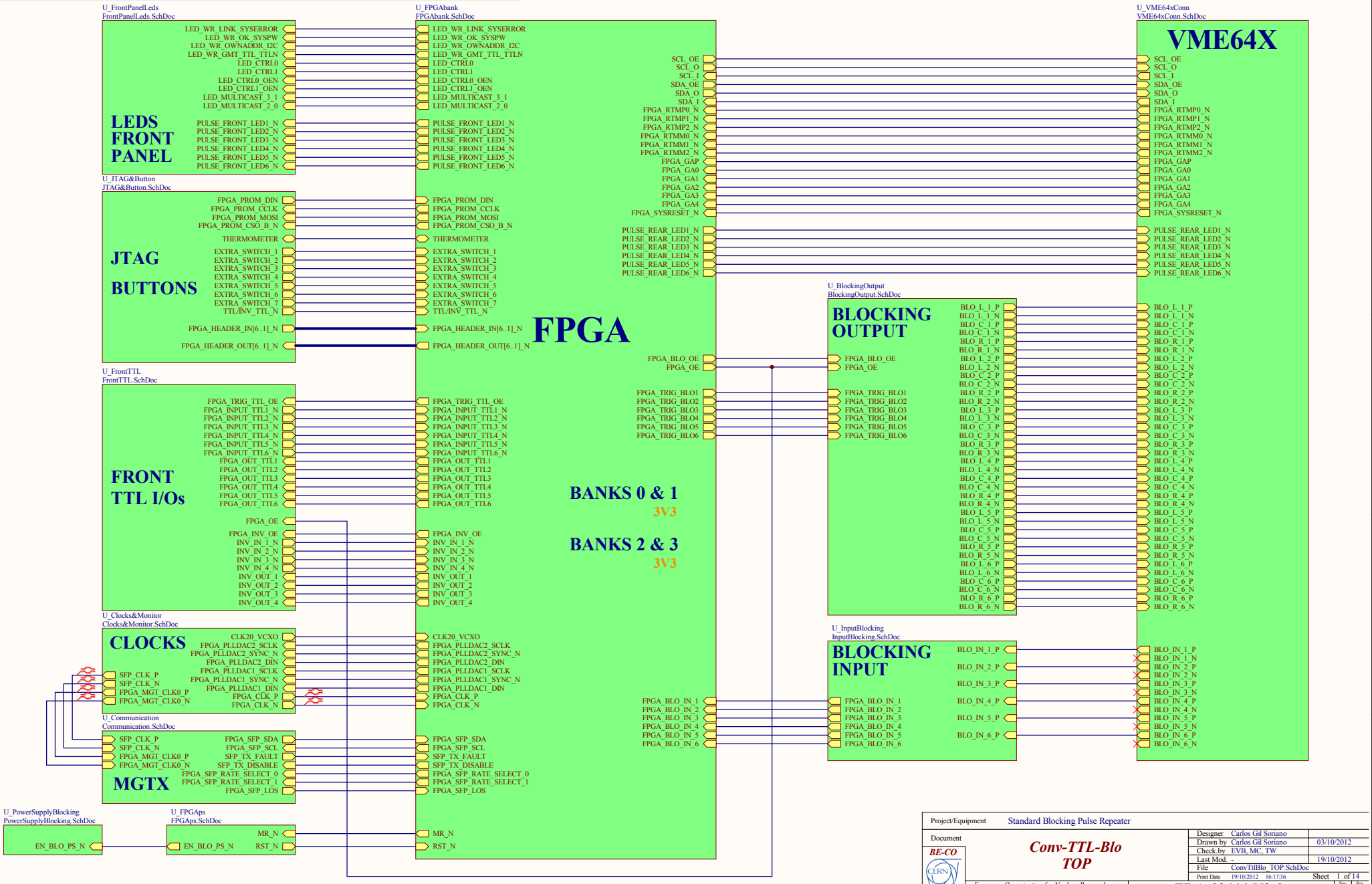


Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo TOP
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check by	EVB, MC, TW
Last Mod.	- 19/10/2012
File	ConvTtlBlo_TOP.SchDoc
Print Date	19/10/2012 16:17:36 Sheet 1 of 14
BE-CO	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland
EDA-02446-V2-0	Size A3 Rev 1

Efficiency of 85% and better

IC29 TPS54312PWP

Capacitor CT not mounted: delay of 570ms

IC30 TPS3808G01DBVT

IC11E IC11F SN74LVC14AD

Not Mounted

IC14G IC14H XC6SLX45T-3FGG484C

Voltages are:

*** FPGA	
VCCO_0	3V3
VCCO_1	3V3
VCCO_2	3V3
VCCO_3	3V3
VCCaux	3V3
VCCint	1V2
*** PROM	
VCCaux	3V3

Test points

PI filters for decoupling noise in the band of 50 MHz to 150 MHz in 3V3 and 5V rails.

BLM41PG181SN1L is a ferrite with low DCR (max 10mOhm) targeted for high current (power rails).

VCCO_int decoupling capacitors

VCCO_0 decoupling capacitors

VCCO_1 decoupling capacitors

VCCO_2 decoupling capacitors

VCCO_3 decoupling capacitors

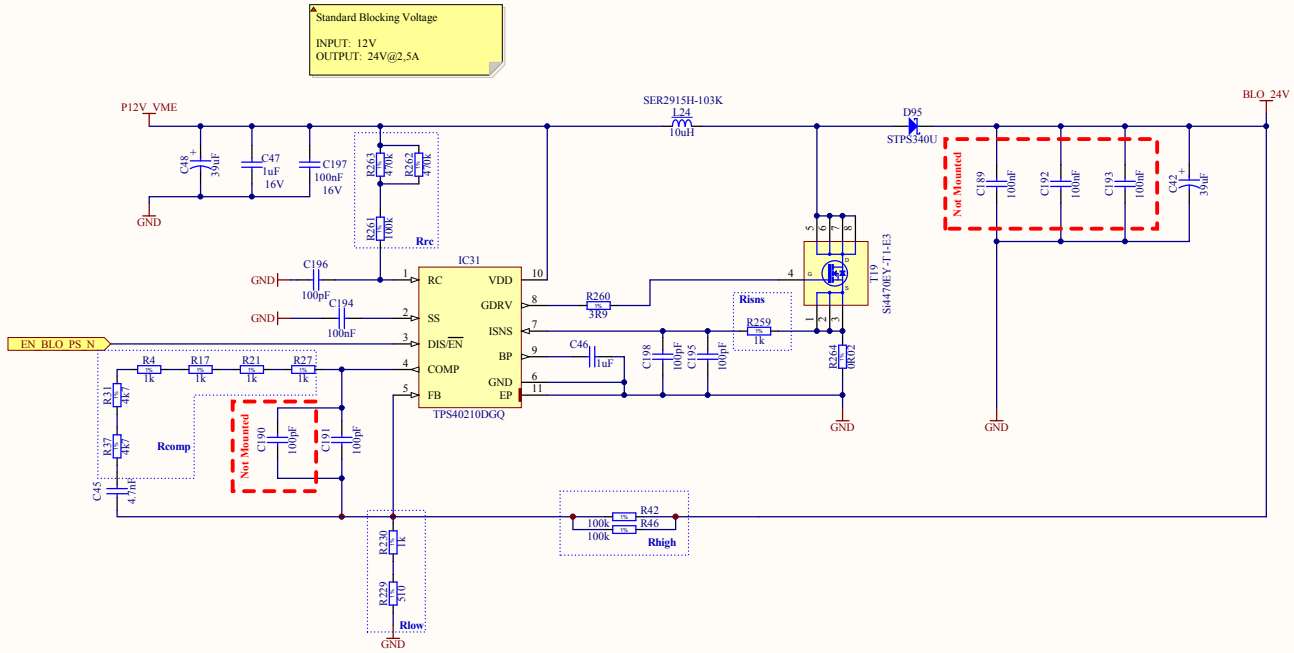
VCCAUX decoupling capacitors

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo FPGA PS
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check by	EVB, MC, TW
Last Mod.	- 18/10/2012
File	FPGAps.SchDoc
Print Date	19/10/2012 16:17:37
Sheet	2 of 14
Size	A3
Rev	1

BE-CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02446-V2-0



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo BLOCKING PS	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File PowerSupplyBlocking.SchDoc	
		Print Date 19/10/2012 16:17:37	Sheet 3 of 14
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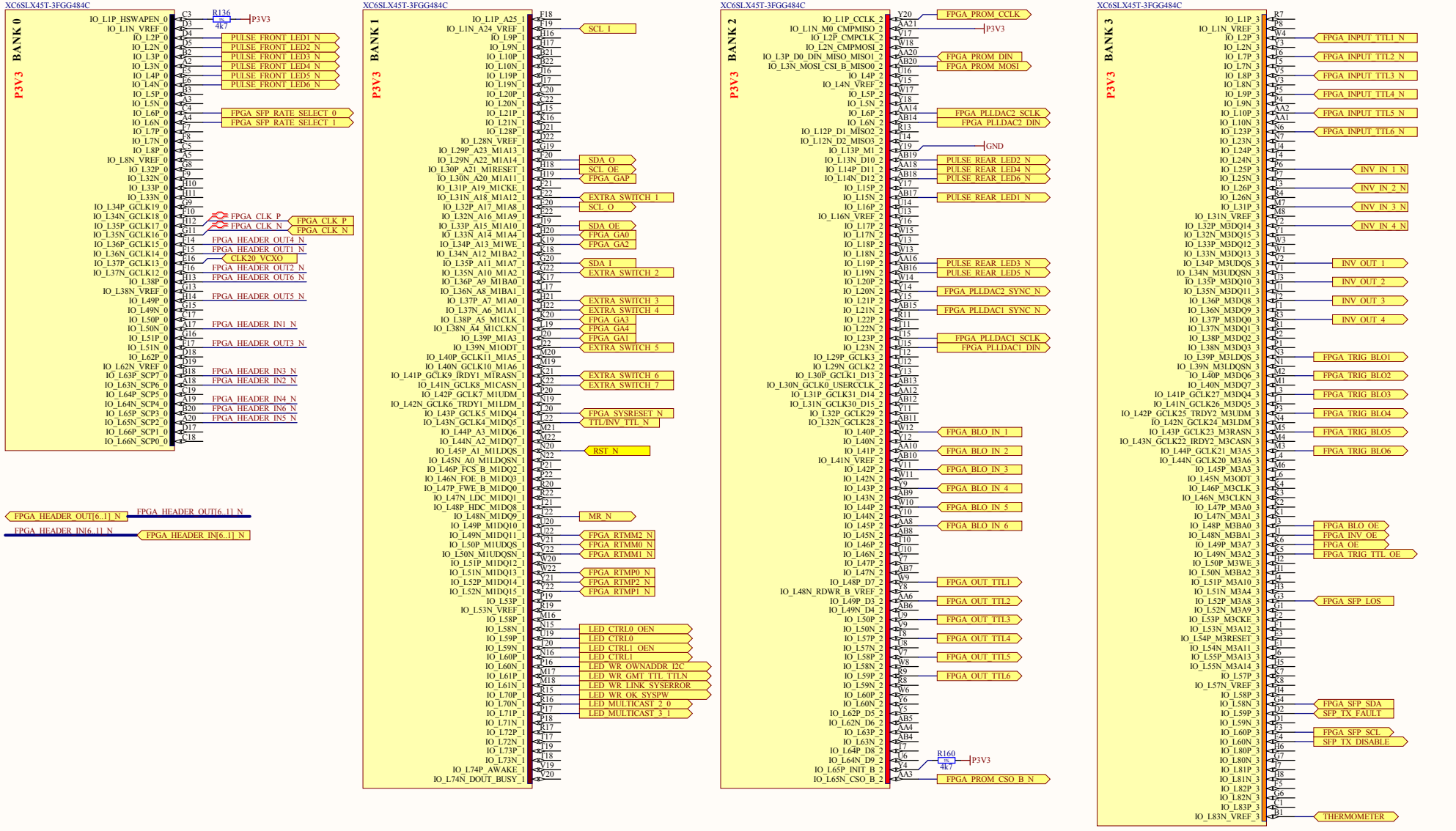
To allow high SerDes ratios, leave all the trigger inputs and outputs in _P pins.

See Xilinx's document UG381, chapter 3 for further information.

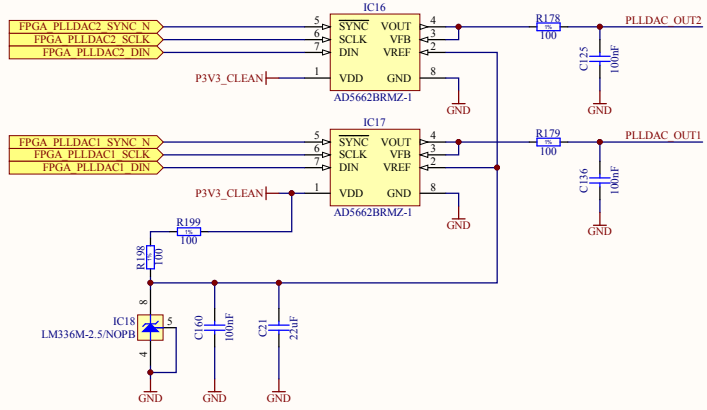


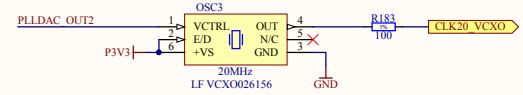
Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo FPGA BANK
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check by	EVB, MC, TW
Last Mod.	- 19/10/2012
File	FPGAbank.SchDoc
Print Date	19/10/2012 16:17:38
Sheet	4 of 14
Size	A3
Rev	1

BE-CO

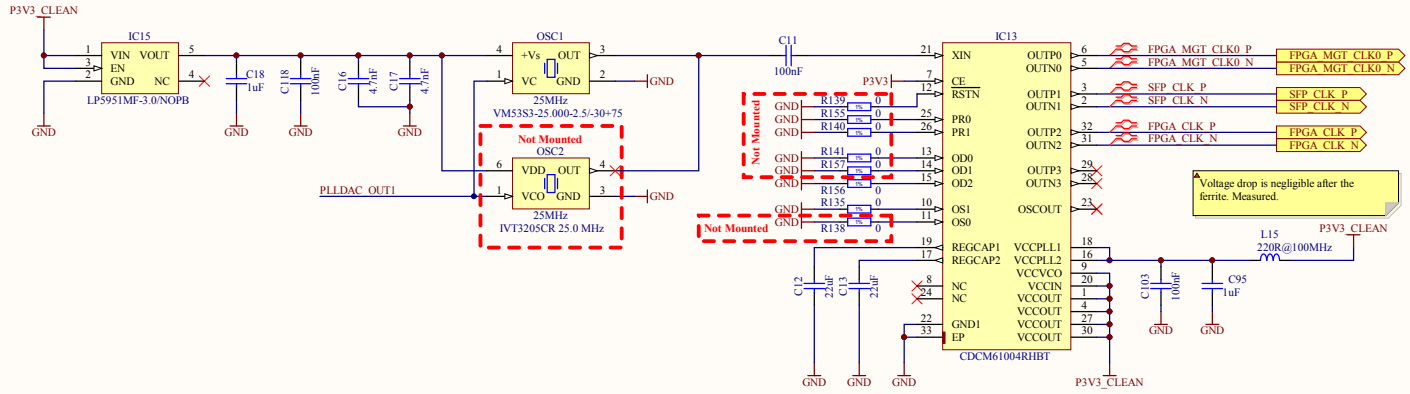
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02446-V2-0





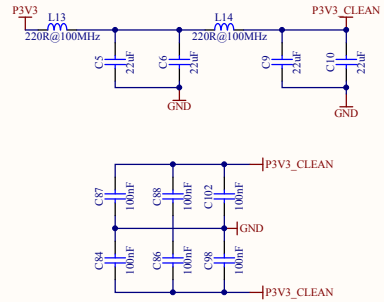
Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).



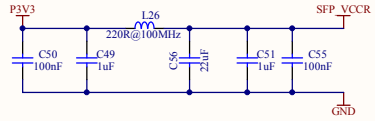
Voltage drop is negligible after the ferrite. Measured.

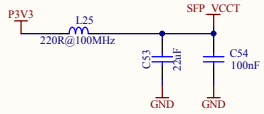
CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.

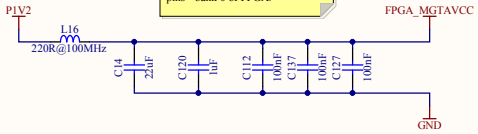
Input = 25 MHz
Output=125 MHz

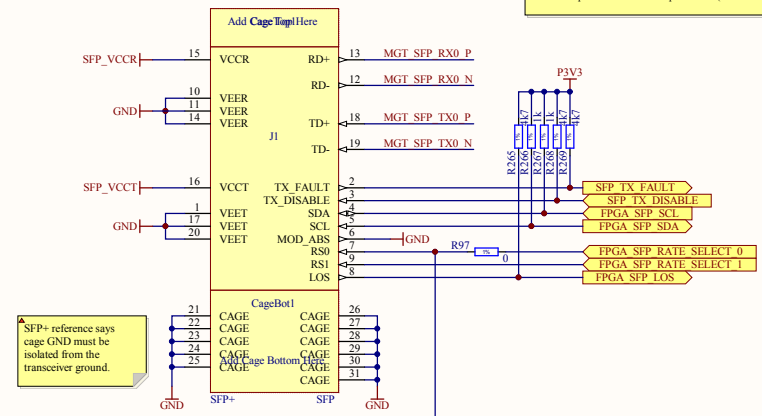


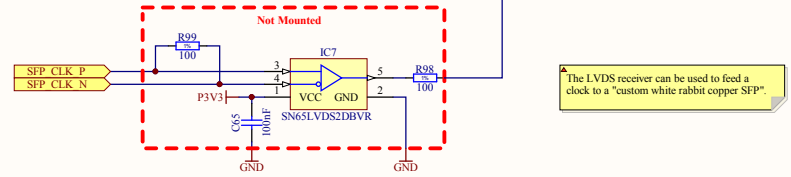
Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo CLOCKS	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File Clocks&Monitor.SchDoc	
		Print Date 19/10/2012 16:17:38	Sheet 5 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

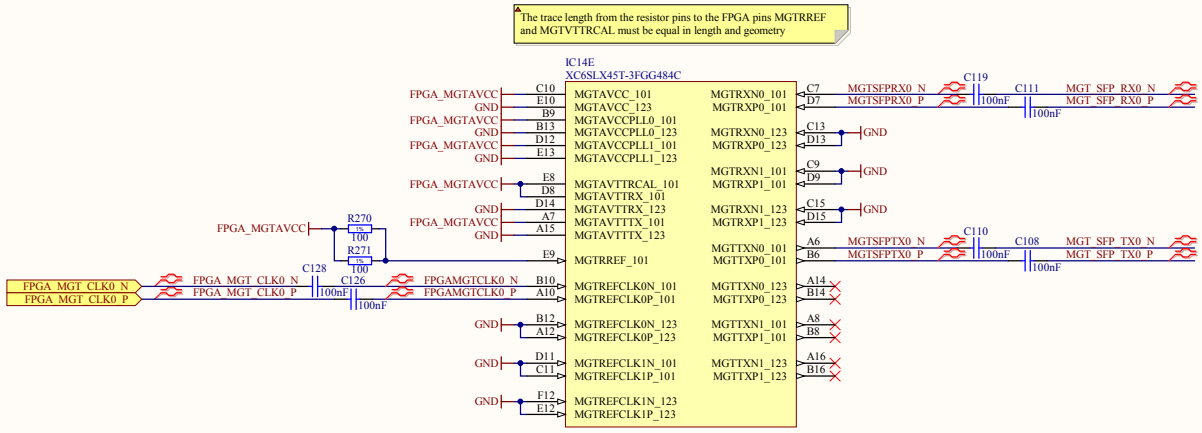






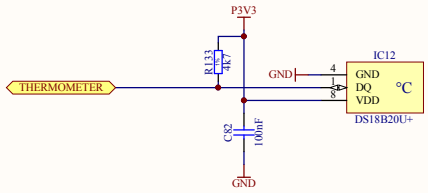




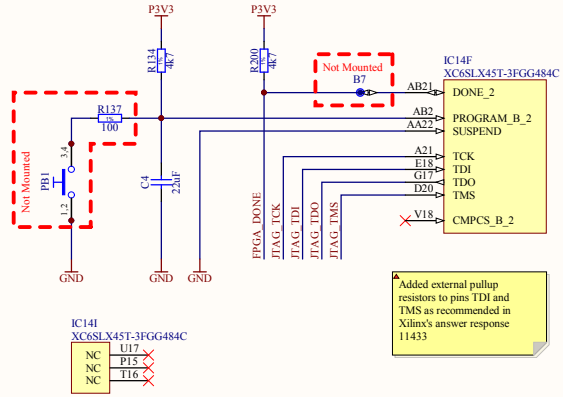


Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo MGTX	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File Communication.SchDoc	
		Print Date 19/10/2012 16:17:39	Sheet 6 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

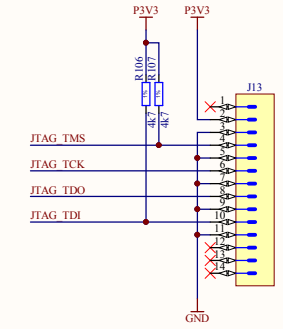
Thermometer will be used to have a FPGA unique ID

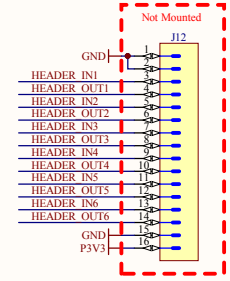


PROGRAM_B must be asserted low for more than 500ns



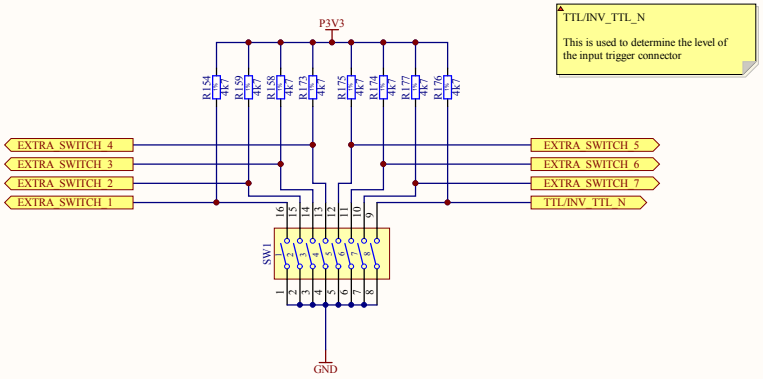
Added external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433

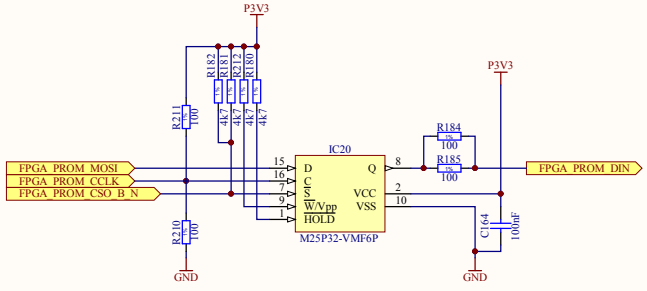


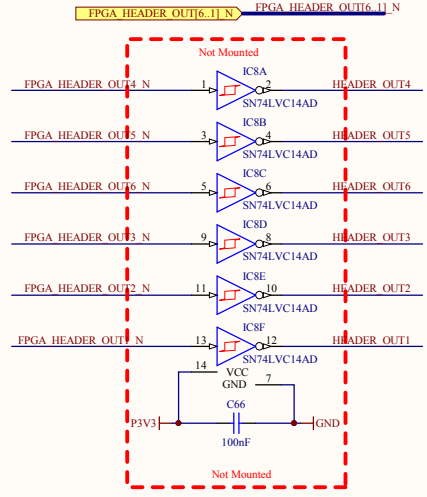


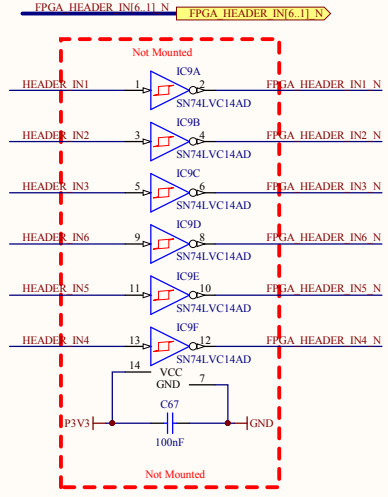
TTL/INV_TTL_N

This is used to determine the level of the input trigger connector





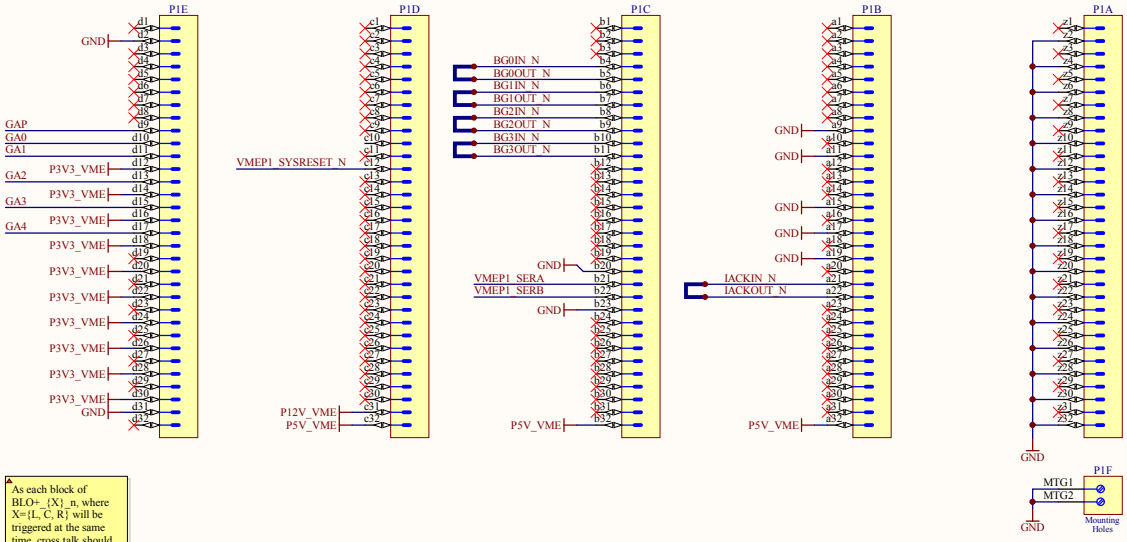




Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo JTAG	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File JTAG&Button.SchDoc	
		Print Date 19/10/2012 16:17:39	Sheet 7 of 14
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3 / Rev 1

Utility Bus Signal: see page 199
ANSI/VITA 1-1994

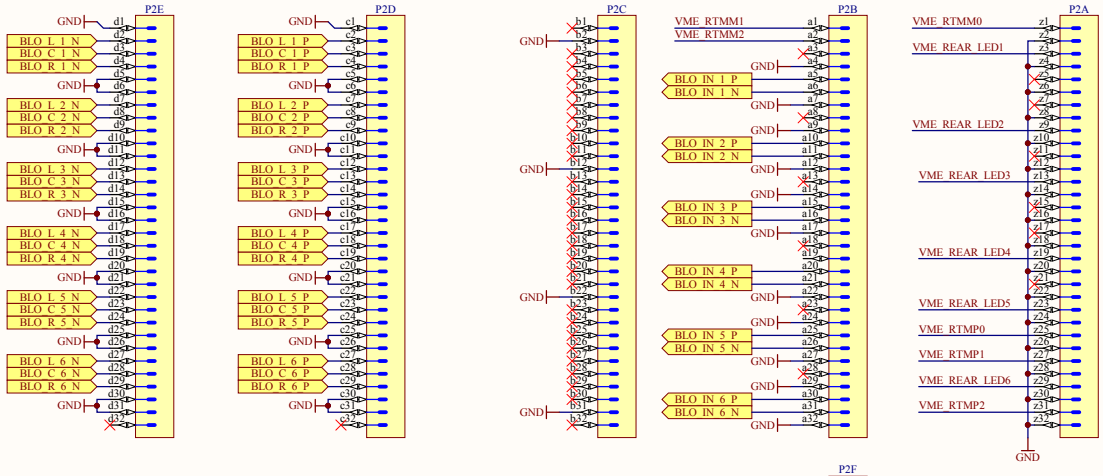
Output configurations in page 230
SYSRESET_N Open collector

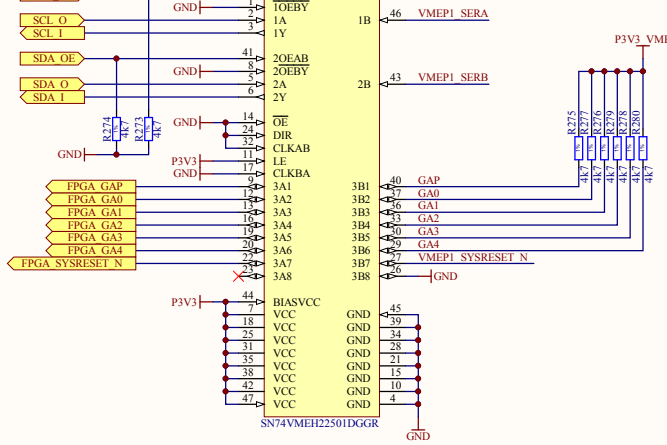


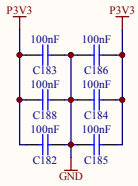
As each block of BLO+_{X}_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical.
However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

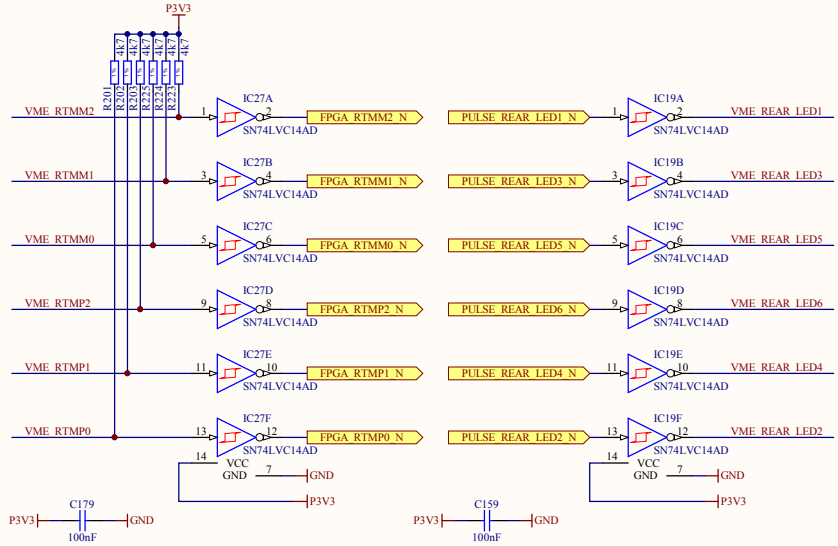
As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo
Signals with more spectral power in higher frequencies should be routed more carefully,so it is better to leave the easiest paths to them.
In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used.
Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

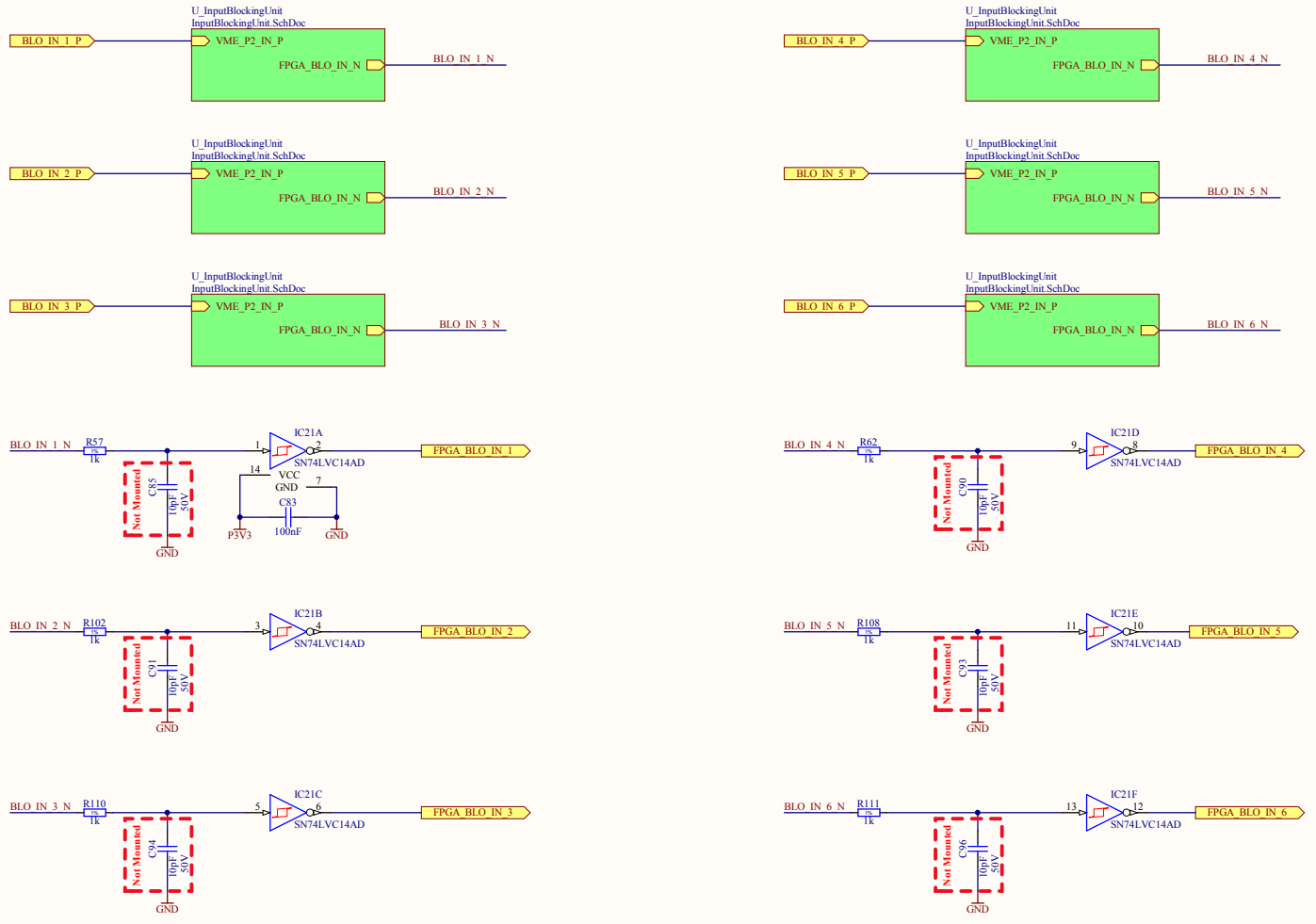






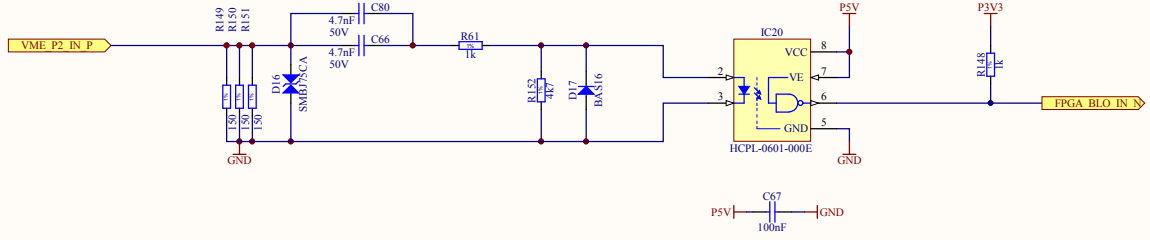


Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo VME64X**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File VME64xConn.SchDoc	
		Print Date 19/10/2012 16:17:40	Sheet 8 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

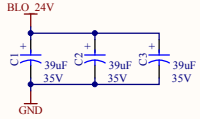


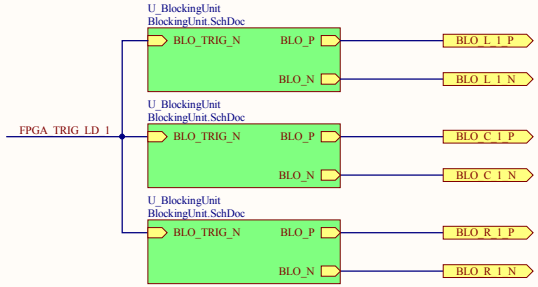
Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT BLO**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	19/10/2012
		File InputBlocking.SchDoc	
		Print Date 19/10/2012 16:17:40	Sheet 9 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

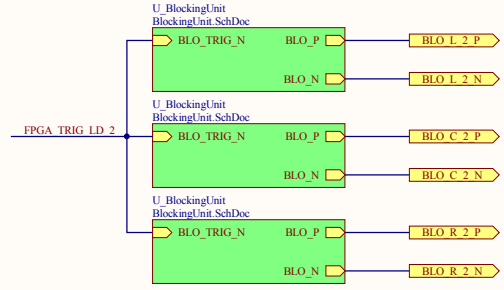
Input waveforms:
nominal 24V Std.Blocking
minimum 5V Std.Blocking

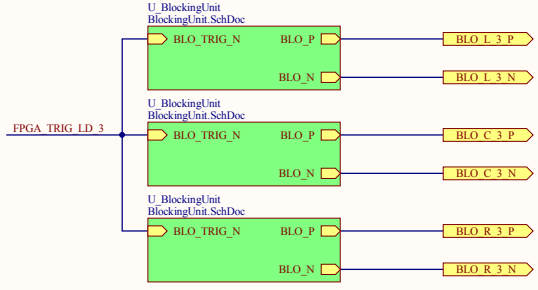


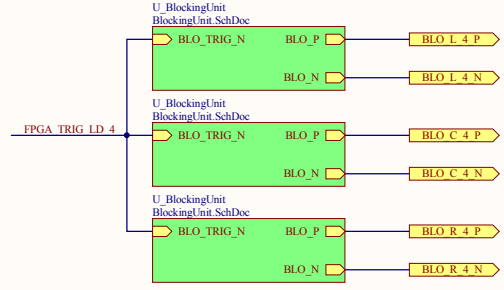
Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	19/10/2012
		File InputBlockingUnit.SchDoc	
		Print Date 19/10/2012 16:17:41	Sheet 10 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

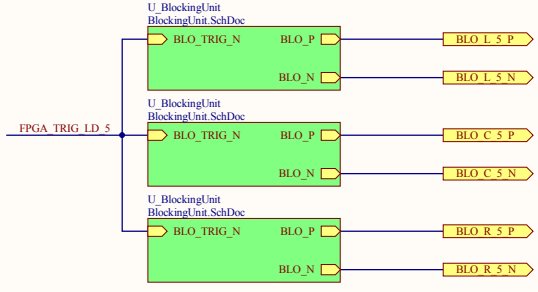


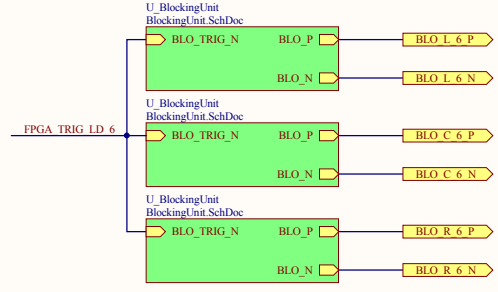


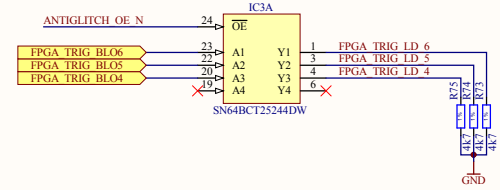


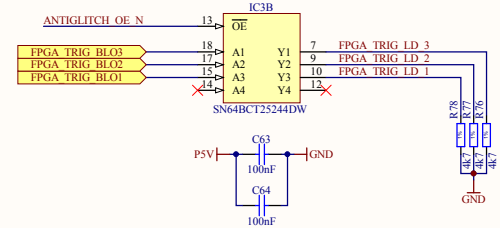


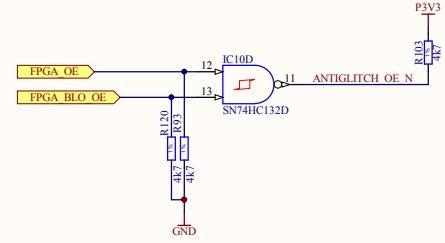


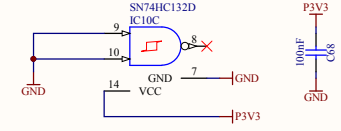




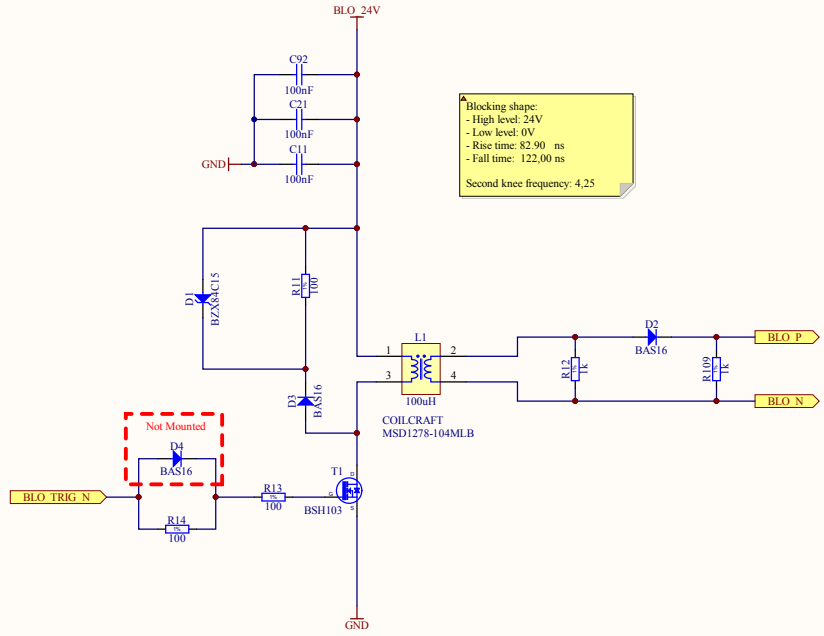








Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT BLO**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File BlockingOutput.SchDoc	
		Print Date 19/10/2012 16:17:41	Sheet 11 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

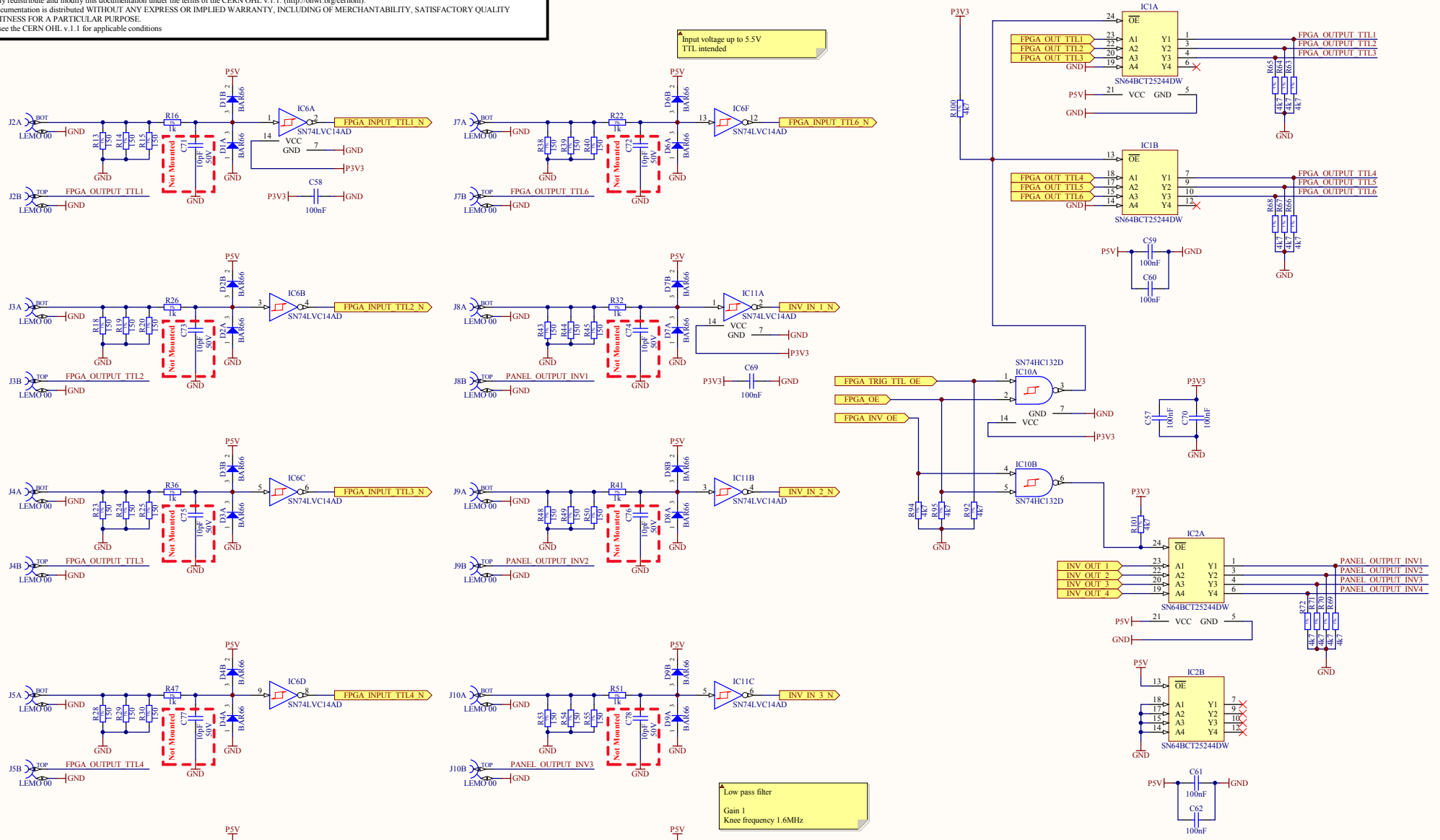


Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File BlockingUnit.SchDoc	
		Print Date 19/10/2012 16:17:42	Sheet 12 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

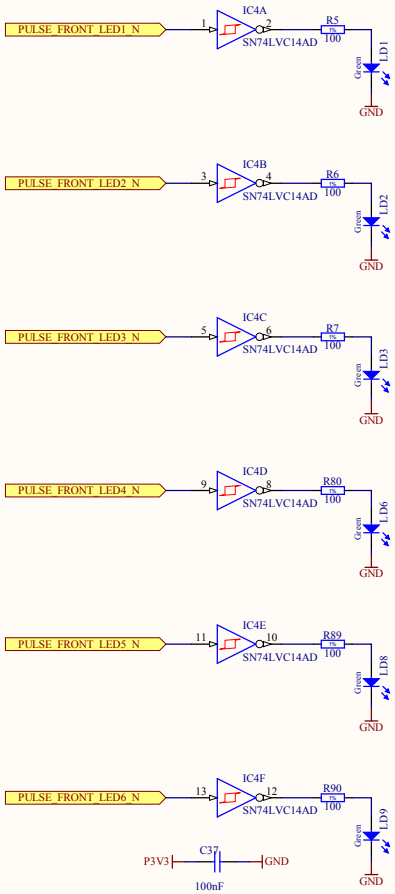
Input voltage up to 5.5V
TTL intended

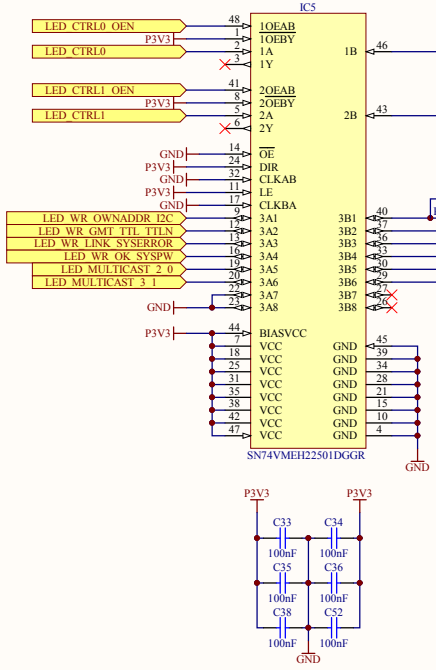
Low pass filter

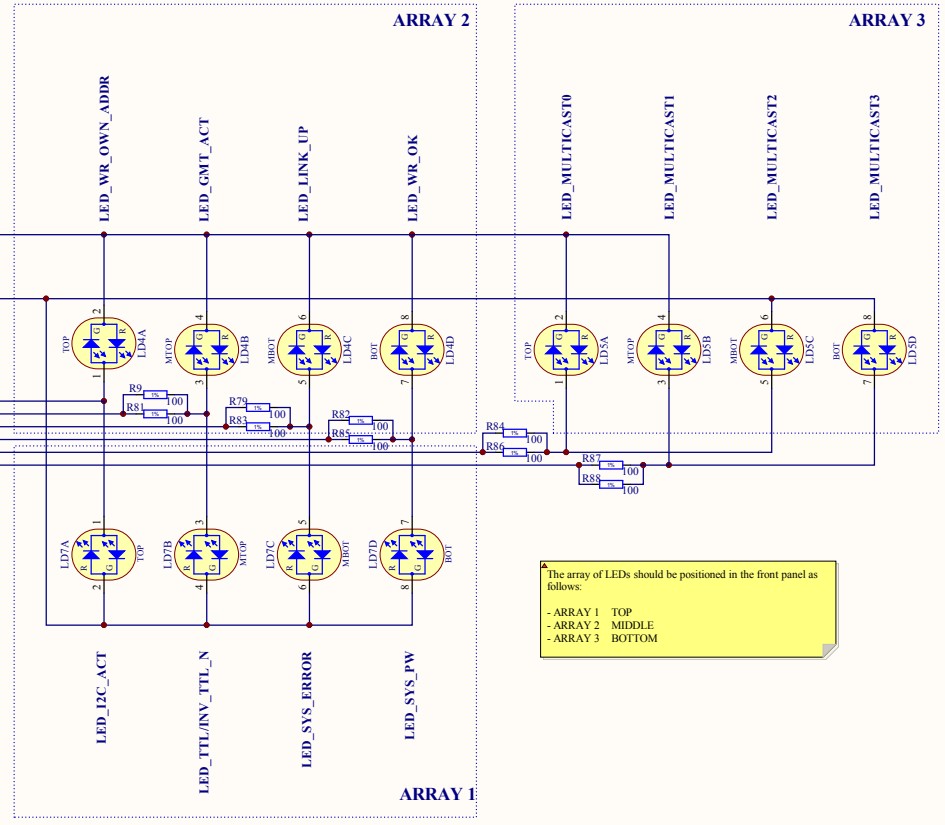
Gain 1
Knee frequency 1.6MHz



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo FRONT TTL	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	19/10/2012
		File FrontTTL.SchDoc	
		Print Date 19/10/2012 16:17:42	Sheet 13 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1







The array of LEDs should be positioned in the front panel as follows:

- ARRAY 1 TOP
- ARRAY 2 MIDDLE
- ARRAY 3 BOTTOM

ESD discharge strips (top and bottom of the card)

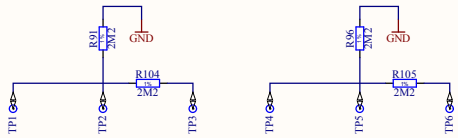


FIG1 FIG2
FIG3 FIG4
FIG5 FIG6

Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo FRONT PANEL	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by EVB, MC, TW	
		Last Mod. -	18/10/2012
		File FrontPanelLeds.SchDoc	
		Print Date 19/10/2012 16:17:43	Sheet 14 of 14
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