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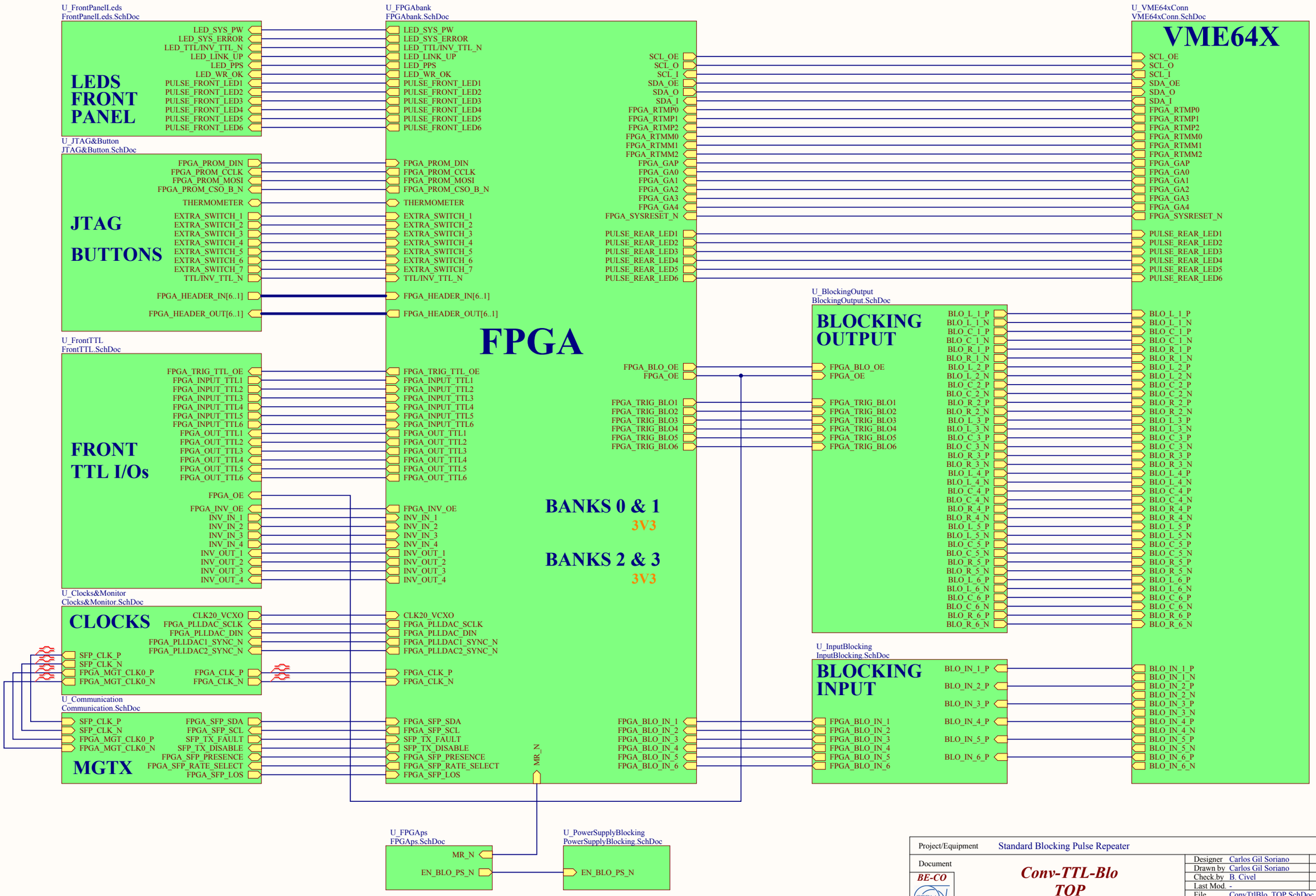

Project/Equipment	Standard Blocking Pulse Repeater		
Document	*Conv-TTL-Blo TOP*	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File ConvTtlBlo_TOP.SchDoc	
		Print Date 22/02/2012 13:27:01	Sheet 1 of 36
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V1-0	Size A3	Rev -

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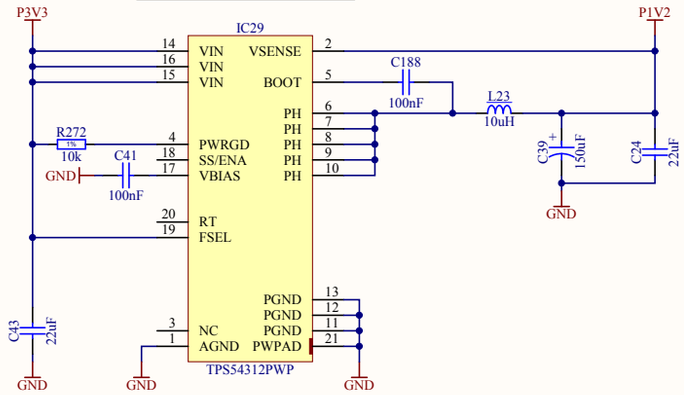
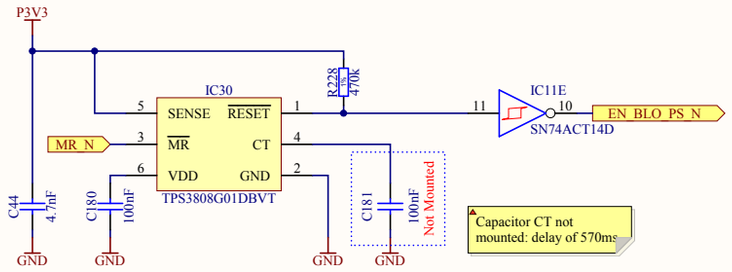
Efficiency of 85% and better





Voltages are:

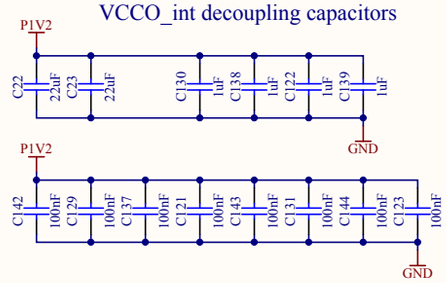
*** FPGA

VCCO_0	3V3
VCCO_1	3V3
VCCO_2	3V3
VCCO_3	3V3
VCCaux	3V3
VCCint	1V2

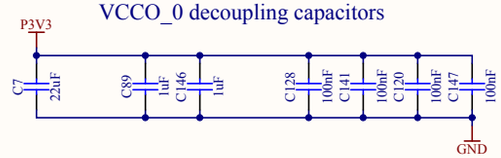
*** PROM

VCCaux	3V3

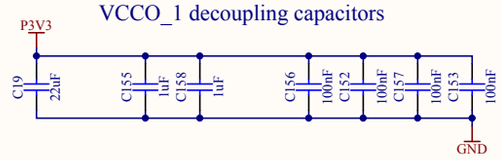
VCCO_int decoupling capacitors



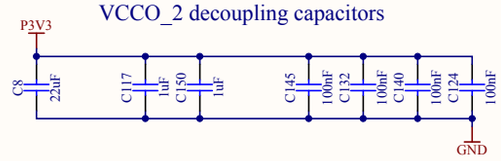
VCCO_0 decoupling capacitors



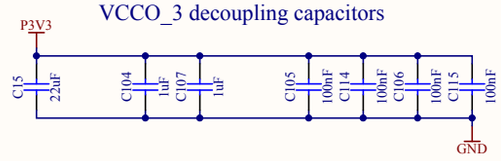
VCCO_1 decoupling capacitors



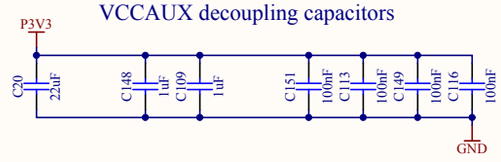
VCCO_2 decoupling capacitors

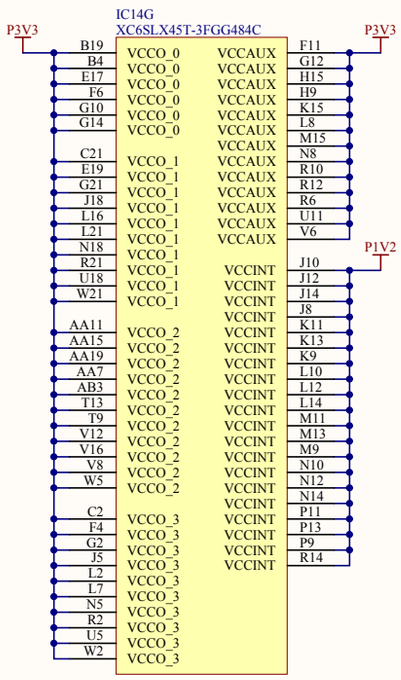


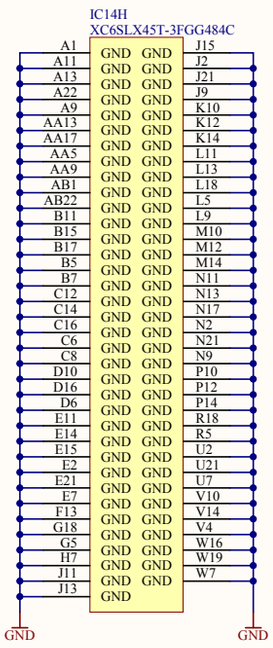
VCCO_3 decoupling capacitors



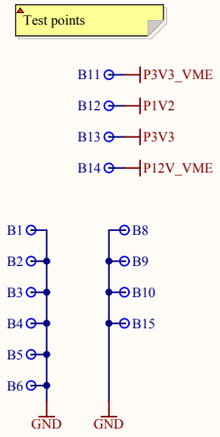
VCCAUX decoupling capacitors

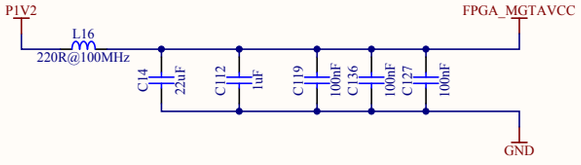




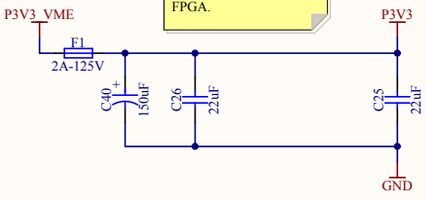


Test points





Closer as possible to GTP DUAL pins --bank 0 of FPGA.



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo FPGA PS**	Designer	Carlos Gil Soriano
		Drawn by	Carlos Gil Soriano 10/10/2011
		Check.by	B. Civel 08/12/2011
		Last Mod.	- 22/02/2012
		File	FPGAps.SchDoc
		Print Date	22/02/2012 13:27:01 Sheet 2 of 36
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V1-0	Size A3 Rev -

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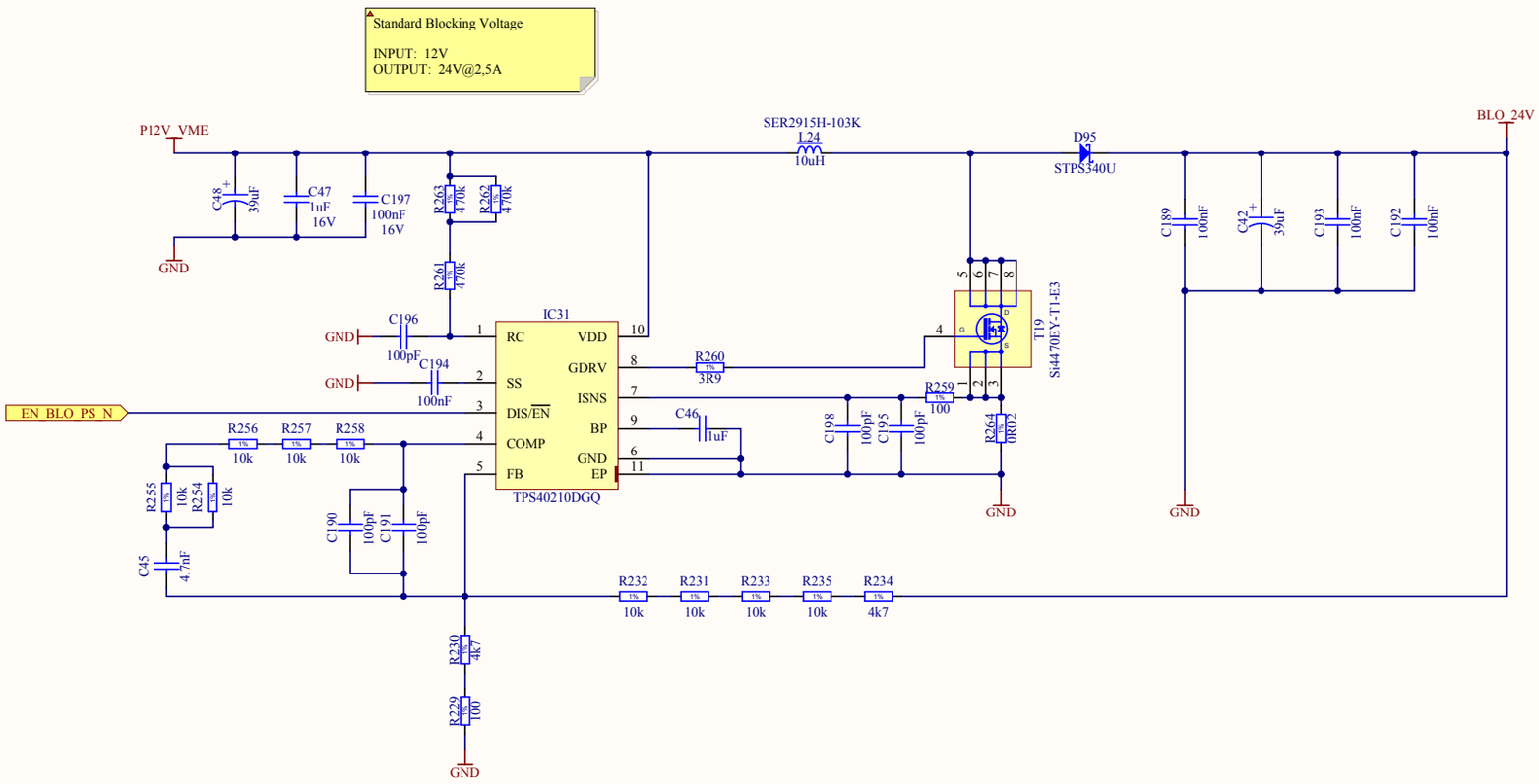
Standard Blocking Voltage

INPUT: 12V
OUTPUT: 24V@2,5A



Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo BLOCKING PS
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check.by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	PowerSupplyBlocking.SchDoc
Print Date	22/02/2012 13:27:01 Sheet 3 of 36
	European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland
	EDA-02446-V1-0 Size A3 Rev -

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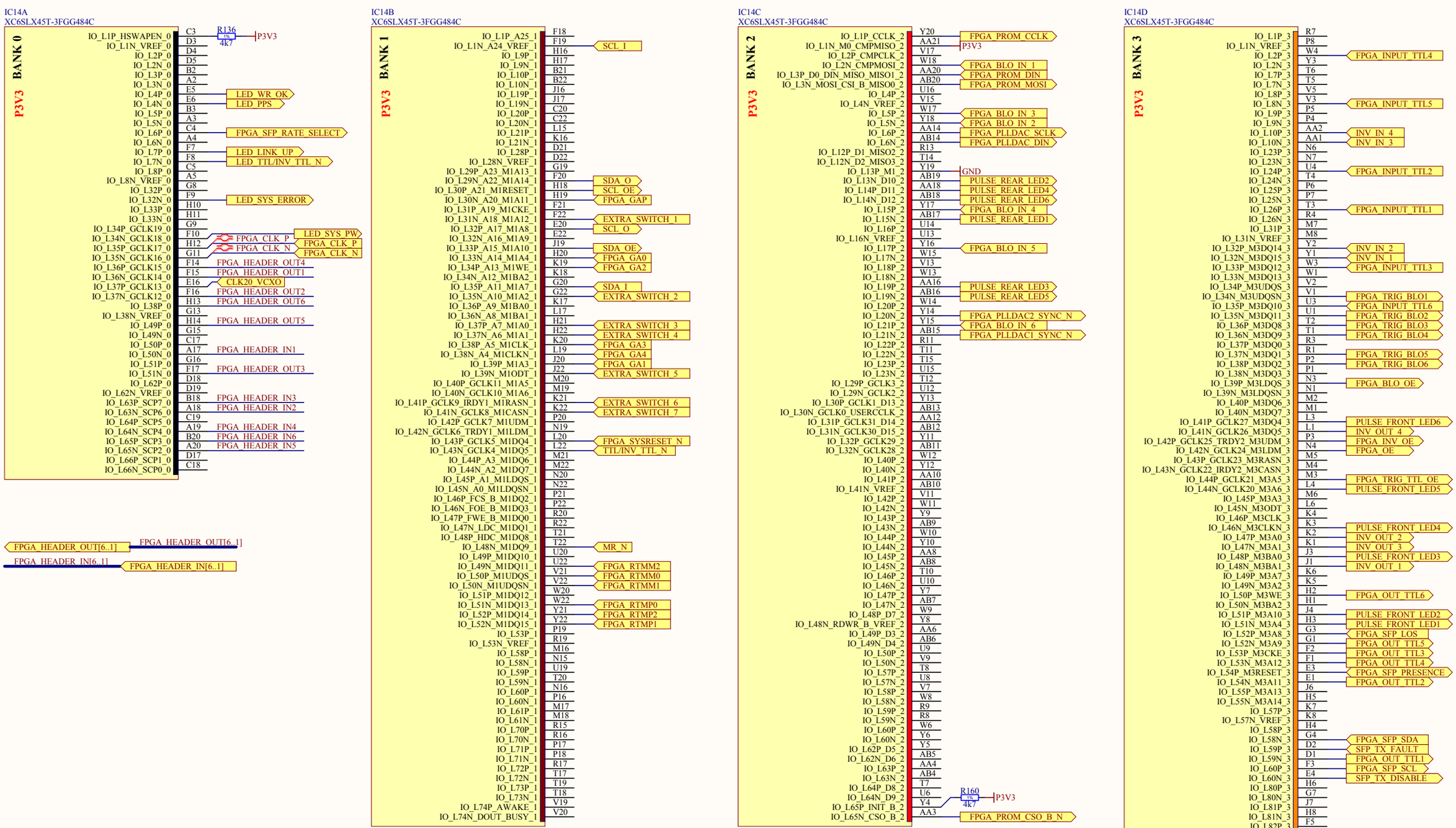

Project/Equipment	Standard Blocking Pulse Repeater
Document	**Conv-TTL-Blo FPGA BANK**
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check.by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	FPGAbank.SchDoc
Print Date	22/02/2012 13:27:02
Sheet	4 of 36
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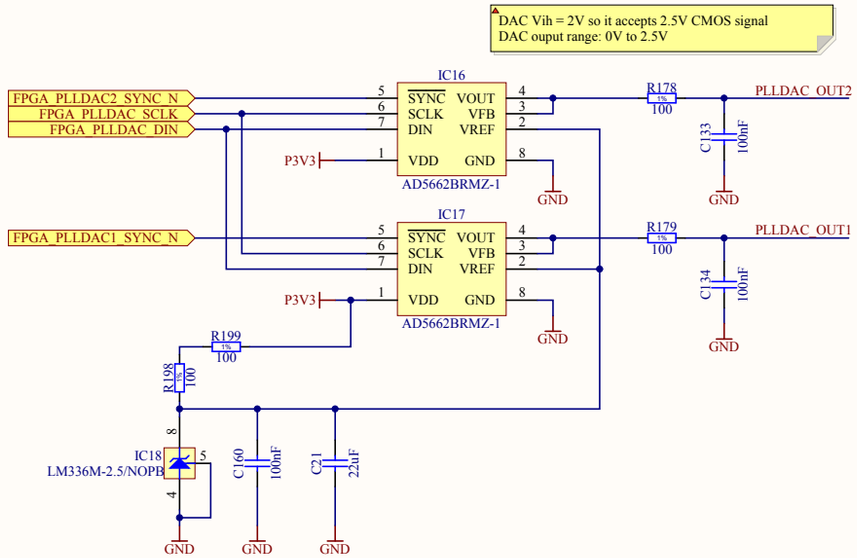

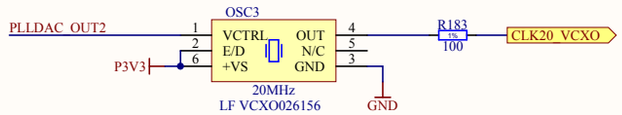

Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo CLOCKS	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File Clocks&Monitor.SchDoc	
		Print Date 22/02/2012 13:27:02	Sheet 5 of 36
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V1-0	Size A3	Rev -

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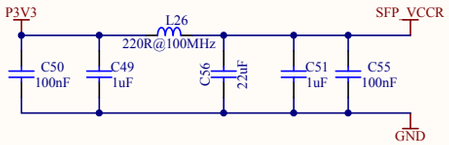

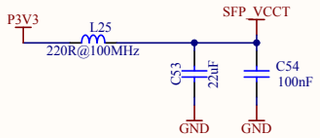

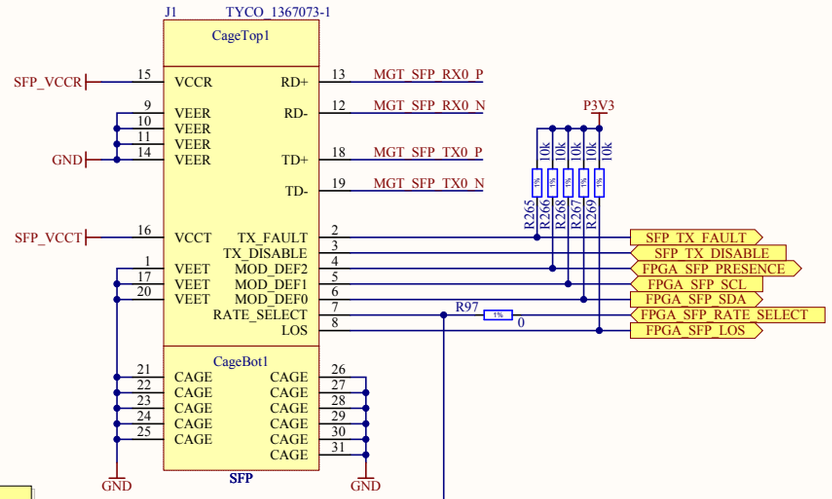

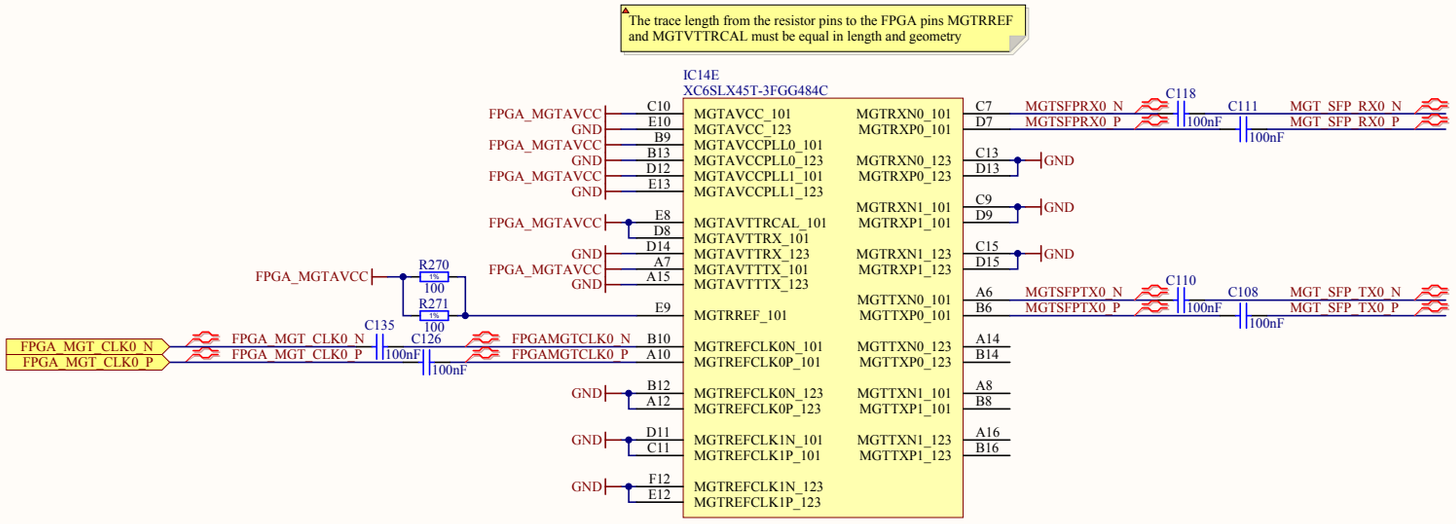

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo MGTX**	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File Communication.SchDoc	
		Print Date 22/02/2012 13:27:02	Sheet 6 of 36
BE-CO CERN	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V1-0	Size A3 / Rev -

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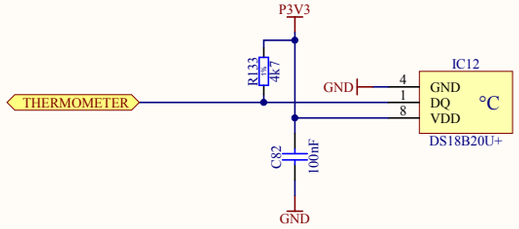
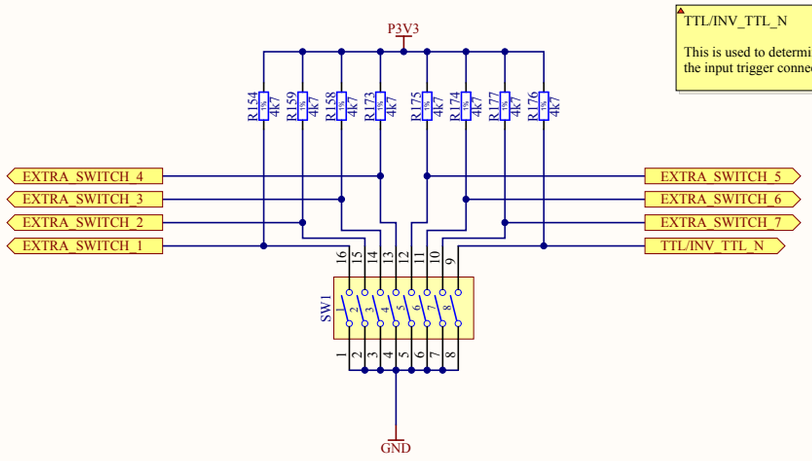
Thermometer will be used to have a FPGA unique ID



RFU switch

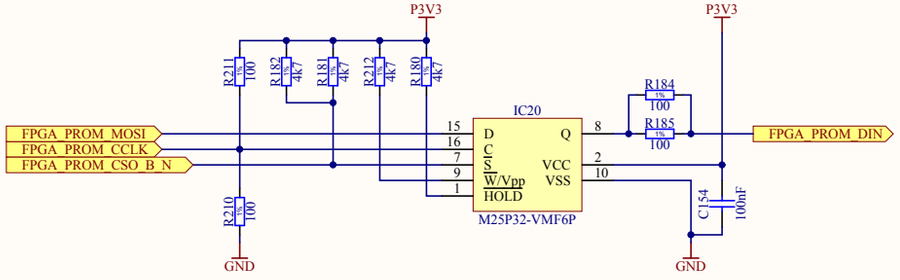
TTL/INV_TTL_N

This is used to determine the level of the input trigger connector

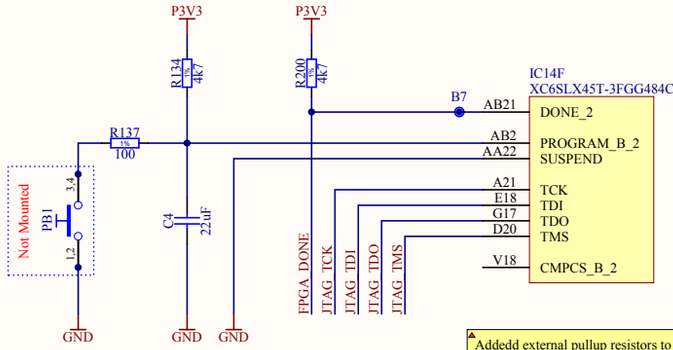


PROM MEMORY

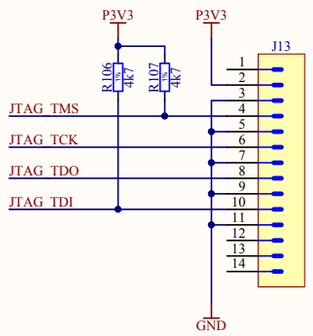
W_N is 1 to allow writes in the memory

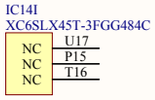


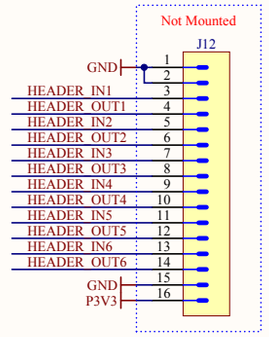
PROGRAM_B must be asserted low for more than 500ns

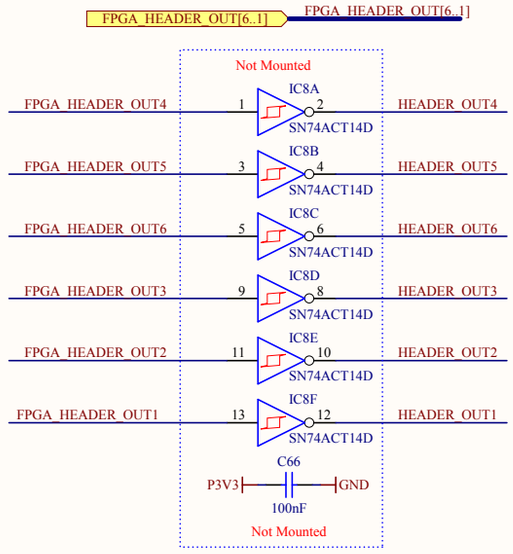


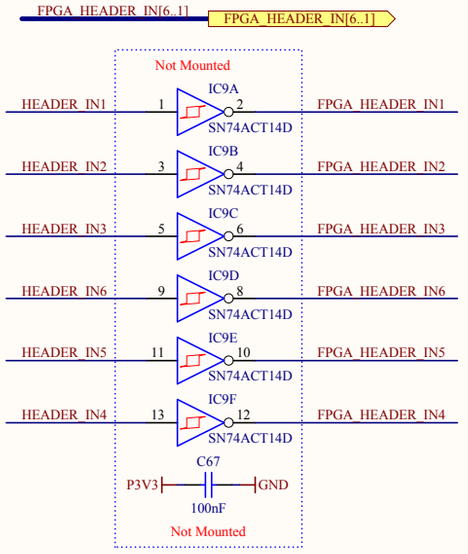
Addeded external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433
However as the JTAG TAP controller fsm is in reset always that TMS experiences two consecutives ones, we can leave it pulled up.
UG380 pg56: the four JTAG pins are internally pulled up.
Hence, there's no need of external ones.











Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo JTAG**	Designer	Carlos Gil Soriano
		Drawn by	Carlos Gil Soriano 10/10/2011
		Check.by	B. Civel 08/12/2011
		Last Mod.	- 22/02/2012
		File	JTAG&Button.SchDoc
		Print Date	22/02/2012 13:27:03 Sheet 7 of 36
BE-CO	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	EDA-02446-V1-0	Size A3 Rev -

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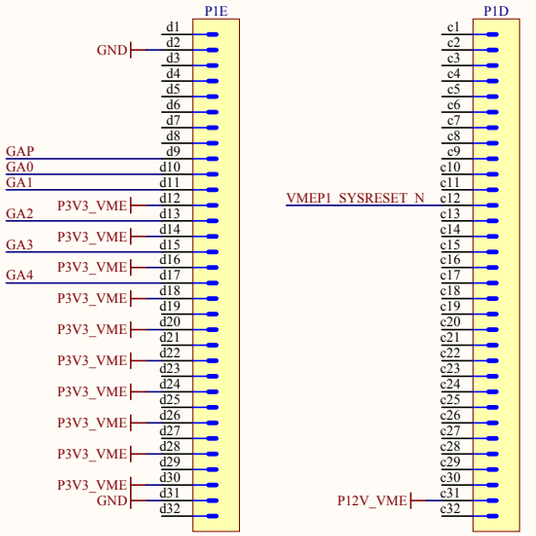
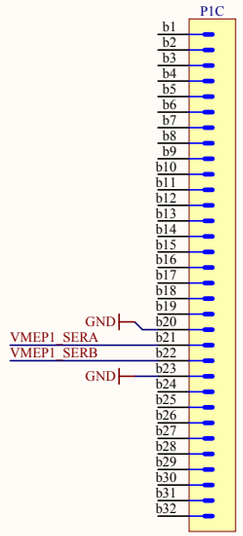
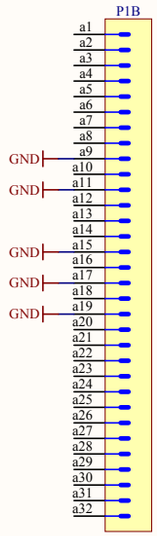
Utility Bus Signal: see page 199
ANSI/VITA 1-1994

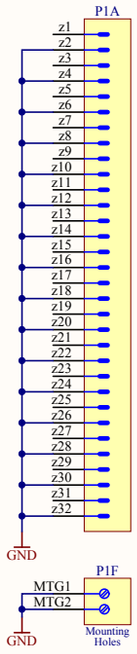
Output configurations in page 230

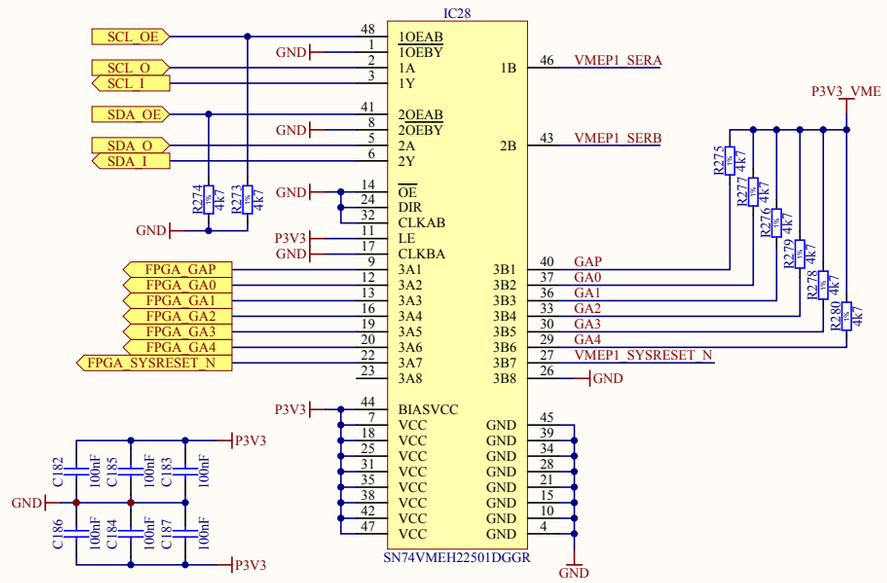
ACFAIL_N	Open collector
SYSFAIL_N	Open collector
SYSRESET_N	Open collector
SYSCLK	Totem-pole







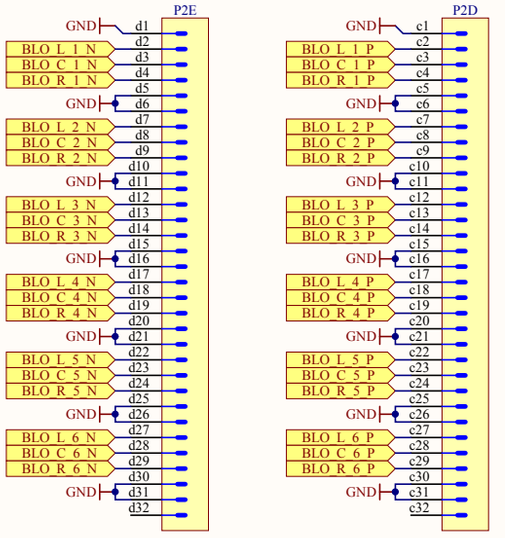


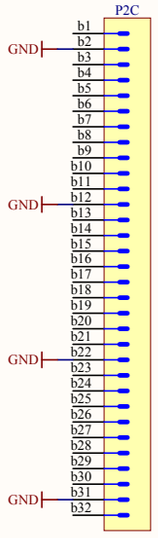


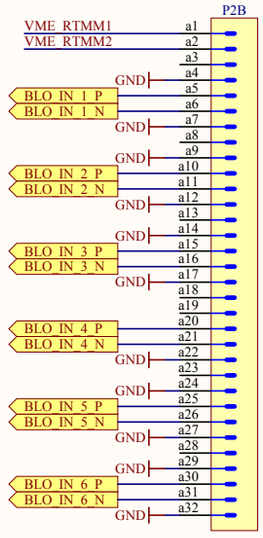
As each block of BLO+_{X}_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical. However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

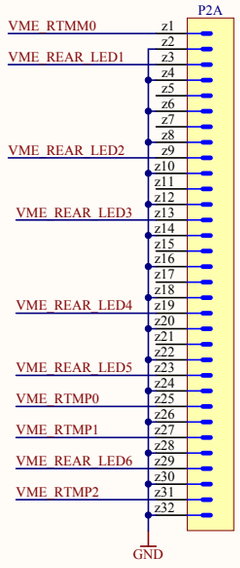
As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo
Signals with more spectral power in higher frequencies should be routed more carefully,so it is better to leave the easiest paths to them.
In this case, outer pins should be available for output signals and inner pins to input ones.

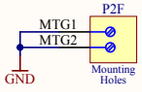
As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used.
Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

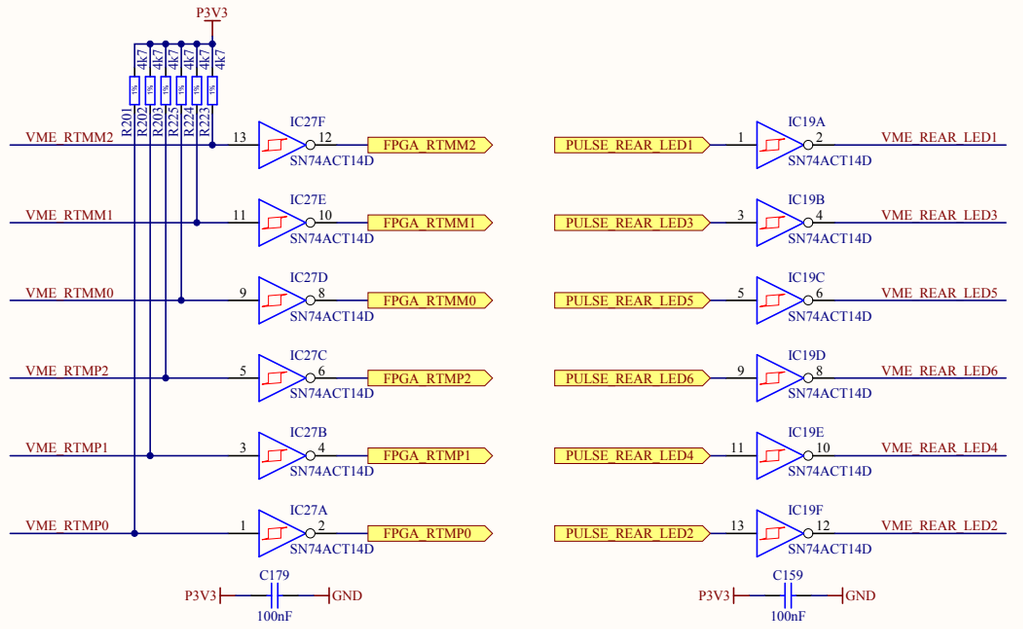












Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo VME64X	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File VME64xConn.SchDoc	
		Print Date 22/02/2012 13:27:03	Sheet 8 of 36
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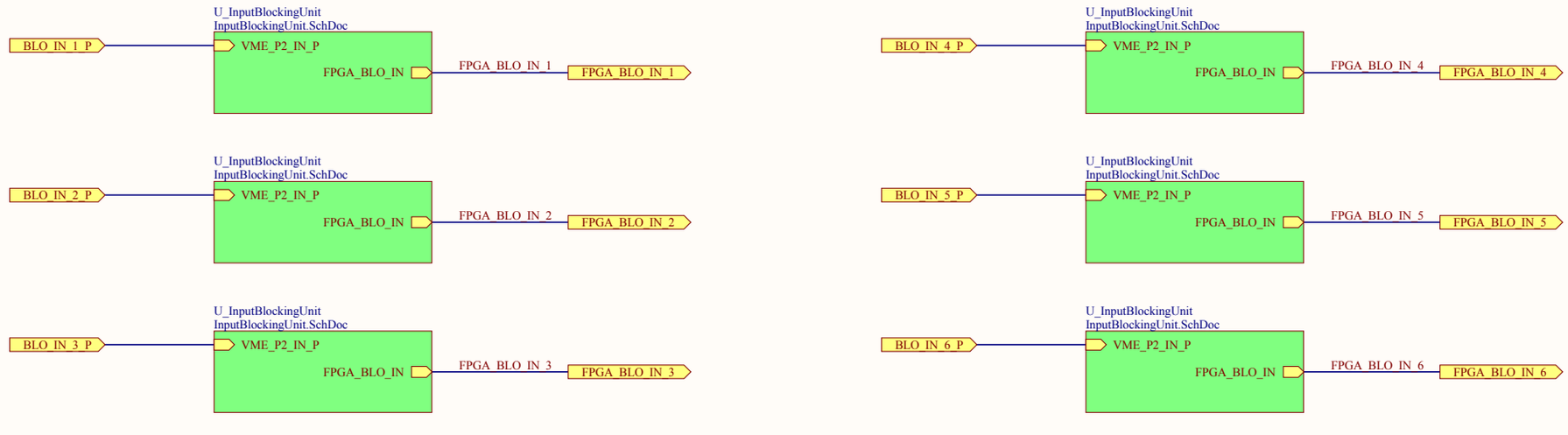

Project/Equipment	Standard Blocking Pulse Repeater		
Document	***Conv-TTL-Blo***	Designer Carlos Gil Soriano	
	INPUT BLO	Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File InputBlocking.SchDoc	
		Print Date 22/02/2012 13:27:03	Sheet 9 of 36
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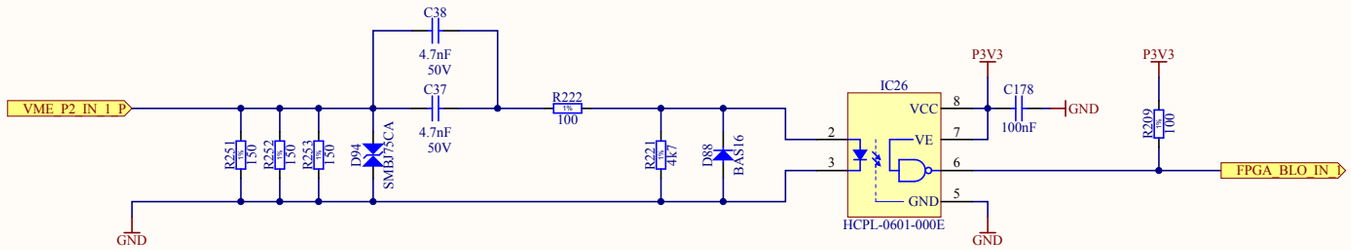
Input waveforms:
nominal 24V Std.Blocking
minimum 4V Std.Blocking

high pass knee frequency: 170 KHz

Minimum isolation voltage: 3750 V



Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo INPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	InputBlockingUnit.SchDoc
Print Date	22/02/2012 13:27:04
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Input waveforms:
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minimum 4V Std.Blocking

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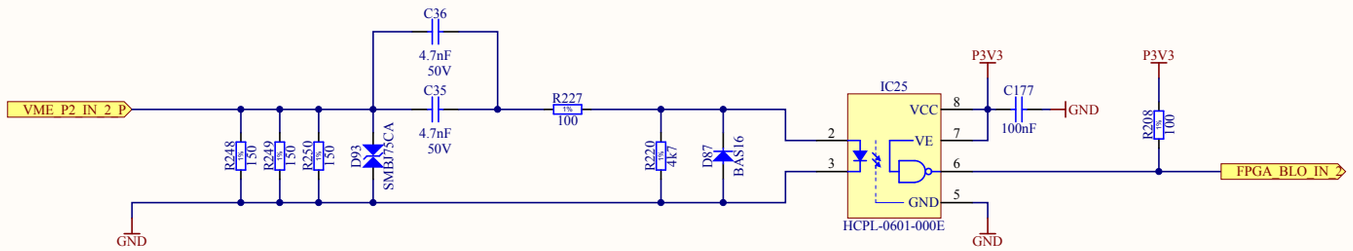

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo INPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	InputBlockingUnit.SchDoc
Print Date	22/02/2012 13:27:04
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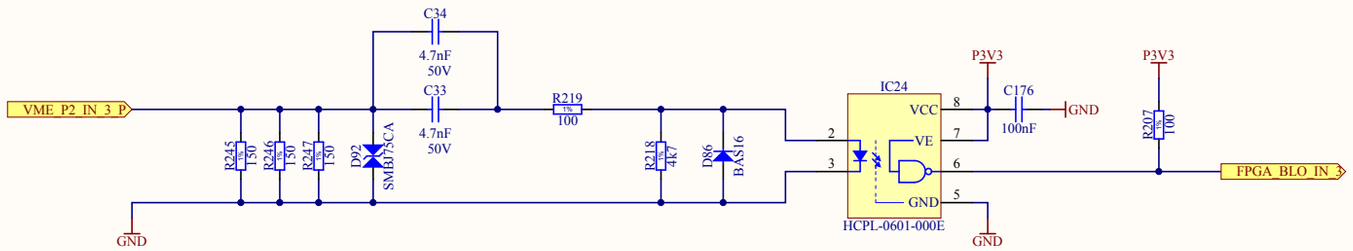

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo INPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	InputBlockingUnit.SchDoc
Print Date	22/02/2012 13:27:04
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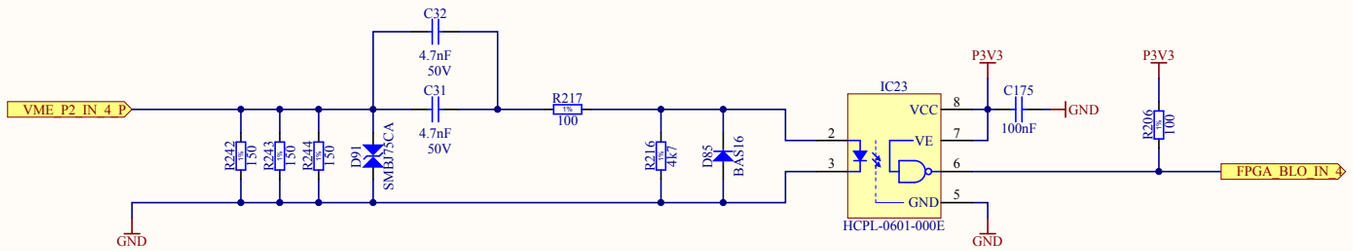

Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo INPUT UNIT	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	10/10/2011
		Check by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File InputBlockingUnit.SchDoc	
		Print Date 22/02/2012 13:27:05	Sheet 10.4 of 36
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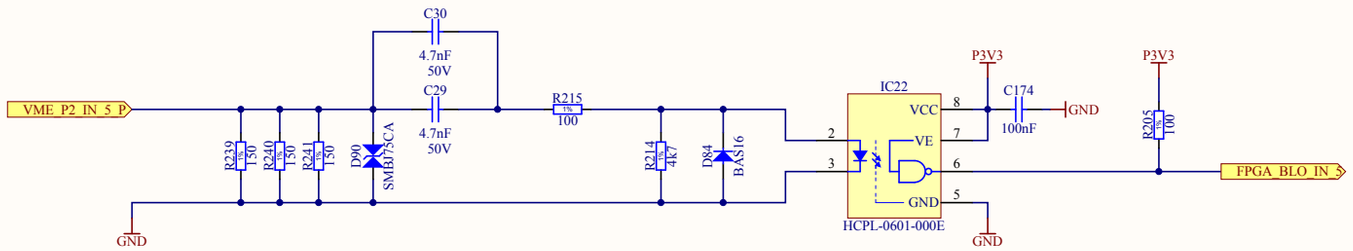
Minimum isolation voltage: 3750 V



Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo INPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	InputBlockingUnit.SchDoc
Print Date	22/02/2012 13:27:05
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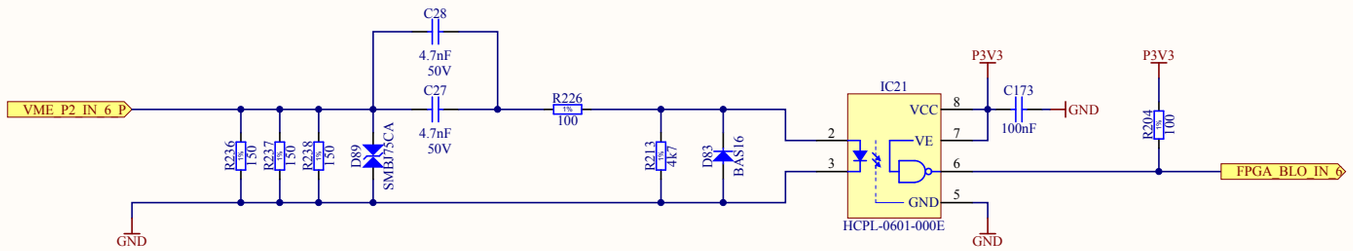

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo INPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	InputBlockingUnit.SchDoc
Print Date	22/02/2012 13:27:05
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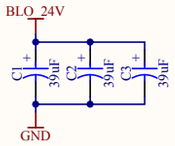
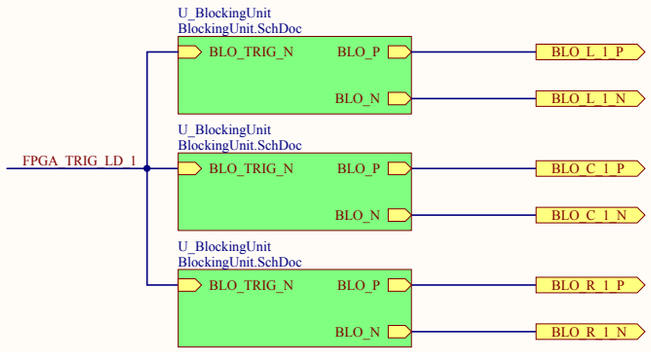
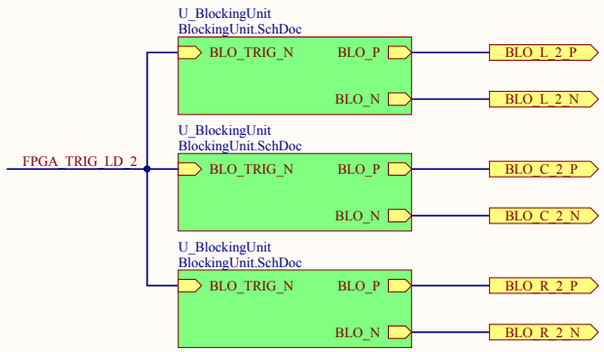
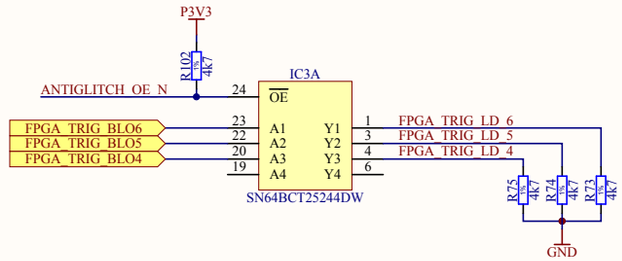
Antiglitch measures:

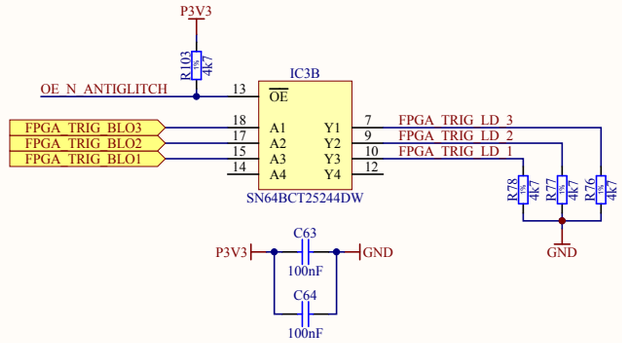
if ANTIGLITCH_OE_N is high the output is high impedance. Then, the pull-down resistors do the rest.

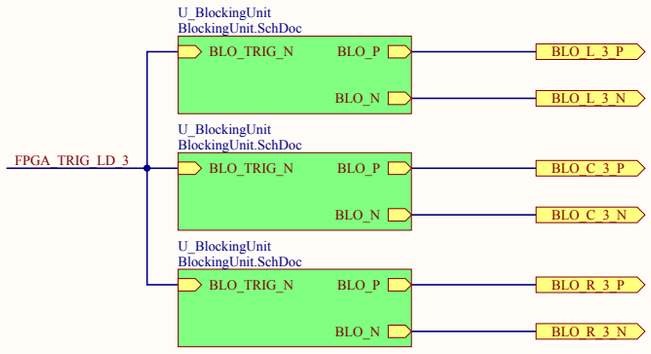


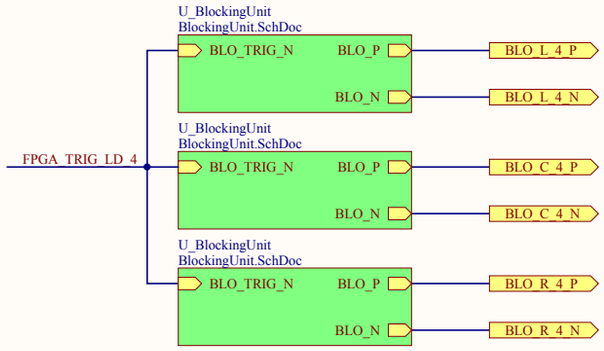


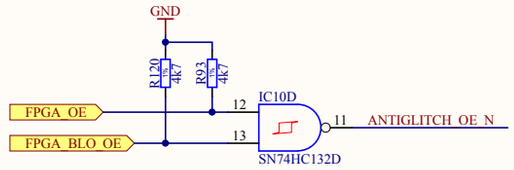


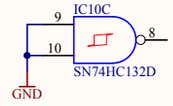


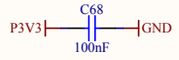


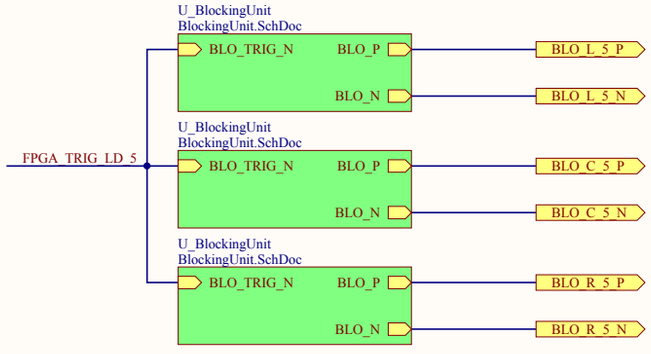


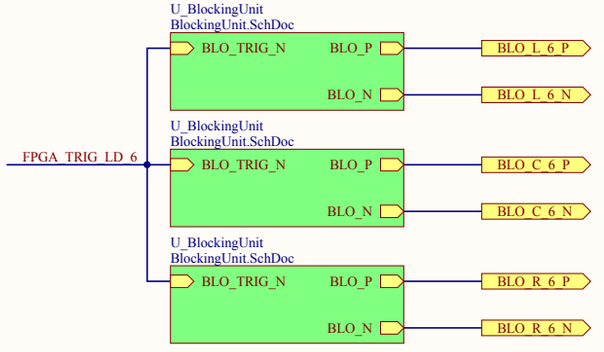












Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT BLO**	Designer	Carlos Gil Soriano
		Drawn by	Carlos Gil Soriano 10/10/2011
		Check.by	B. Civel 08/12/2011
		Last Mod.	- 22/02/2012
		File	BlockingOutput.SchDoc
		Print Date	22/02/2012 13:27:06 Sheet 11 of 36
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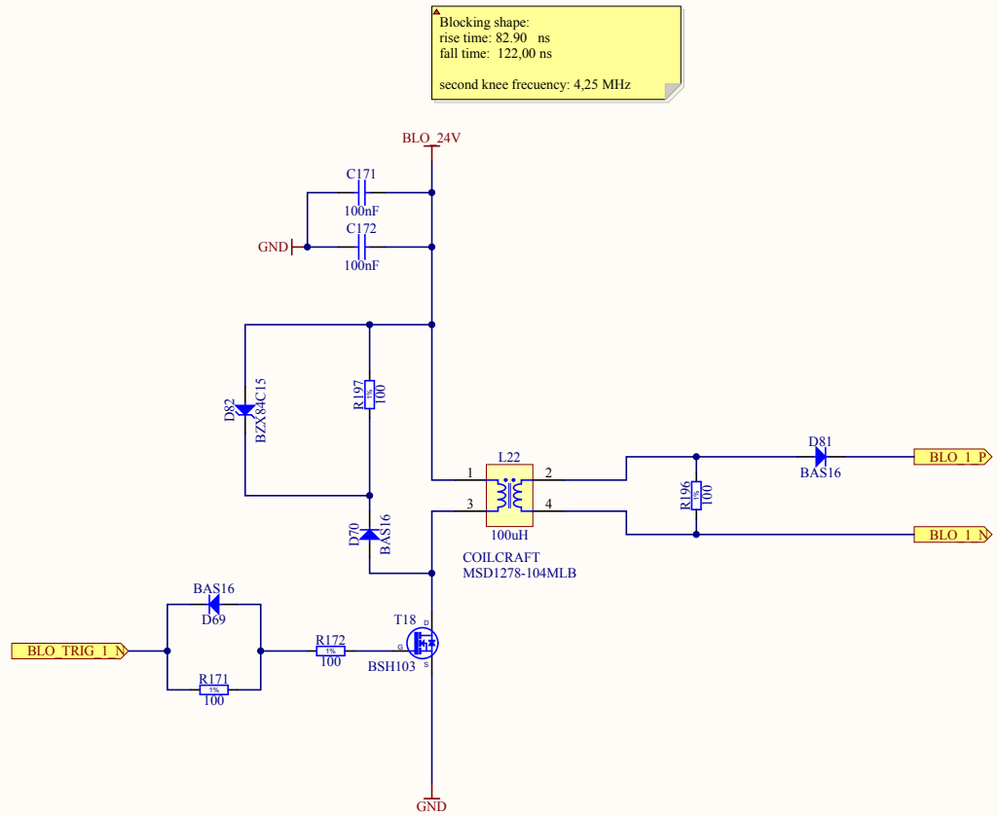

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File BlockingUnit.SchDoc	
		Print Date 22/02/2012 13:27:06	Sheet 12 of 36
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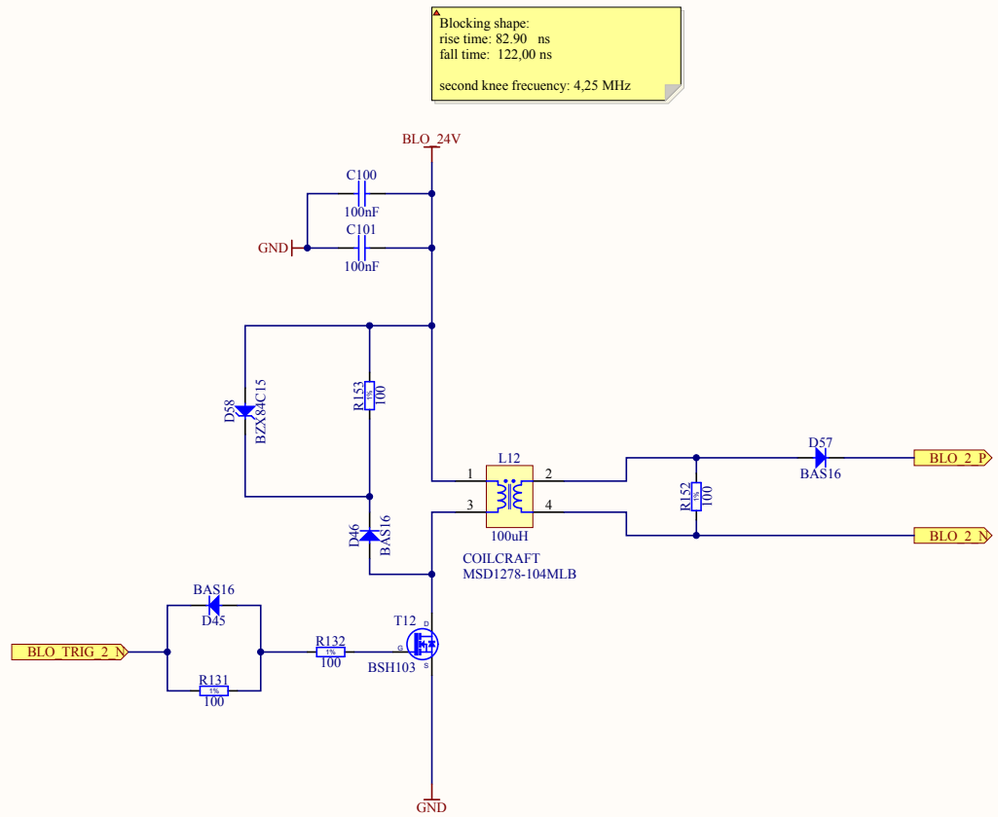

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
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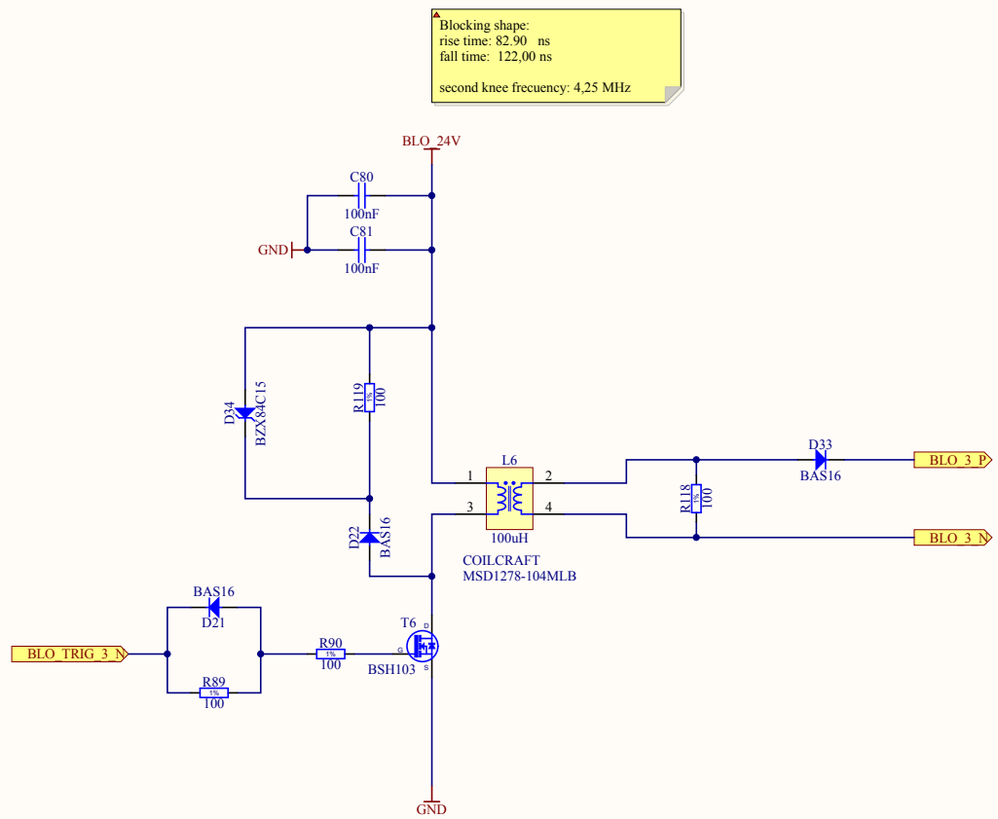

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo OUTPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check.by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	BlockingUnit.SchDoc
Print Date	22/02/2012 13:27:08
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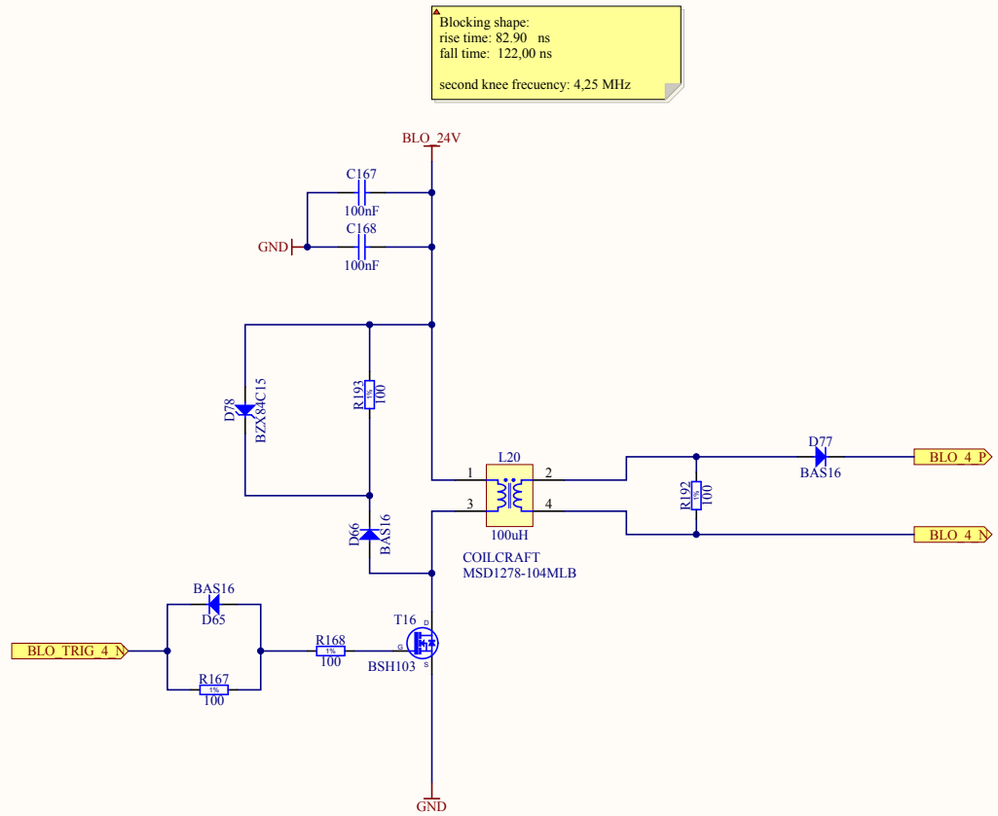

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
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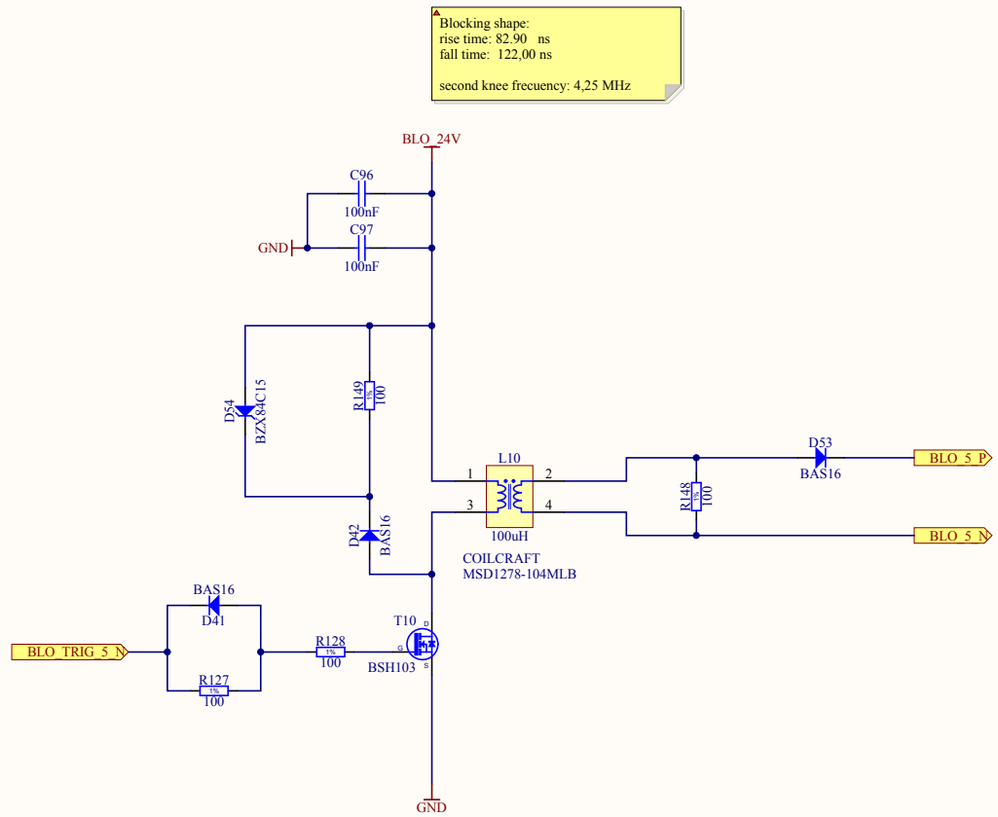

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
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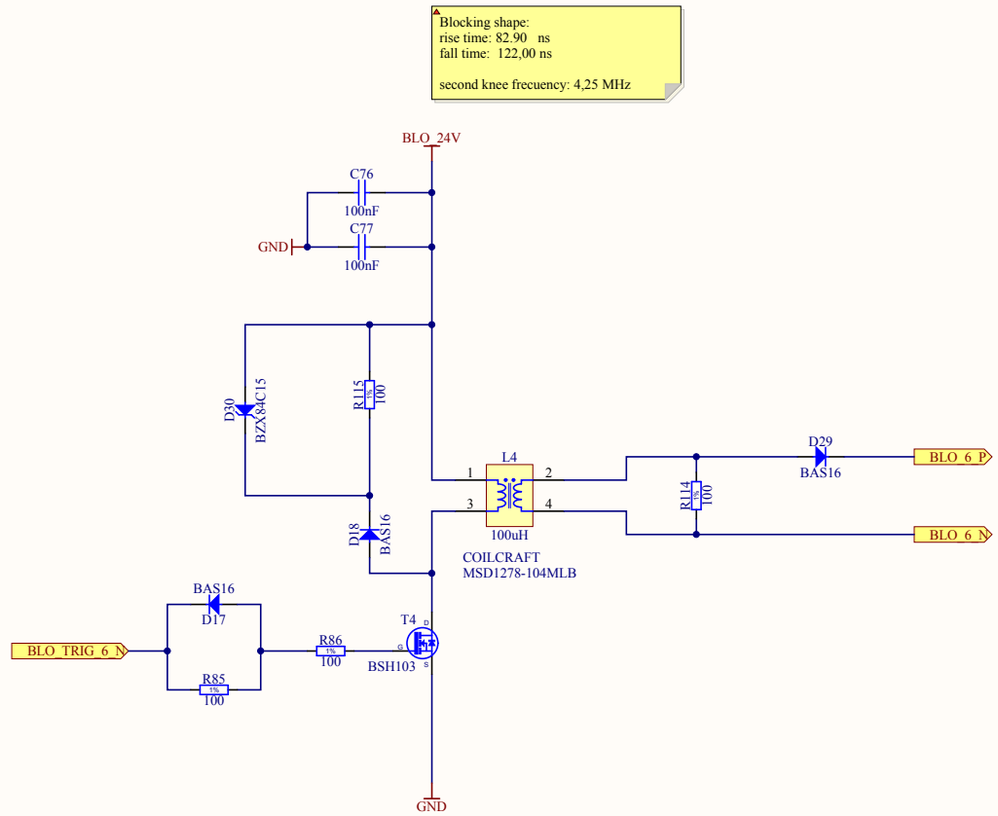

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	10/10/2011
		Check.by B. Civel	08/12/2011
		Last Mod. -	22/02/2012
		File BlockingUnit.SchDoc	
		Print Date 22/02/2012 13:27:10	Sheet 12.6of 36
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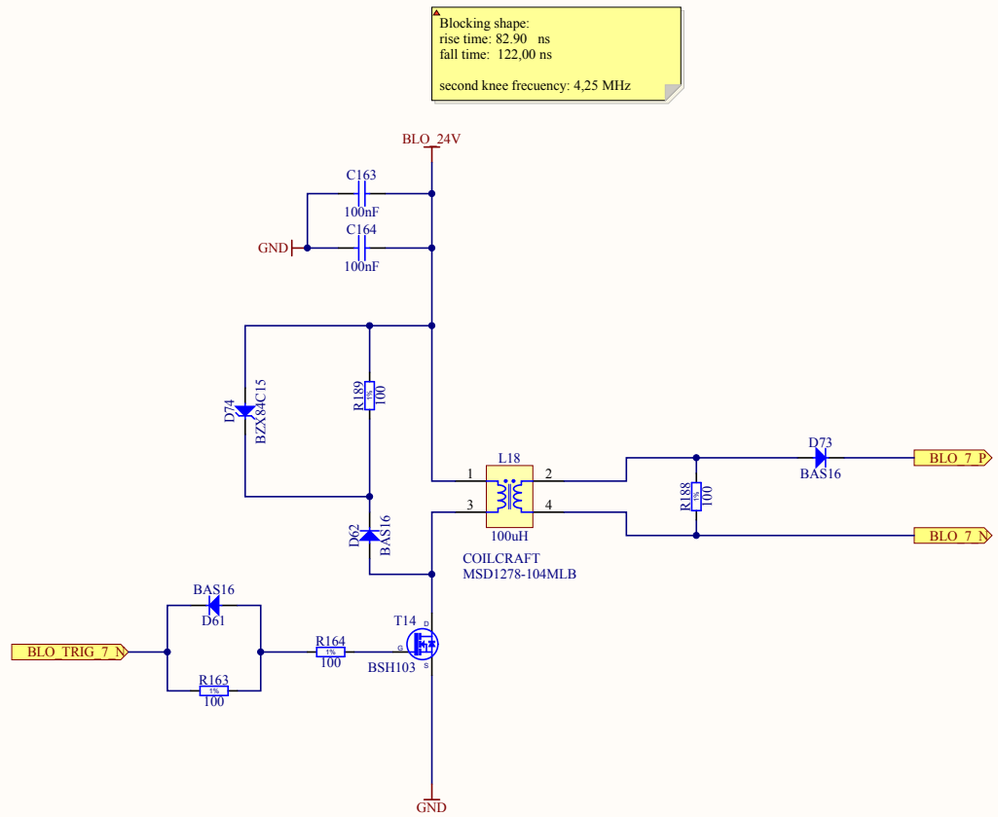

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		Check.by B. Civel	08/12/2011
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		File BlockingUnit.SchDoc	
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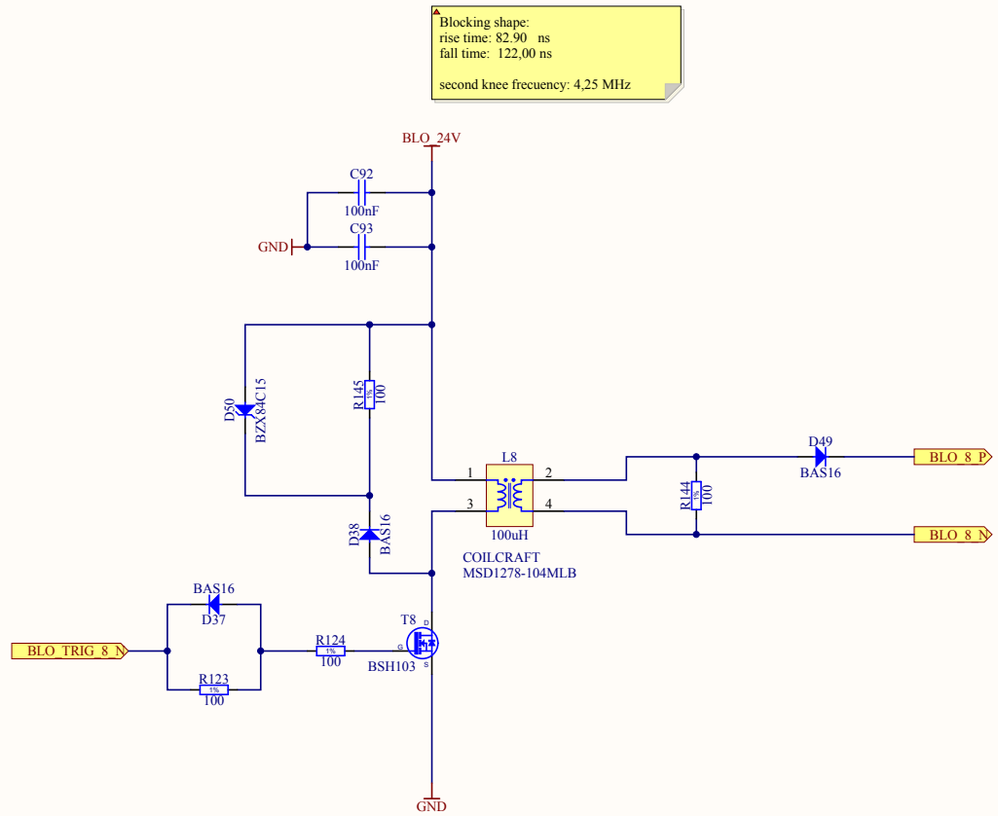

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Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
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		Check.by B. Civel	08/12/2011
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		Print Date 22/02/2012 13:27:12	Sheet 12.8of 36
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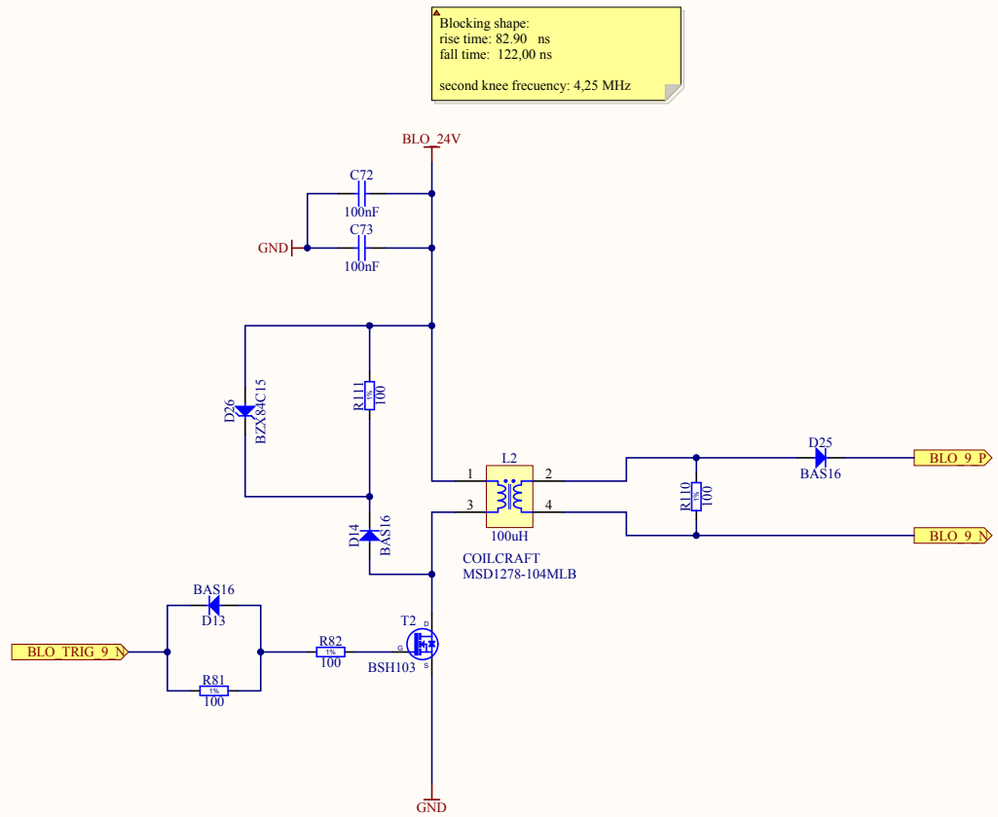

Project/Equipment	Standard Blocking Pulse Repeater
Document	**Conv-TTL-Blo OUTPUT UNIT**
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check.by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	BlockingUnit.SchDoc
Print Date	22/02/2012 13:27:13
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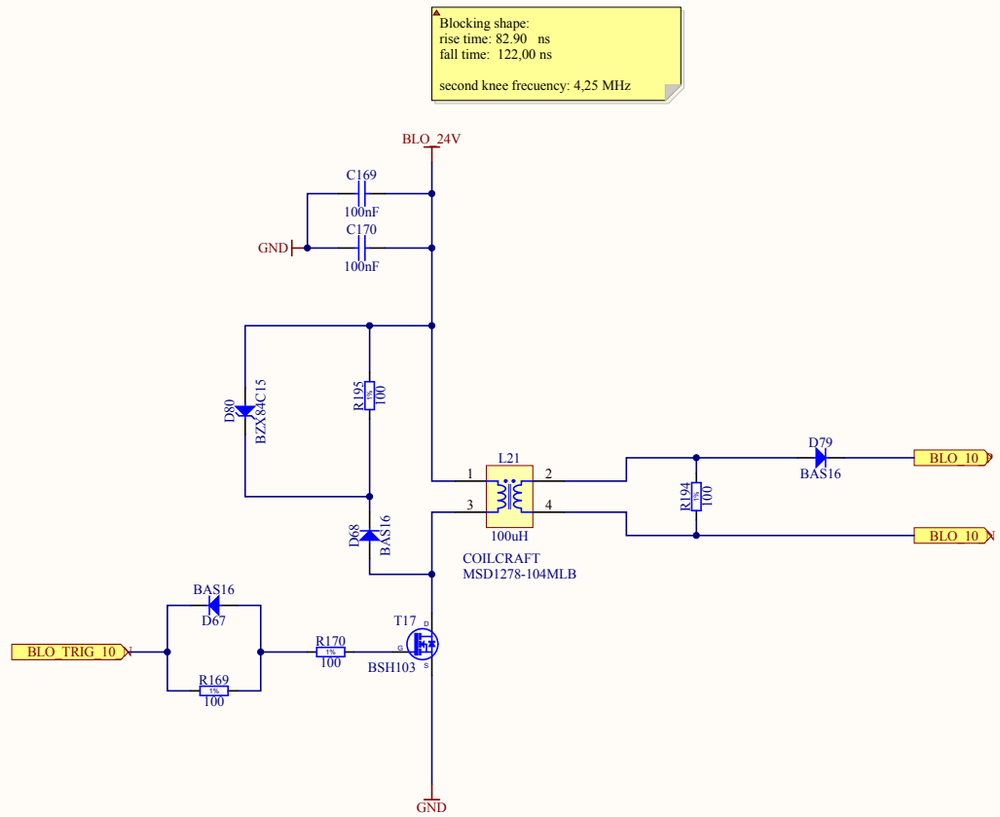

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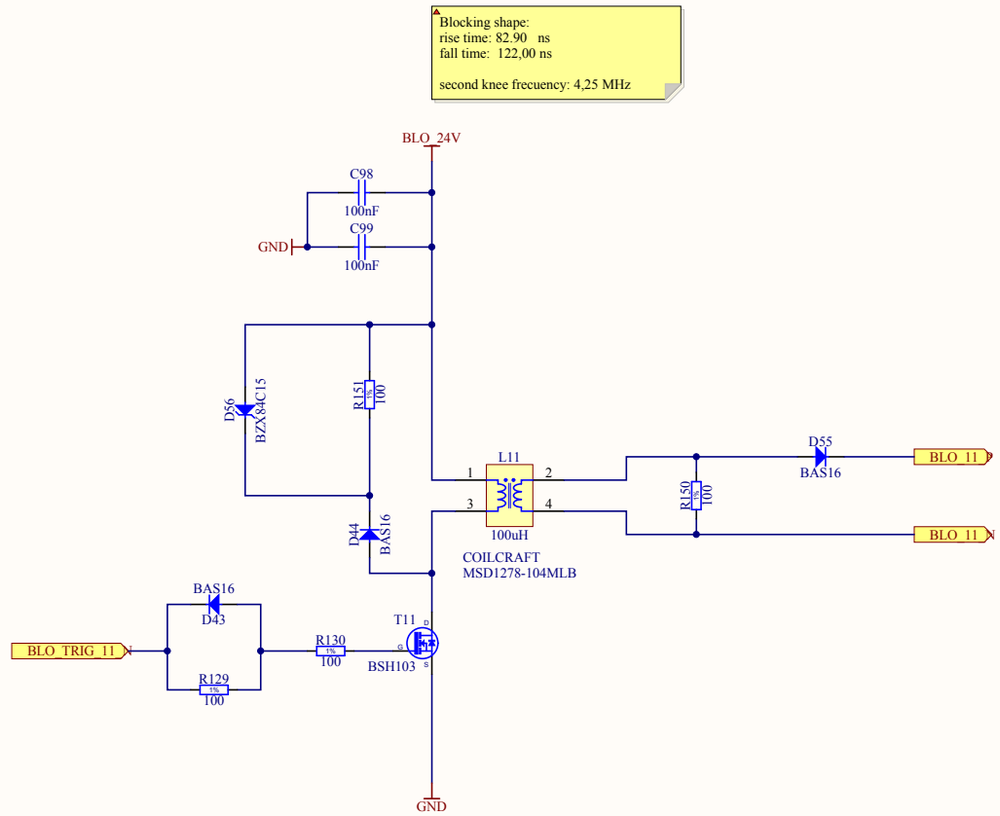

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Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
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		Check.by B. Civel	08/12/2011
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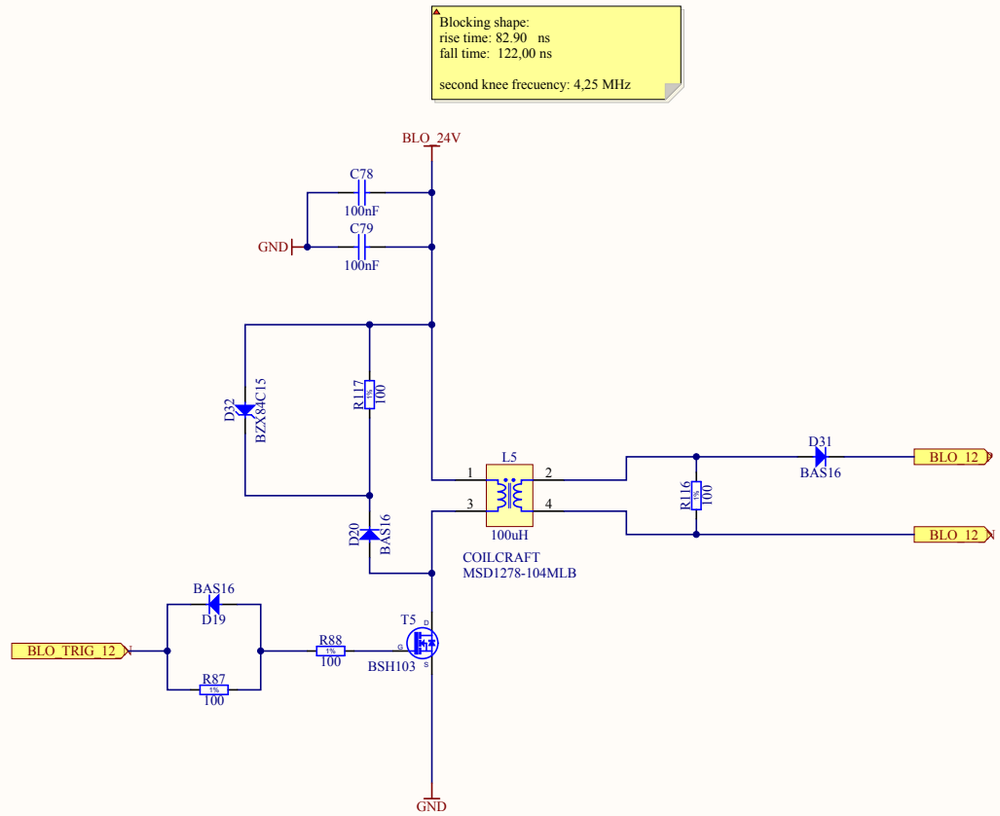

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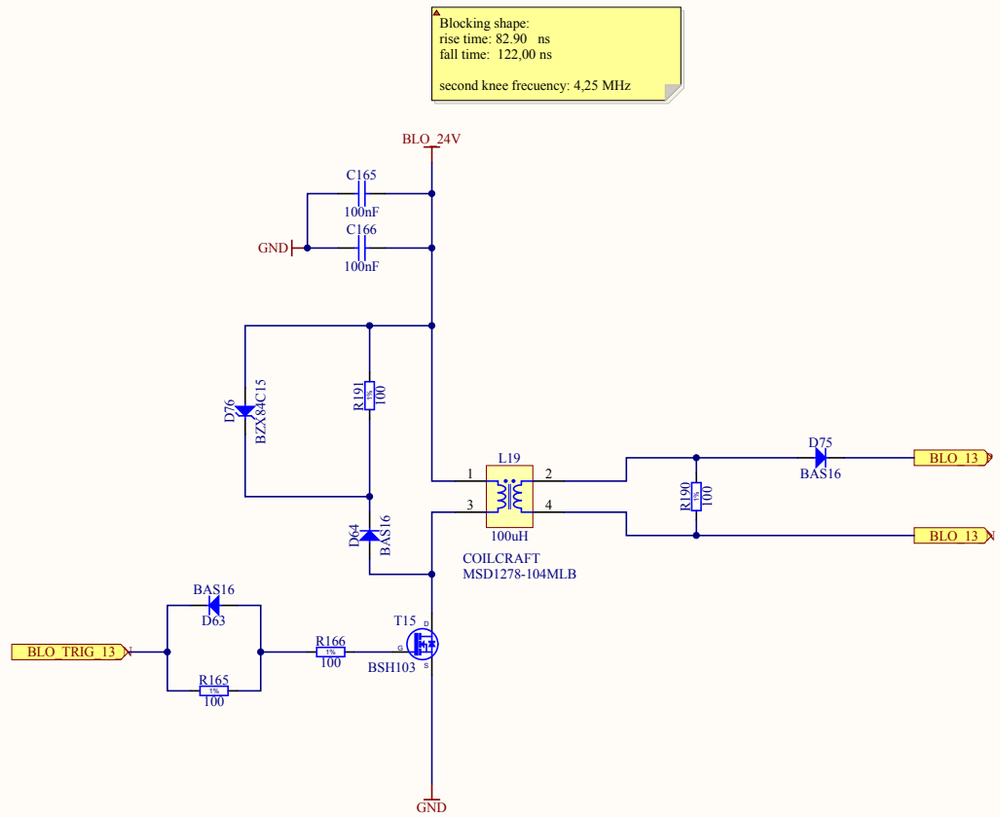

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo OUTPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check.by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	BlockingUnit.SchDoc
Print Date	22/02/2012 13:27:16
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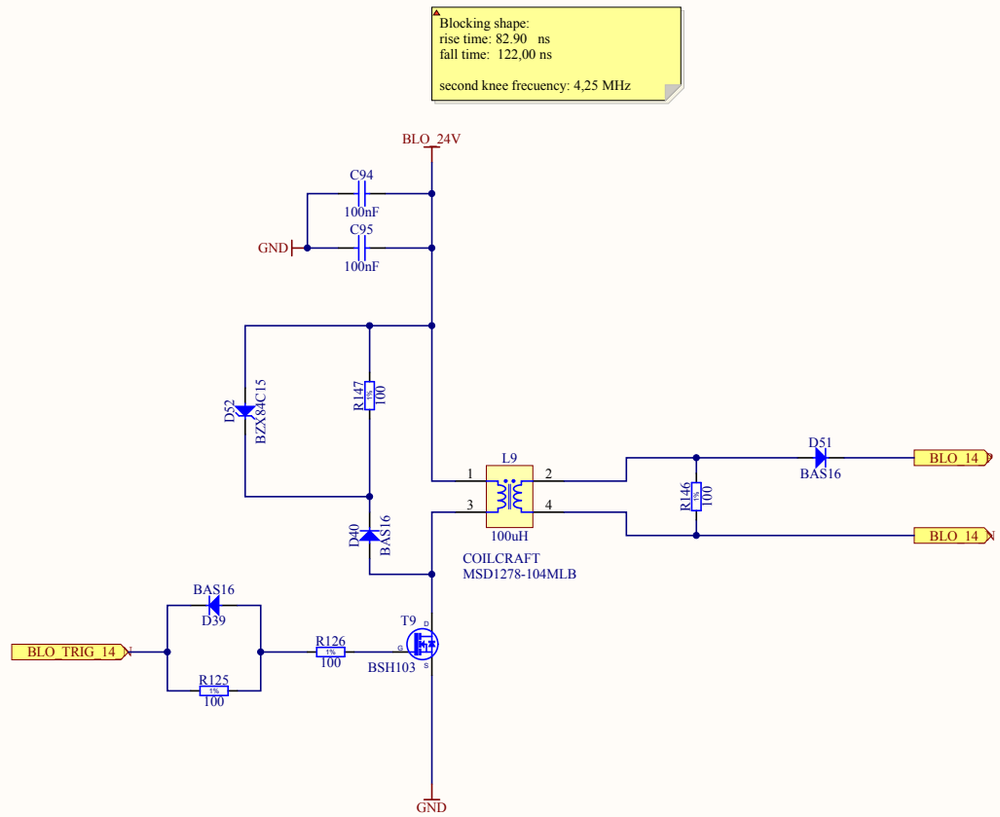

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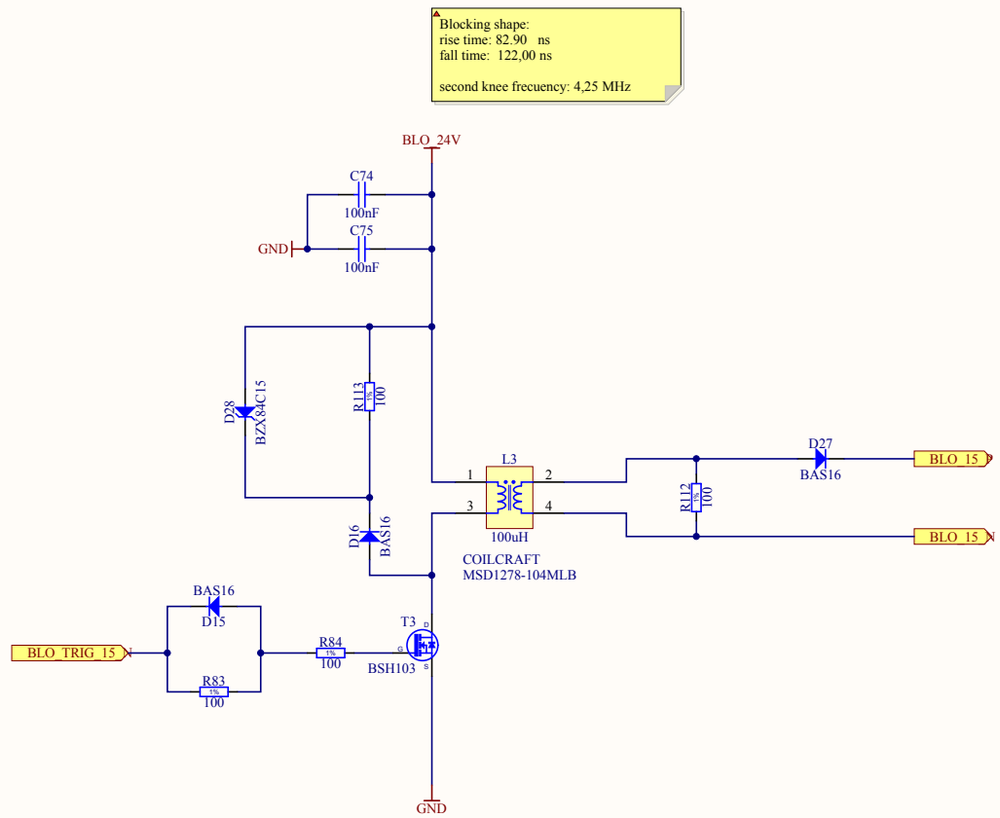

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		Print Date 22/02/2012 13:27:18	Sheet 12 of 36
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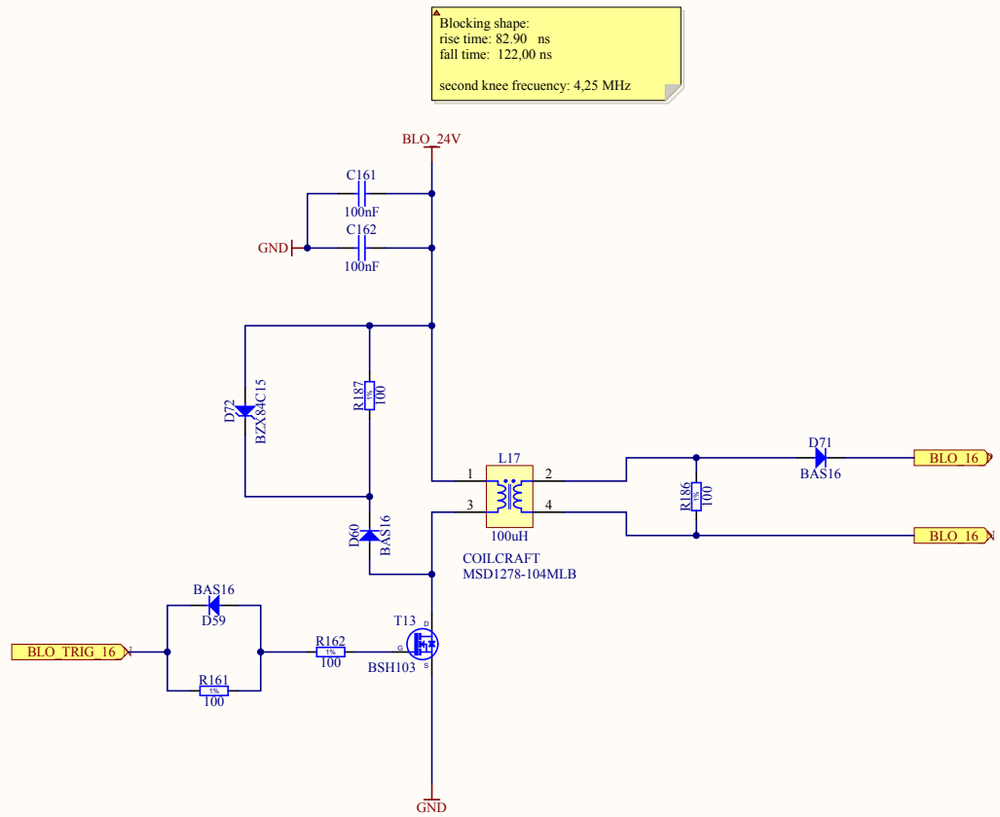

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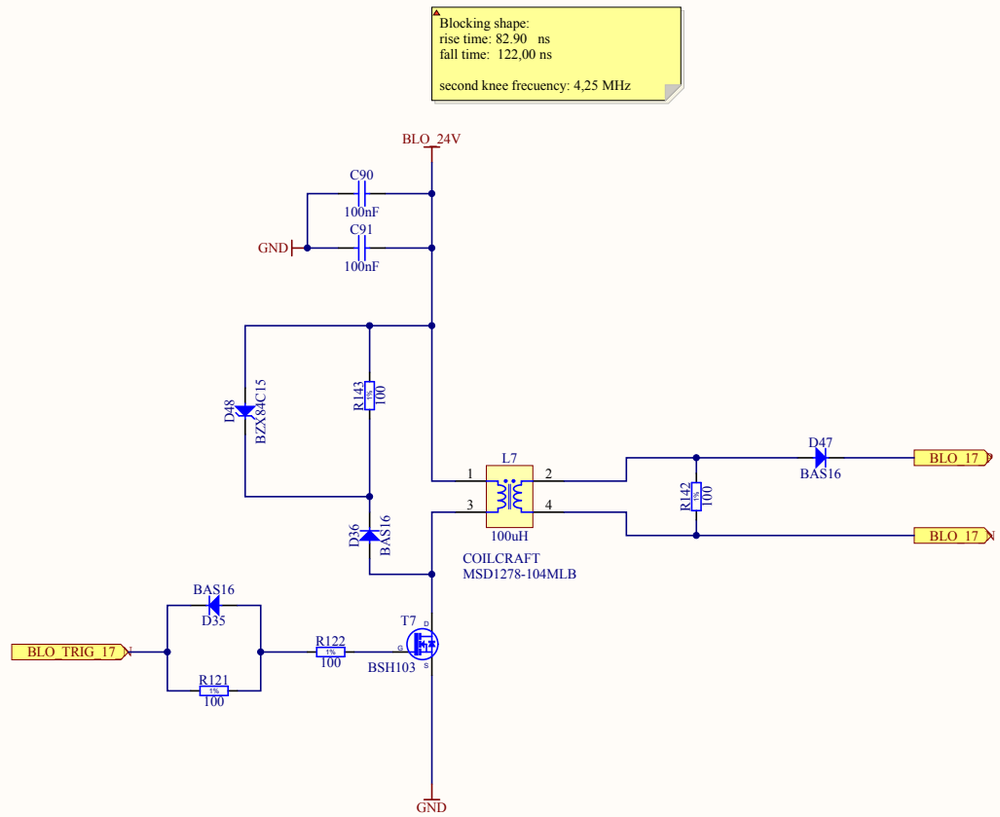

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo OUTPUT UNIT
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 10/10/2011
Check.by	B. Civel 08/12/2011
Last Mod.	- 22/02/2012
File	BlockingUnit.SchDoc
Print Date	22/02/2012 13:27:19
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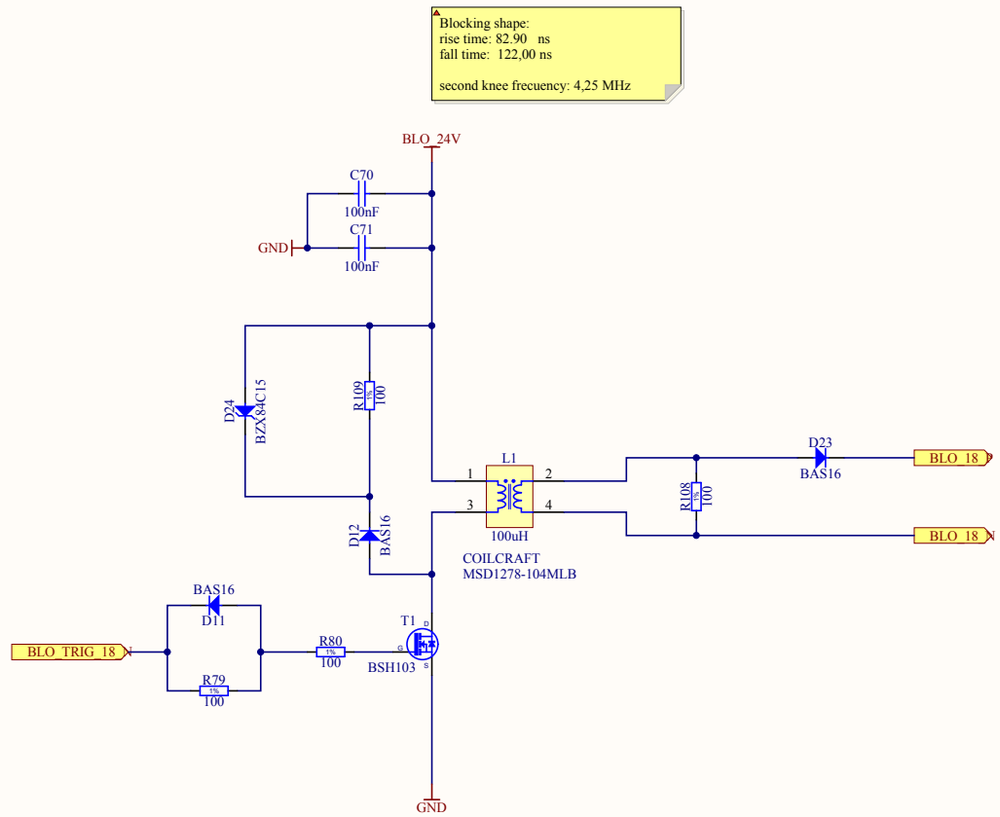

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Input voltage up to 5.5V
TTL intended

J2A BOT LEMO 00 — R13 150, R14 150, R15 150 — R16 150 — D1B BAR66, D1A BAR66 — IC6A SN74ACT14D — FPGA_INPUT_TTL1
J2B TOP LEMO 00 — FPGA_OUTPUT_TTL1
R17 4K7 (Not Mounted)
C58 100nF

J7A BOT LEMO 00 — R38 150, R39 150, R40 150 — R41 150 — D6B BAR66, D6A BAR66 — IC6F SN74ACT14D — FPGA_INPUT_TTL6
J7B TOP LEMO 00 — FPGA_OUTPUT_TTL6
R42 4K7 (Not Mounted)

J3A BOT LEMO 00 — R18 150, R19 150, R20 150 — R22 150 — D2B BAR66, D2A BAR66 — IC6B SN74ACT14D — FPGA_INPUT_TTL2
J3B TOP LEMO 00 — FPGA_OUTPUT_TTL2
R21 4K7 (Not Mounted)

J8A BOT LEMO 00 — R43 150, R44 150, R45 150 — R47 150 — D7B BAR66, D7A BAR66 — IC11A SN74ACT14D — INV_IN_1
J8B TOP LEMO 00 — PANEL_OUTPUT_INV1
R46 4K7 (Not Mounted)
C69 100nF

J4A BOT LEMO 00 — R23 150, R24 150, R25 150 — R26 150 — D3B BAR66, D3A BAR66 — IC6C SN74ACT14D — FPGA_INPUT_TTL3
J4B TOP LEMO 00 — FPGA_OUTPUT_TTL3
R27 4K7 (Not Mounted)

J9A BOT LEMO 00 — R48 150, R49 150, R50 150 — R51 150 — D8B BAR66, D8A BAR66 — IC11B SN74ACT14D — INV_IN_2
J9B TOP LEMO 00 — PANEL_OUTPUT_INV2
R52 4K7 (Not Mounted)

J5A BOT LEMO 00 — R28 150, R29 150, R30 150 — R32 150 — D4B BAR66, D4A BAR66 — IC6D SN74ACT14D — FPGA_INPUT_TTL4
J5B TOP LEMO 00 — FPGA_OUTPUT_TTL4
R31 4K7 (Not Mounted)

J10A BOT LEMO 00 — R53 150, R54 150, R55 150 — R57 150 — D9B BAR66, D9A BAR66 — IC11C SN74ACT14D — INV_IN_3
J10B TOP LEMO 00 — PANEL_OUTPUT_INV3
R56 4K7 (Not Mounted)

J6A BOT LEMO 00 — R33 150, R34 150, R35 150 — R36 150 — D5B BAR66, D5A BAR66 — IC6E SN74ACT14D — FPGA_INPUT_TTL5
J6B TOP LEMO 00 — FPGA_OUTPUT_TTL5
R37 4K7 (Not Mounted)

J11A BOT LEMO 00 — R58 150, R59 150, R60 150 — R61 150 — D10B BAR66, D10A BAR66 — IC11D SN74ACT14D — INV_IN_4
J11B TOP LEMO 00 — PANEL_OUTPUT_INV4
R62 4K7 (Not Mounted)

P3V3 — R100 4K7

IC1A SN64BCT25244DW
FPGA_OUT_TTL1 → FPGA_OUTPUT_TTL1
FPGA_OUT_TTL2 → FPGA_OUTPUT_TTL2
FPGA_OUT_TTL3 → FPGA_OUTPUT_TTL3
R65 4K7, R64 4K7, R63 4K7

IC1B SN64BCT25244DW
FPGA_OUT_TTL4 → FPGA_OUTPUT_TTL4
FPGA_OUT_TTL5 → FPGA_OUTPUT_TTL5
FPGA_OUT_TTL6 → FPGA_OUTPUT_TTL6
R68 4K7, R67 4K7, R66 4K7
C59 100nF
C60 100nF

FPGA_TRIG_TTL_OE
FPGA_OE
FPGA_INV_OE
IC10A SN74HC132D
IC10B SN74HC132D
R94 4K7, R95 4K7, R92 4K7

R101 4K7
IC2A SN64BCT25244DW
INV_OUT_1 → PANEL_OUTPUT_INV1
INV_OUT_2 → PANEL_OUTPUT_INV2
INV_OUT_3 → PANEL_OUTPUT_INV3
INV_OUT_4 → PANEL_OUTPUT_INV4
R72 4K7, R71 4K7, R70 4K7, R69 4K7

IC2B SN64BCT25244DW
C61 100nF
C62 100nF

IC11F SN74ACT14D

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo FRONT TTL**	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	10/10/2011
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		File FrontTTL.SchDoc	
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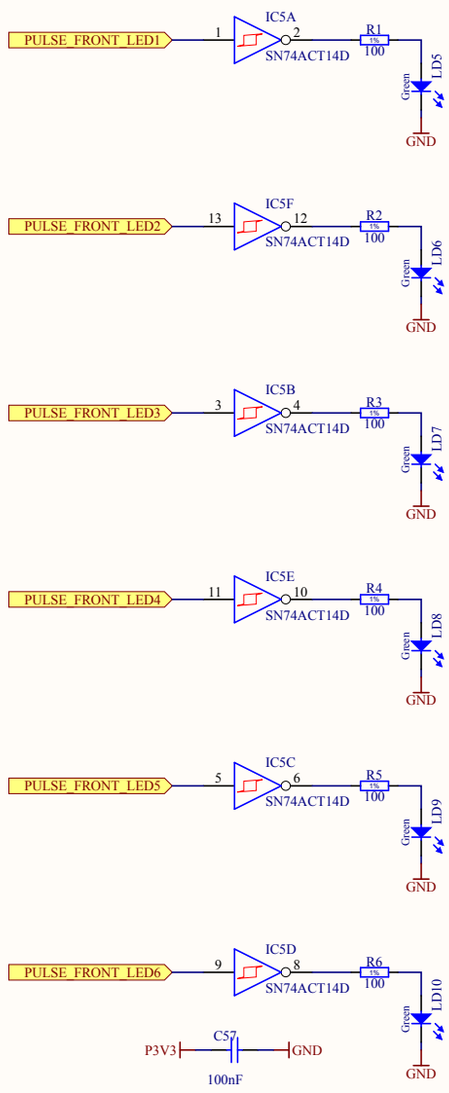
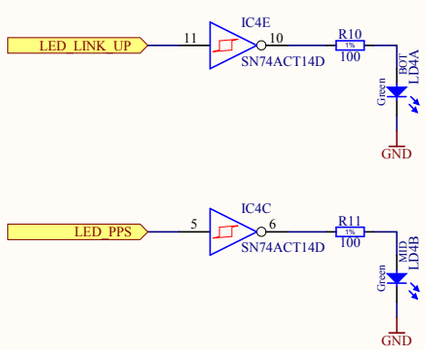
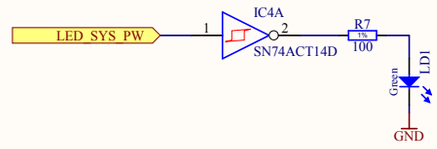
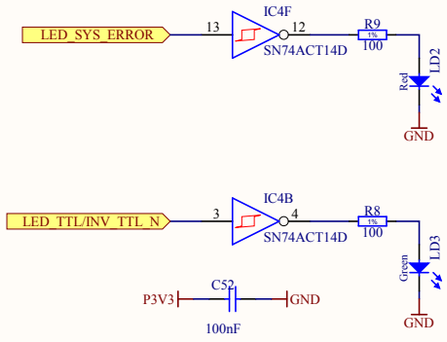


Dialight model

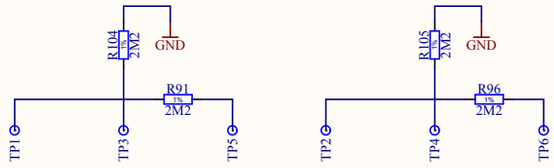
Green	551-1307F	2.5V@ 4.7mA
Red	551-1107F	1.9V@ 6mA







ESD discharge strips (top and bottom of the card)



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Document	**Conv-TTL-Blo FRONT PANEL**	Designer Carlos Gil Soriano	
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