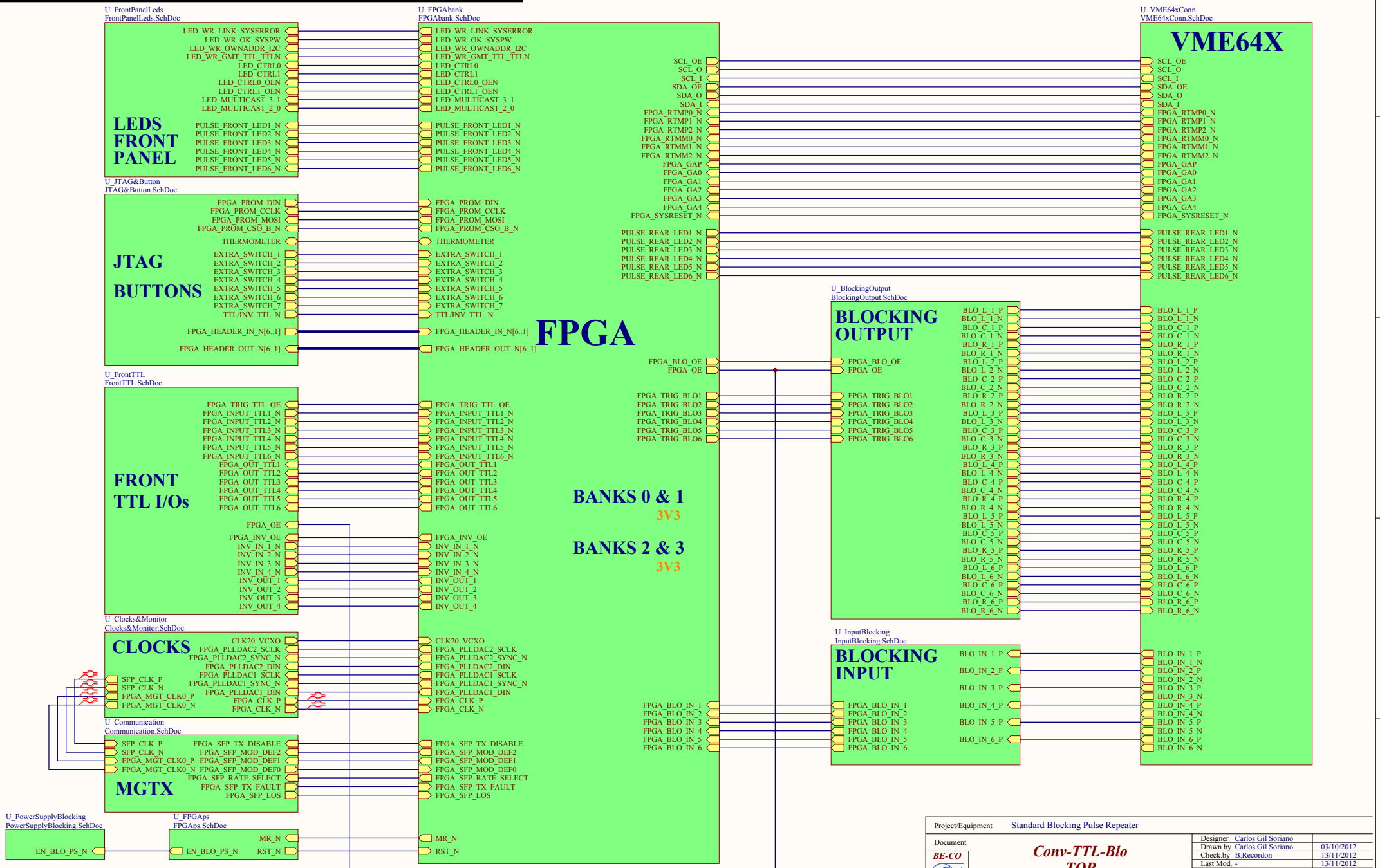

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo TOP
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check by	B.Recordon 13/11/2012
Last Mod.	- 13/11/2012
File	ConvTtlBlo_TOP.SchDoc
Print Date	13/11/2012 08:50:31
Sheet	1 of 14
Size	A3
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BE-CO

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Efficiency of 85% and better

IC31 TPS54312PWP

IC29 TPS3808G01DBVT

IC11E SN74LVC14AD

IC11F SN74LVC14AD

Capacitor CT not mounted: delay of 570ms

Voltages are:

*** FPGA	
VCCO_0	3V3
VCCO_1	3V3
VCCO_2	3V3
VCCO_3	3V3
VCCaux	3V3
VCCint	1V2
*** PROM	
VCCaux	3V3

IC14G XC6SLX45T-3FGG484C

IC14H XC6SLX45T-3FGG484C

Test points

PI filters for decoupling noise in the band of 50 MHz to 150 MHz in 3V3 and 5V rails.

BLM41PG181SN1L is a ferrite with low DCR (max 10mOhm) targeted for high current (power rails).

VCCO_int decoupling capacitors

VCCO_0 decoupling capacitors

VCCO_1 decoupling capacitors

VCCO_2 decoupling capacitors

VCCO_3 decoupling capacitors

VCCAUX decoupling capacitors

Project/Equipment	Standard Blocking Pulse Repeater
Document	Conv-TTL-Blo FPGA PS
Designer	Carlos Gil Soriano
Drawn by	Carlos Gil Soriano 03/10/2012
Check by	B.Recordon 13/11/2012
Last Mod.	- 13/11/2012
File	FPGAps.SchDoc
Print Date	13/11/2012 08:50:32
Sheet	2 of 14
Size	A3
Rev	1

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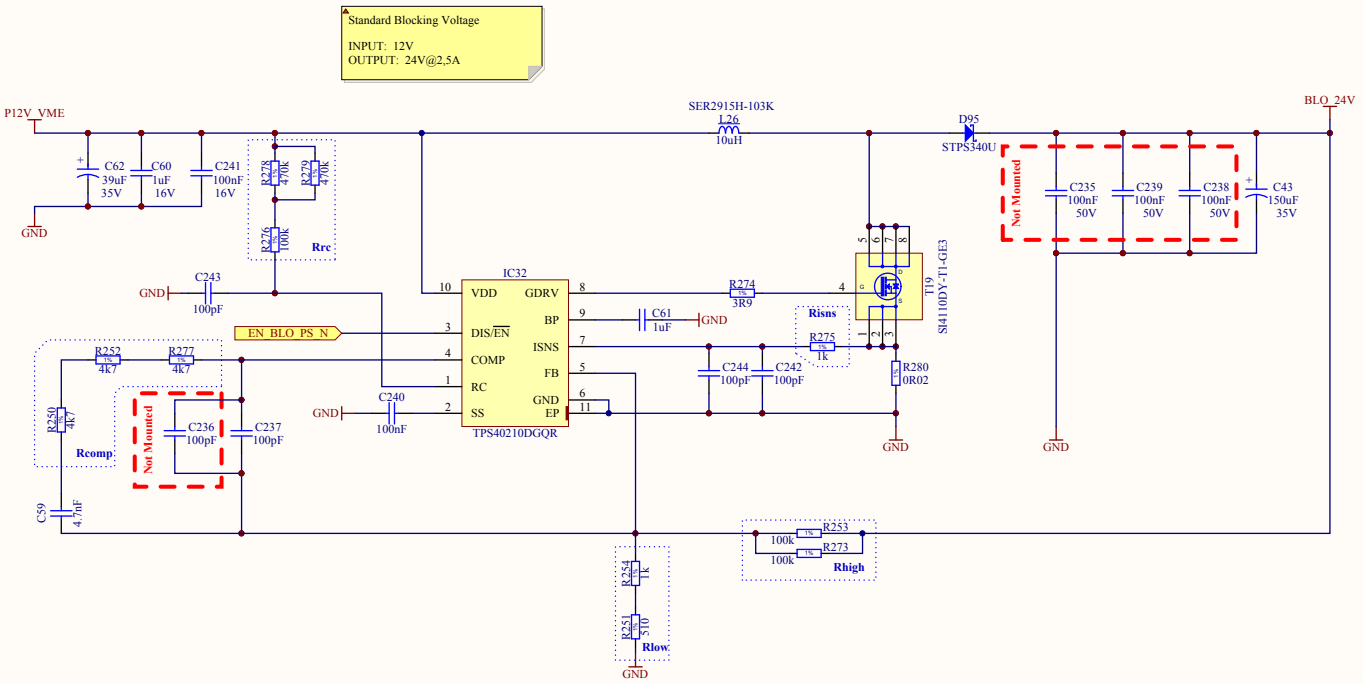

Project/Equipment	Standard Blocking Pulse Repeater		
Document	*Conv-TTL-Blo BLOCKING PS*	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File PowerSupplyBlocking.SchDoc	
		Print Date 13/11/2012 08:50:32	Sheet 3 of 14
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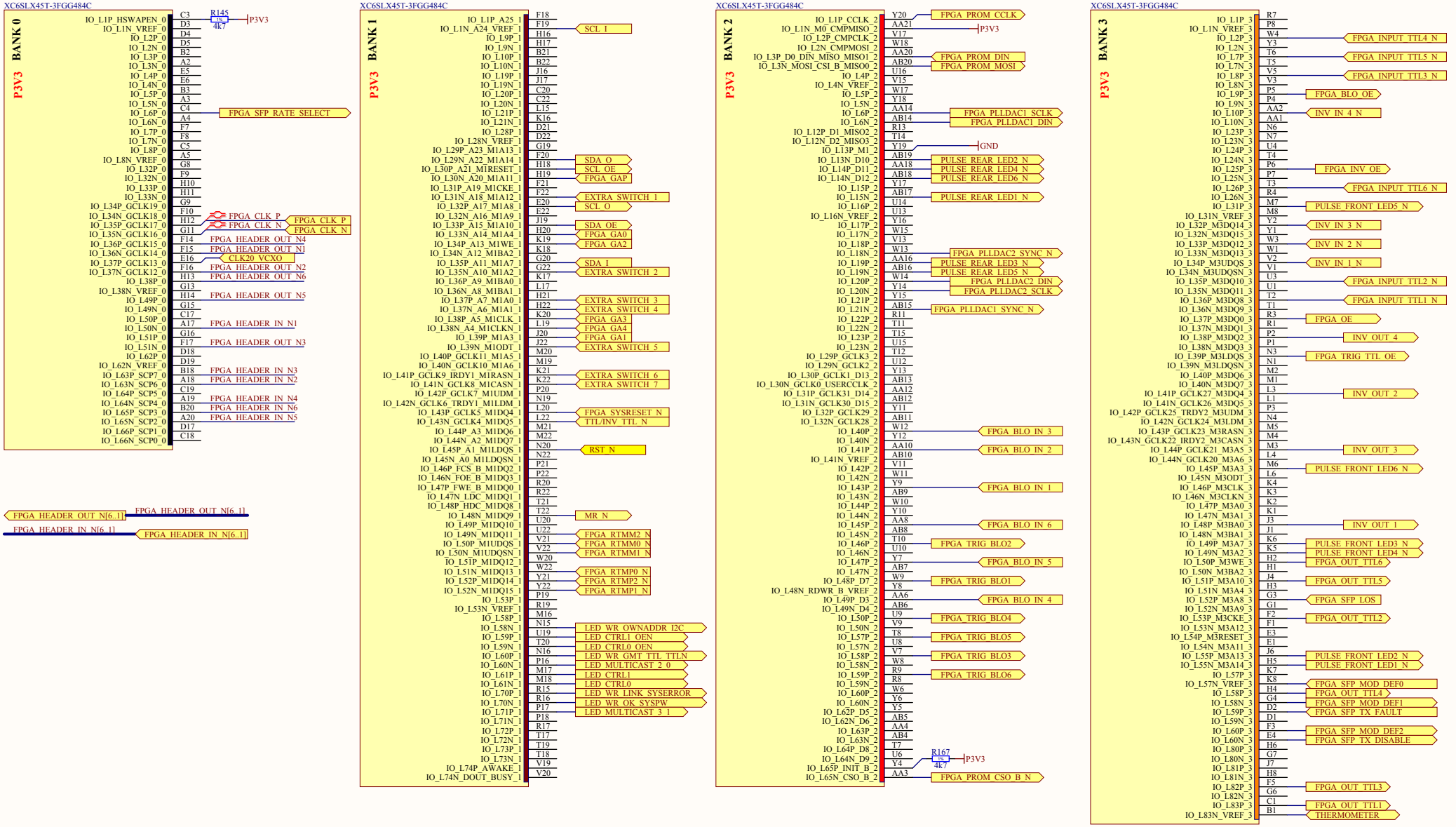
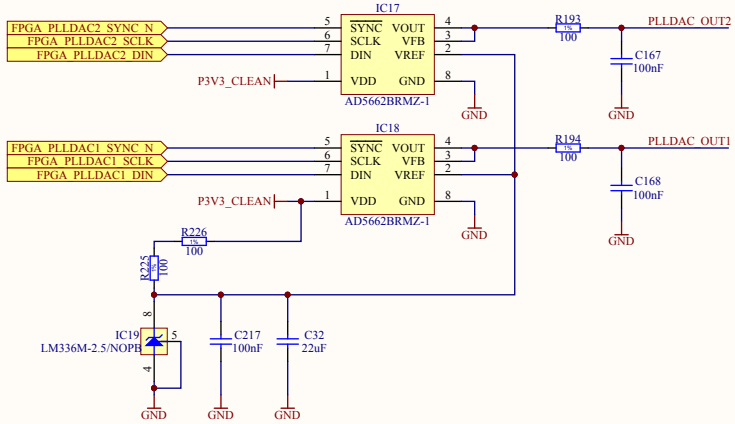
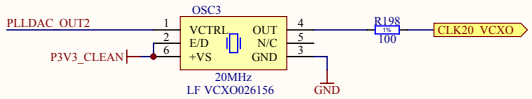
To allow high SerDes ratios, leave all the trigger inputs and outputs in _P pins.

See Xilinx's document UG381, chapter 3 for further information.

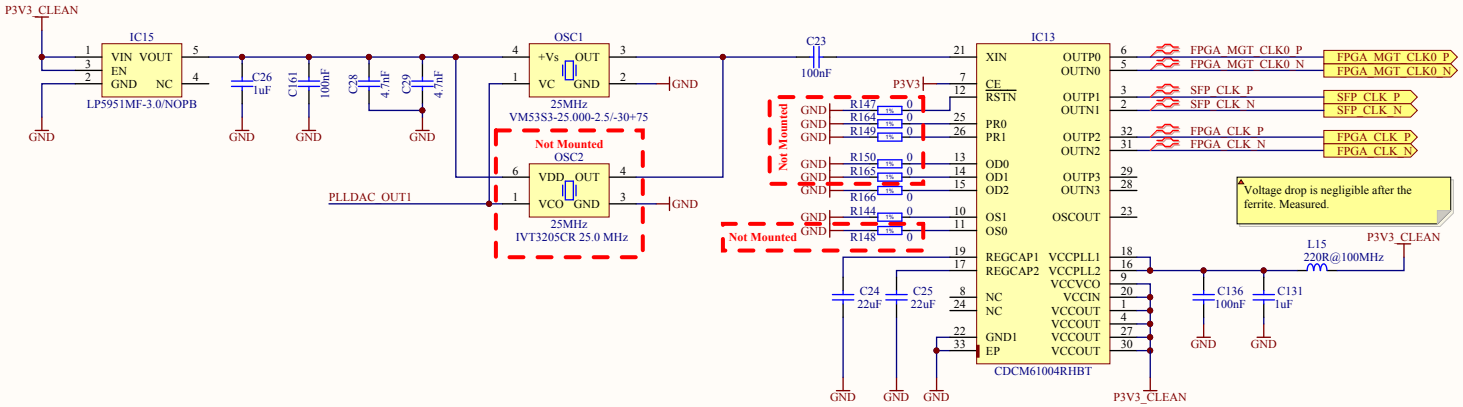


Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo FPGA BANK**	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File FPGAbank.SchDoc	
		Print Date 13/11/2012 08:50:33	Sheet 4 of 14
BE-CO CERN	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3 / Rev 1





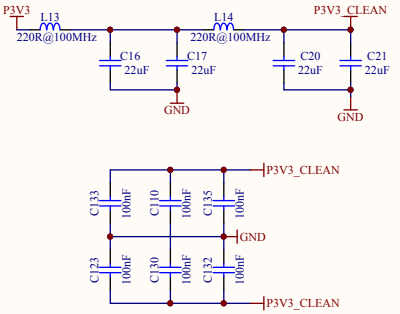
Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).



Voltage drop is negligible after the ferrite. Measured.

CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.

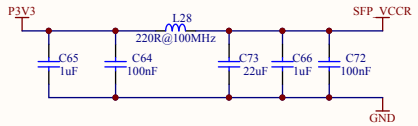
Input = 25 MHz
Output=125 MHz

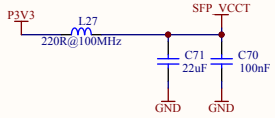


Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo CLOCKS	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File Clocks&Monitor.SchDoc	
		Print Date 13/11/2012 08:50:33	Sheet 5 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

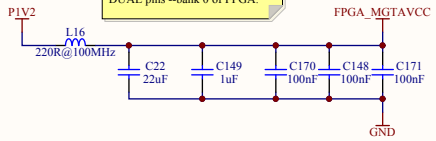
SFP+ module.

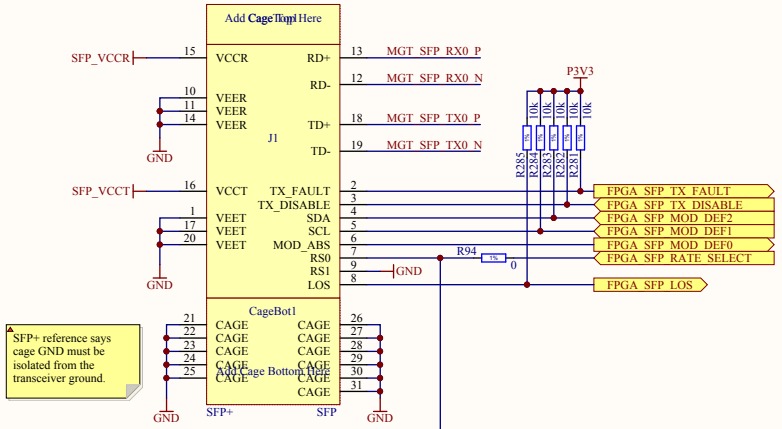
Please refer to "SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+" to full understanding of the capabilities.

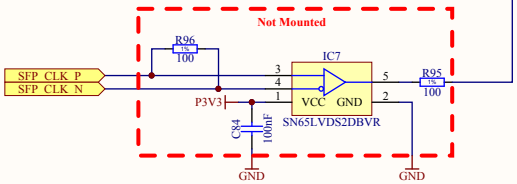




As close as possible to GTP DUAL pins --bank 0 of FPGA.

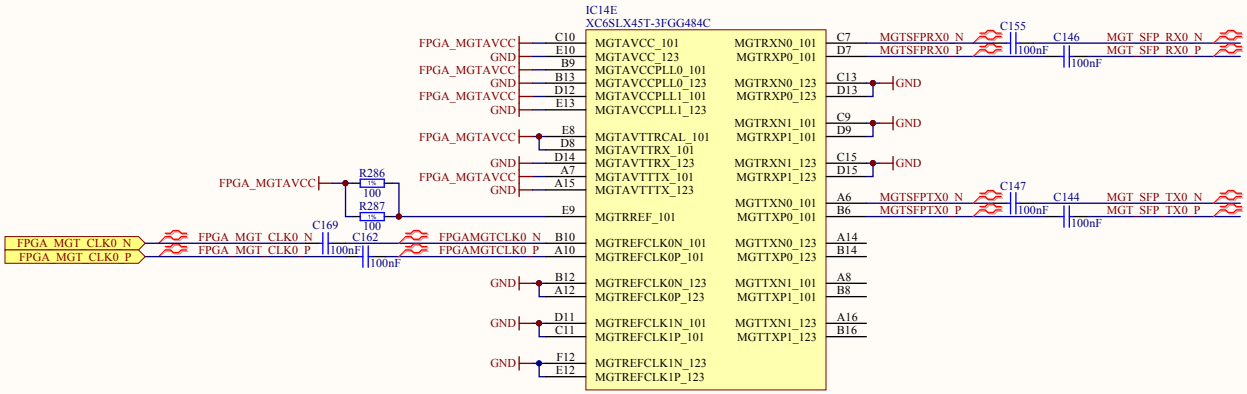






The LVDS receiver can be used to feed a clock to a "custom white rabbit copper SFP".

The trace length from the resistor pins to the FPGA pins MGTRREF and MGTVTTRCAL must be equal in length and geometry



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo MGTX	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File Communication.SchDoc	
		Print Date 13/11/2012 08:50:34	Sheet 6 of 14
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3 / Rev 1

Thermometer will be used to have a FPGA unique ID

P3V3 R126 4k7 THERMOMETER GND IC12 GND DQ VDD °C DS18B20U+ C109 100nF GND

PROGRAM_B must be asserted low for more than 500ns

P3V3 R143 4k7 P3V3 R227 4k7 Not Mounted B7 IC14F XC6SLX45T-3FGG484C DONE_2 PROGRAM_B_2 SUSPEND TCK TDI TDO TMS CMPCS_B_2 AB21 AB2 AA22 A21 E18 G17 D20 V18 R146 100 Not Mounted PB1 C15 22uF GND GND GND FPGA_DONE JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS

Added external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433

IC14I XC6SLX45T-3FGG484C NC U17 NC P15 NC T16

P3V3 P3V3 R107 4k7 R108 4k7 J13 JTAG_TMS JTAG_TCK JTAG_TDO JTAG_TDI GND

Not Mounted J12 GND HEADER_IN1 HEADER_OUT1 HEADER_IN2 HEADER_OUT2 HEADER_IN3 HEADER_OUT3 HEADER_IN4 HEADER_OUT4 HEADER_IN5 HEADER_OUT5 HEADER_IN6 HEADER_OUT6 GND P3V3

TTL/INV_TTL_N

This is used to determine the level of the input trigger connector

P3V3 R163 4k7 R174 4k7 R175 4k7 R188 4k7 R189 4k7 R190 4k7 R191 4k7 R192 4k7 EXTRA_SWITCH_4 EXTRA_SWITCH_3 EXTRA_SWITCH_2 EXTRA_SWITCH_1 EXTRA_SWITCH_5 EXTRA_SWITCH_6 EXTRA_SWITCH_7 TTL/INV_TTL_N SW1 GND

P3V3 R196 4k7 R197 4k7 R230 4k7 R195 4k7 R228 100 R229 100 IC20 D C S W/Vpp HOLD Q VCC VSS M25P32-VMF6P FPGA_PROM_MOSI FPGA_PROM_CCLK FPGA_PROM_CSO_B_N FPGA_PROM_DIN R212 100 R211 100 P3V3 C212 100nF GND GND

FPGA_HEADER_OUT_N[6..1] FPGA_HEADER_OUT_N[6..1]

Not Mounted IC8A FPGA_HEADER_OUT_N4 HEADER_OUT4 IC8B FPGA_HEADER_OUT_N5 HEADER_OUT5 IC8C FPGA_HEADER_OUT_N6 HEADER_OUT6 IC8D FPGA_HEADER_OUT_N3 HEADER_OUT3 IC8E FPGA_HEADER_OUT_N2 HEADER_OUT2 IC8F FPGA_HEADER_OUT_N1 HEADER_OUT1 SN74LVC14AD VCC GND C103 100nF P3V3 GND Not Mounted

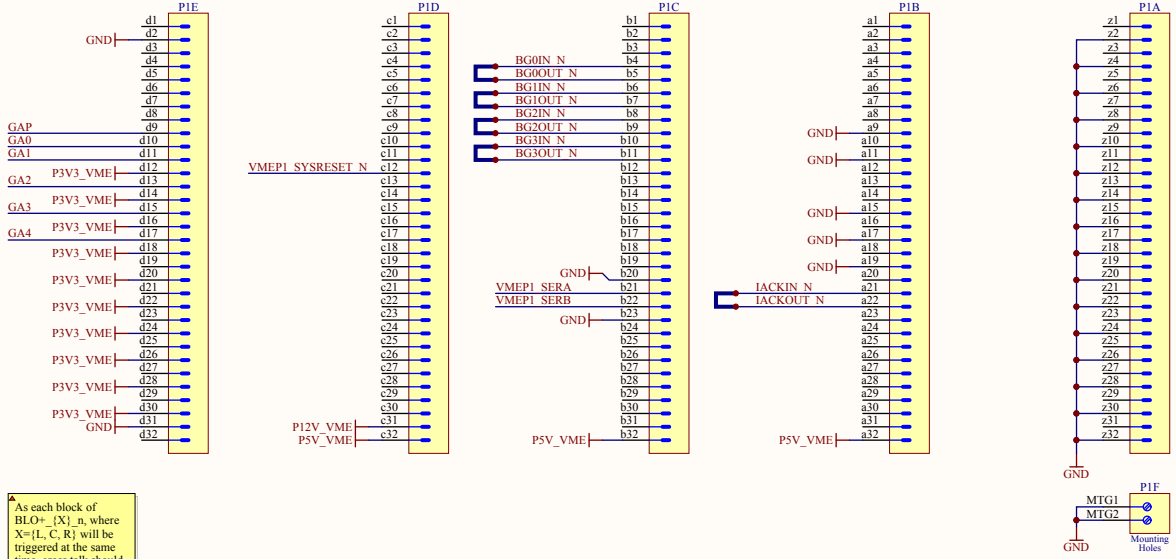
FPGA_HEADER_IN_N[6..1] FPGA_HEADER_IN_N[6..1]

Not Mounted IC9A HEADER_IN1 FPGA_HEADER_IN_N1 IC9B HEADER_IN2 FPGA_HEADER_IN_N2 IC9C HEADER_IN3 FPGA_HEADER_IN_N3 IC9D HEADER_IN6 FPGA_HEADER_IN_N6 IC9E HEADER_IN5 FPGA_HEADER_IN_N5 IC9F HEADER_IN4 FPGA_HEADER_IN_N4 SN74LVC14AD VCC GND C104 100nF P3V3 GND Not Mounted

Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo JTAG	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File JTAG&Button.SchDoc	
		Print Date 13/11/2012 08:50:34	Sheet 7 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1

Utility Bus Signal: see page 199
ANSI/VITA 1-1994

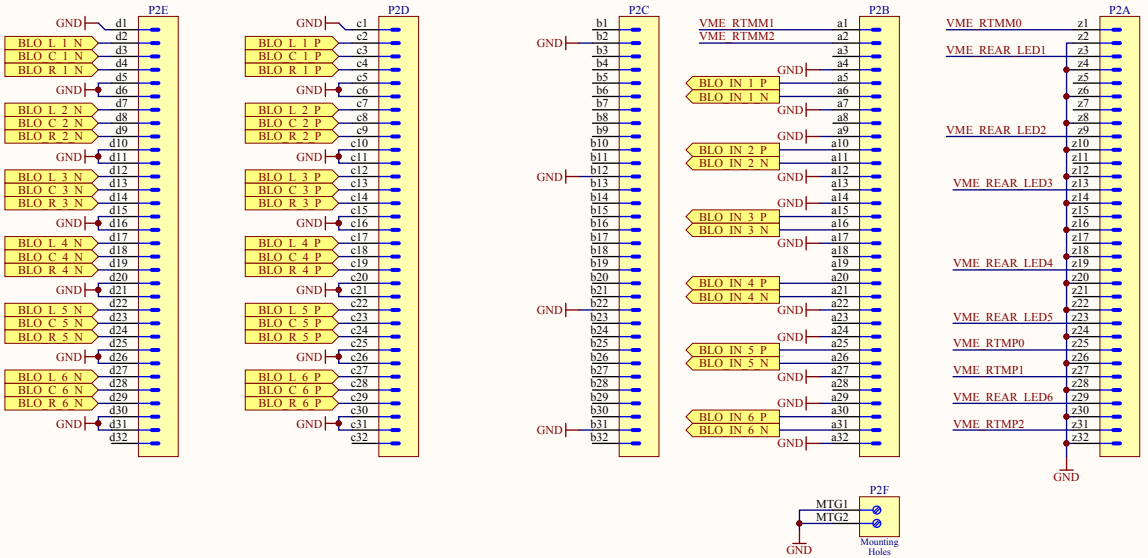
Output configurations in page 230
SYSRESET_N Open collector

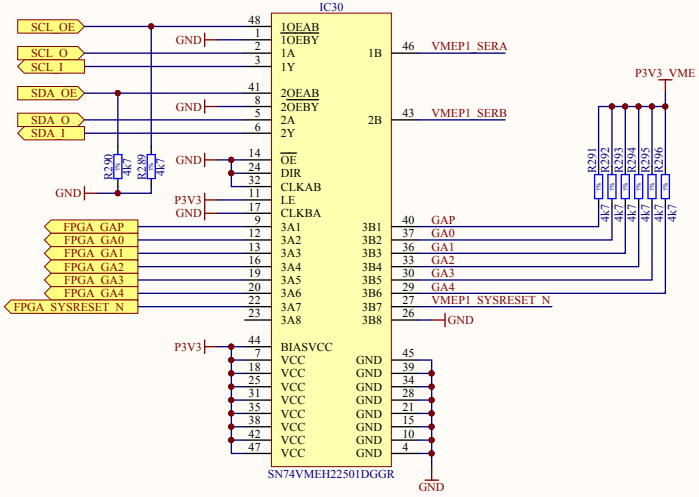


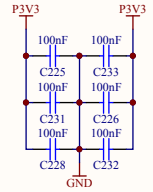
As each block of BLO+_{X}_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical. However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

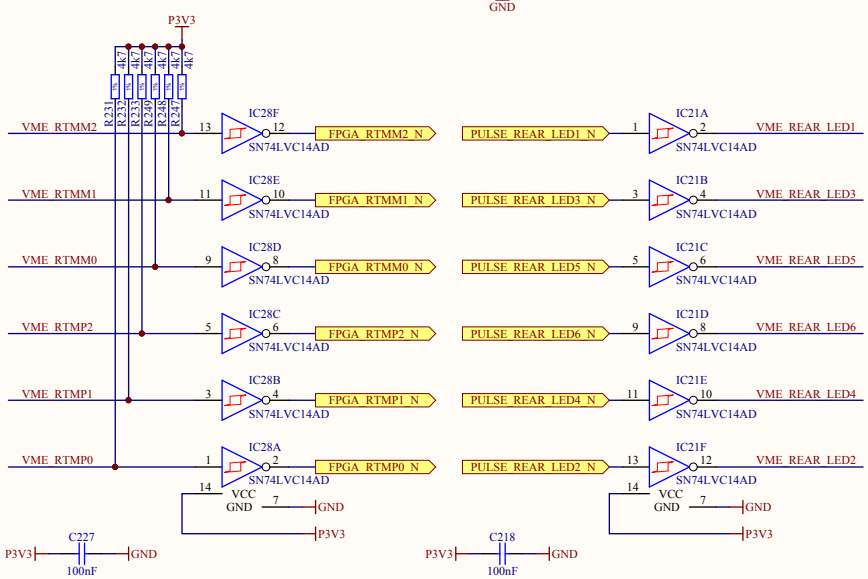
As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo
Signals with more spectral power in higher frequencies should be routed more carefully,so it is better to leave the easiest paths to them.
In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used.
Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

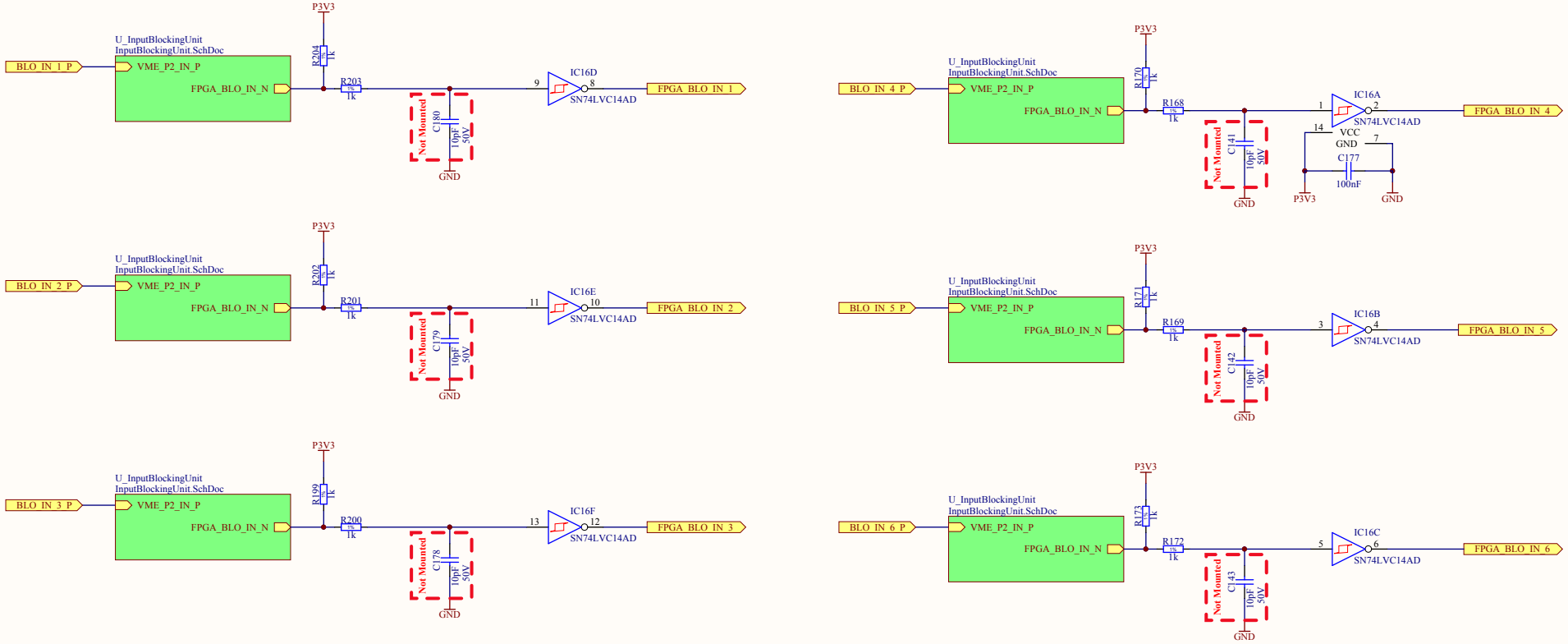




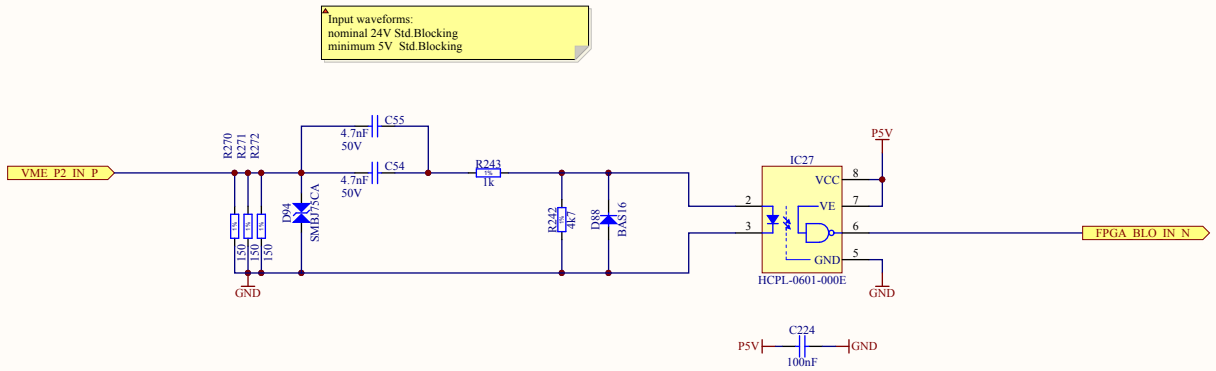




Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo VME64X**	Designer Carlos Gil Soriano	
BE-CO CERN		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File VME64xConn.SchDoc	
		Print Date 13/11/2012 08:50:35	Sheet 8 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT BLO**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File InputBlocking.SchDoc	
		Print Date 13/11/2012 08:50:36	Sheet 9 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
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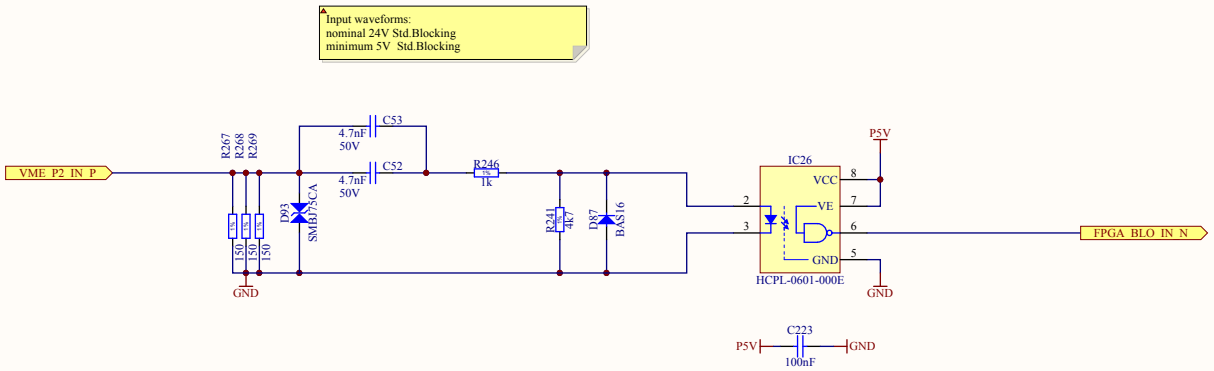
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File InputBlockingUnit.SchDoc	
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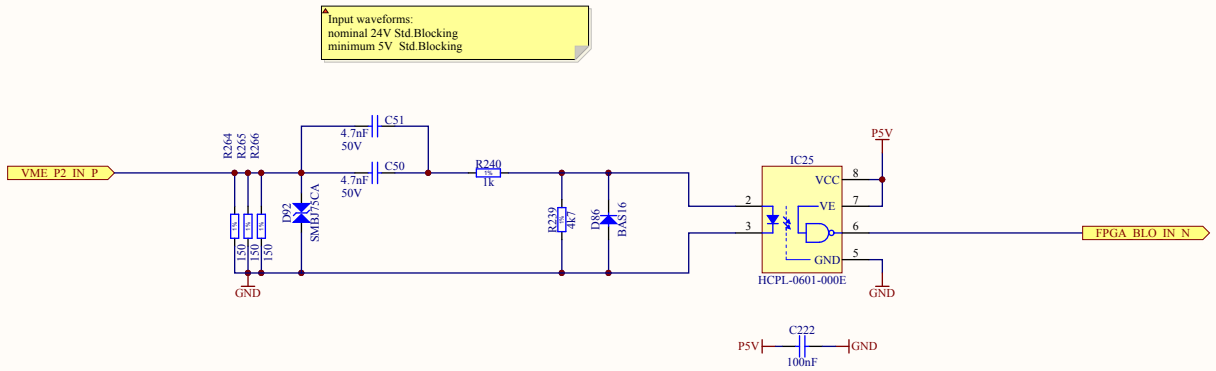
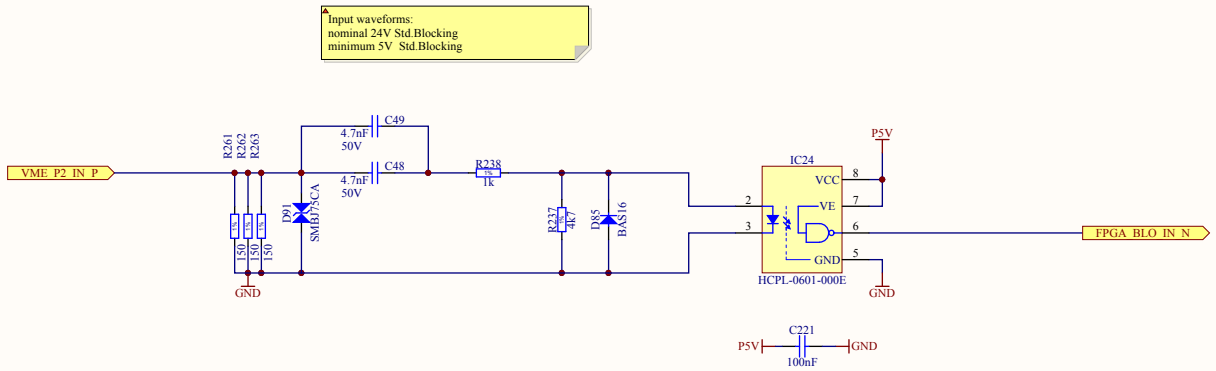
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo INPUT UNIT	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File InputBlockingUnit.SchDoc	
		Print Date 13/11/2012 08:50:37	Sheet 10 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File InputBlockingUnit.SchDoc	
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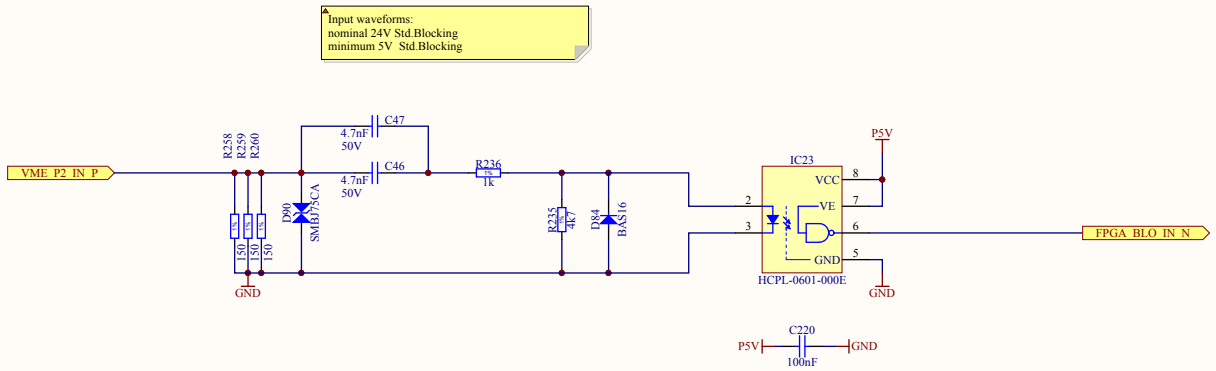
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	Conv-TTL-Blo INPUT UNIT	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
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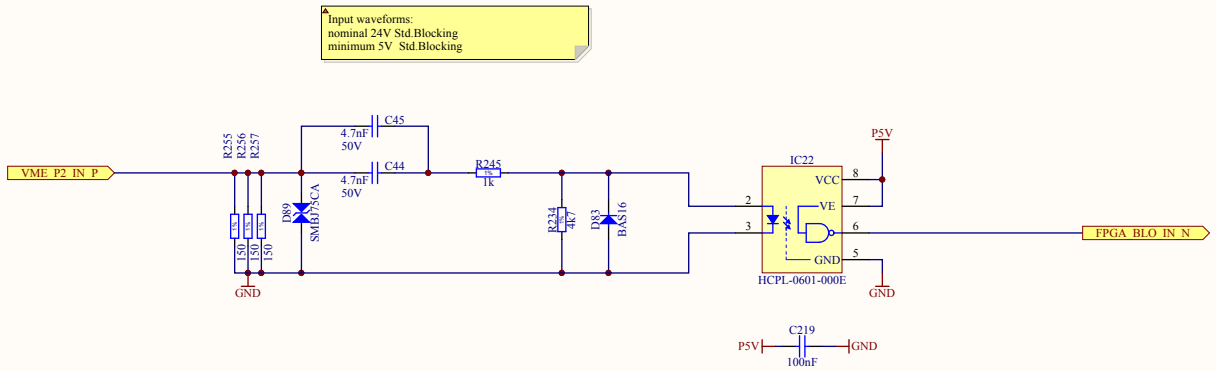
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo INPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File InputBlockingUnit.SchDoc	
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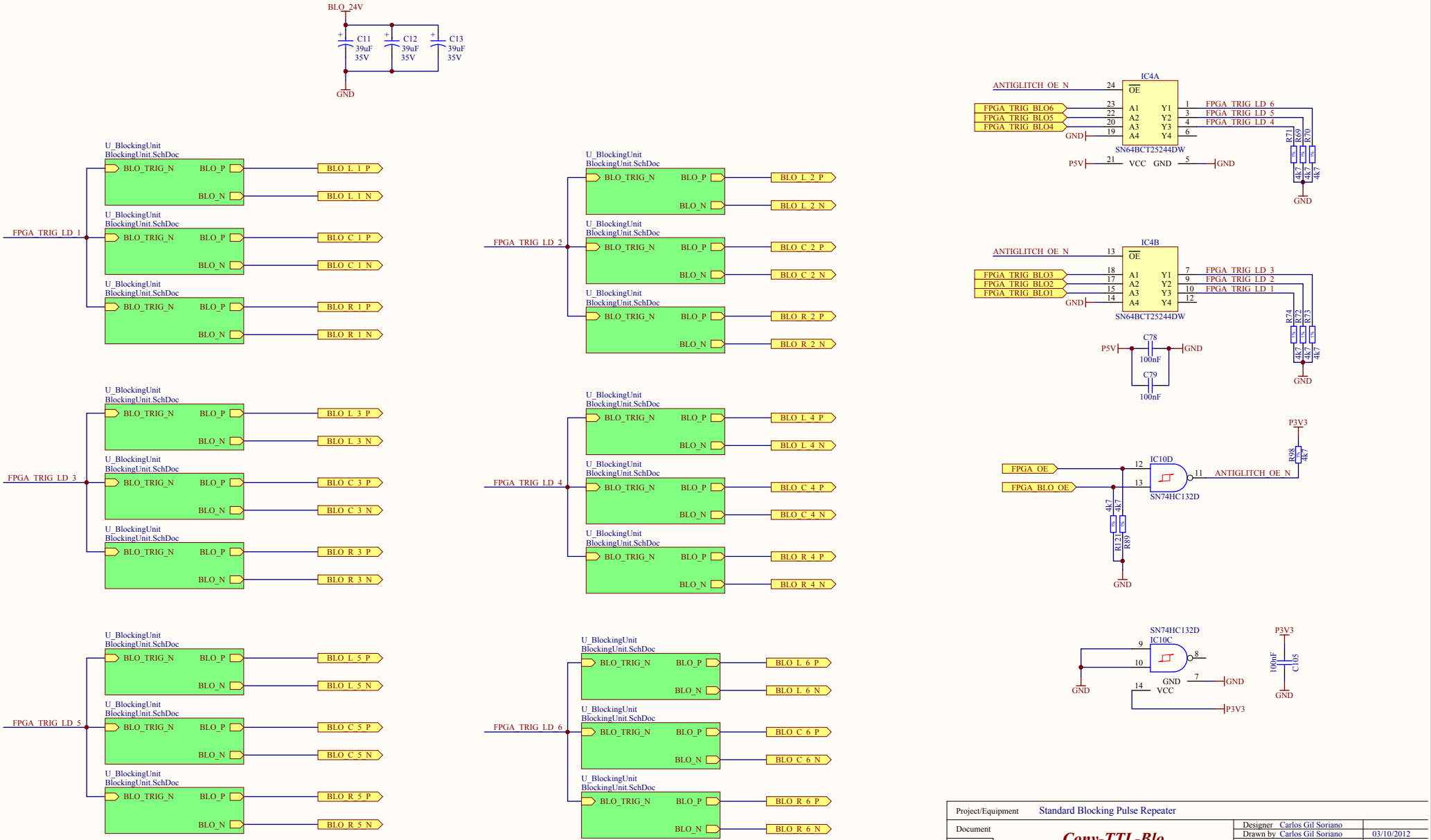
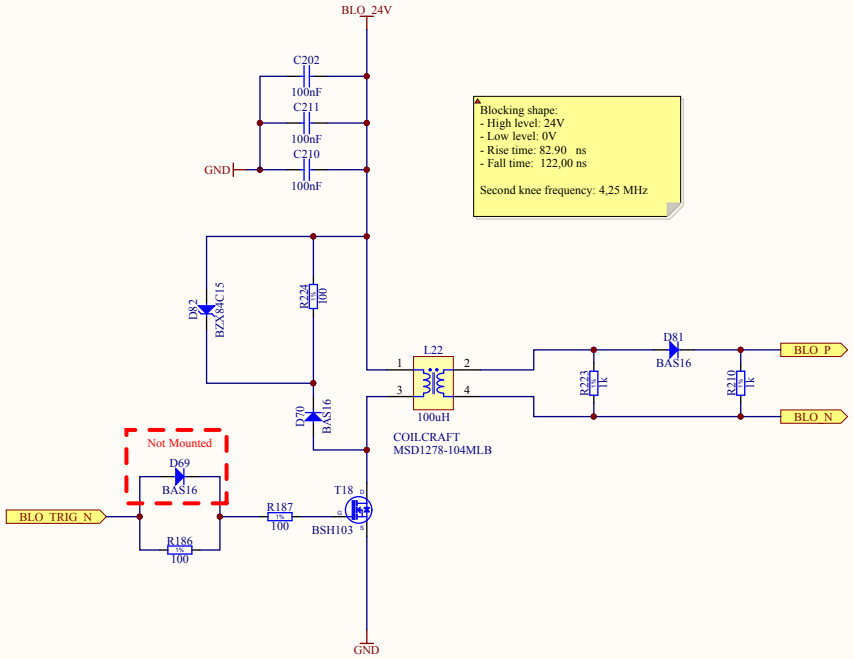
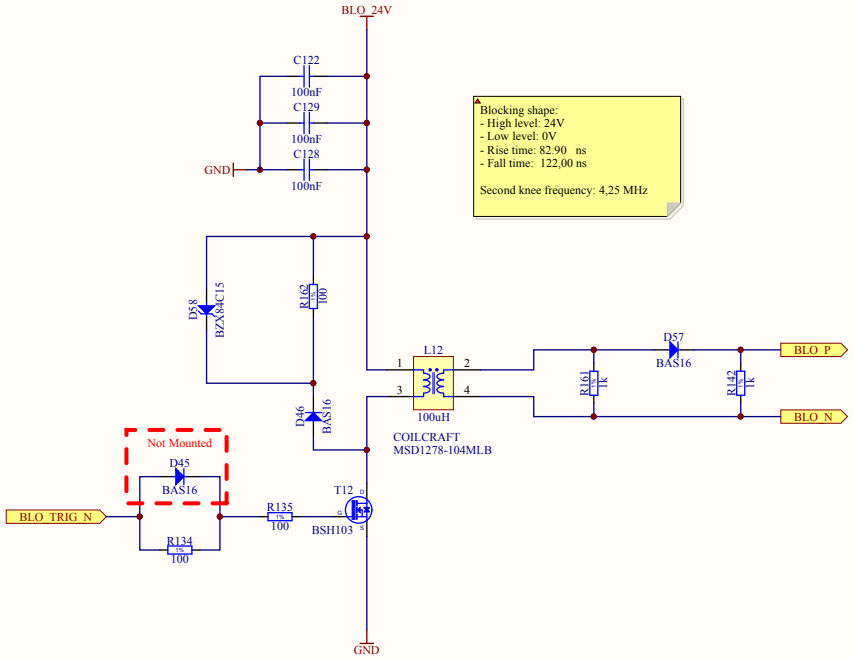
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT BLO**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File BlockingOutput.SchDoc	
		Print Date 13/11/2012 08:50:38	Sheet 11 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
		File BlockingUnit.SchDoc	
		Print Date 13/11/2012 08:50:39	Sheet 12 of 14
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
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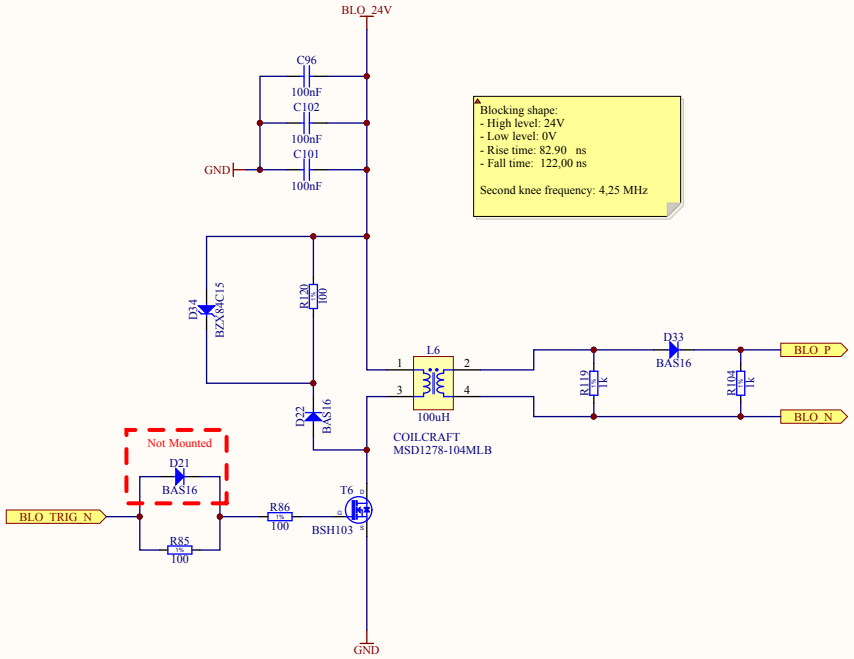

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
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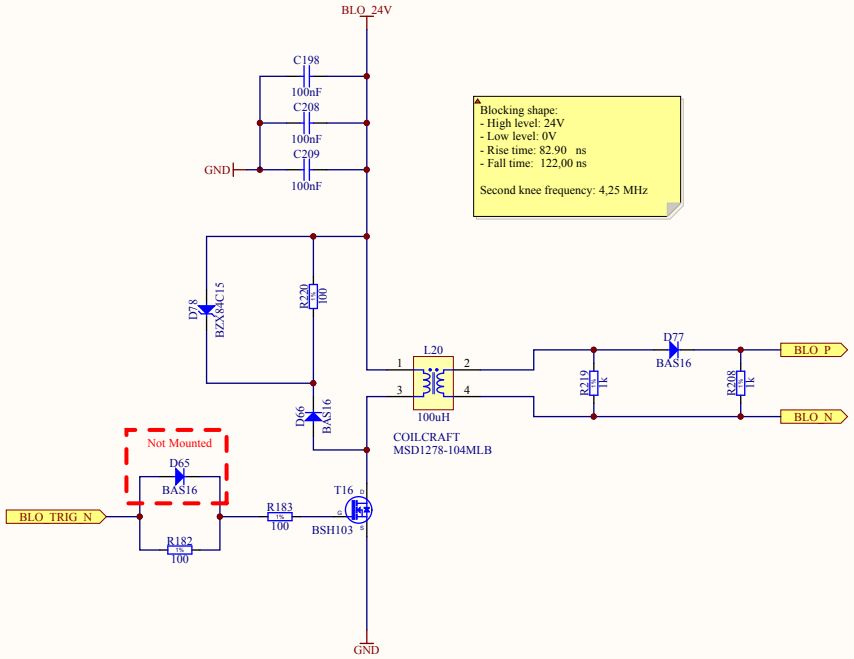

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
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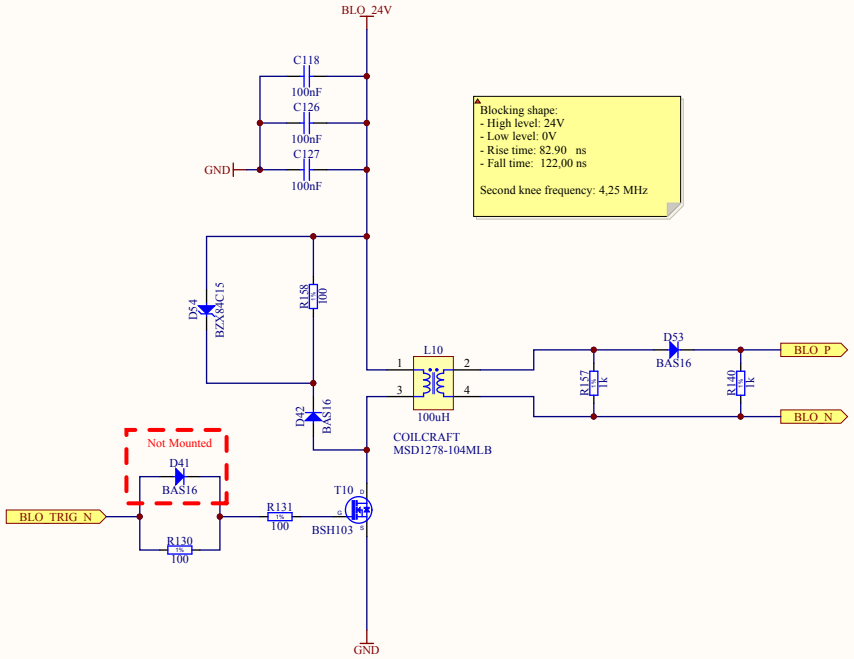

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
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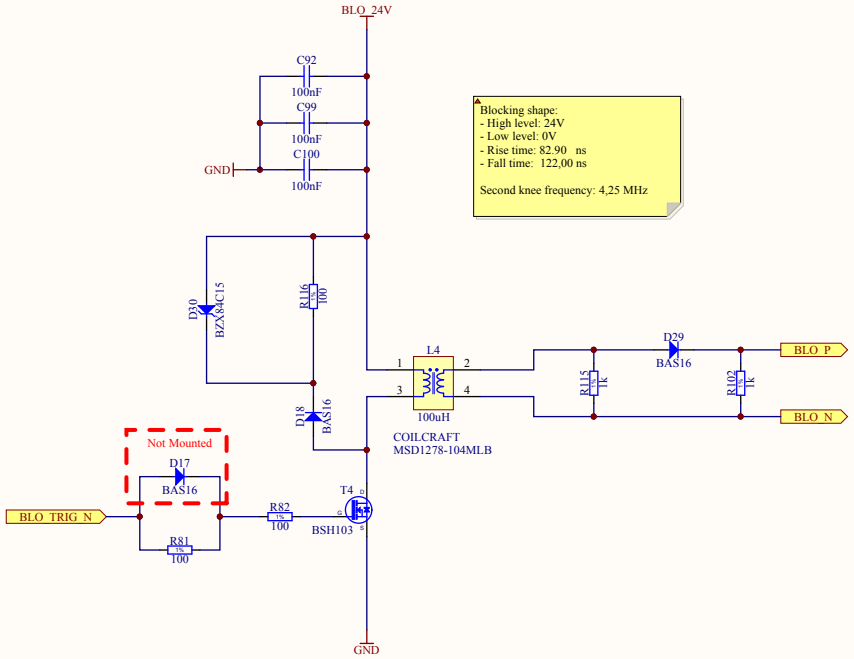
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
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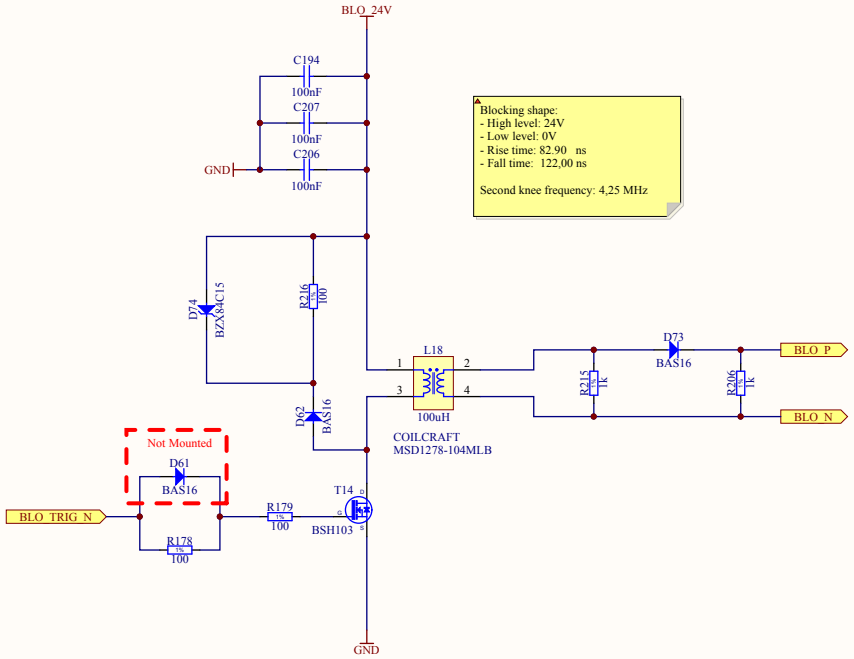

Project/Equipment	Standard Blocking Pulse Repeater		
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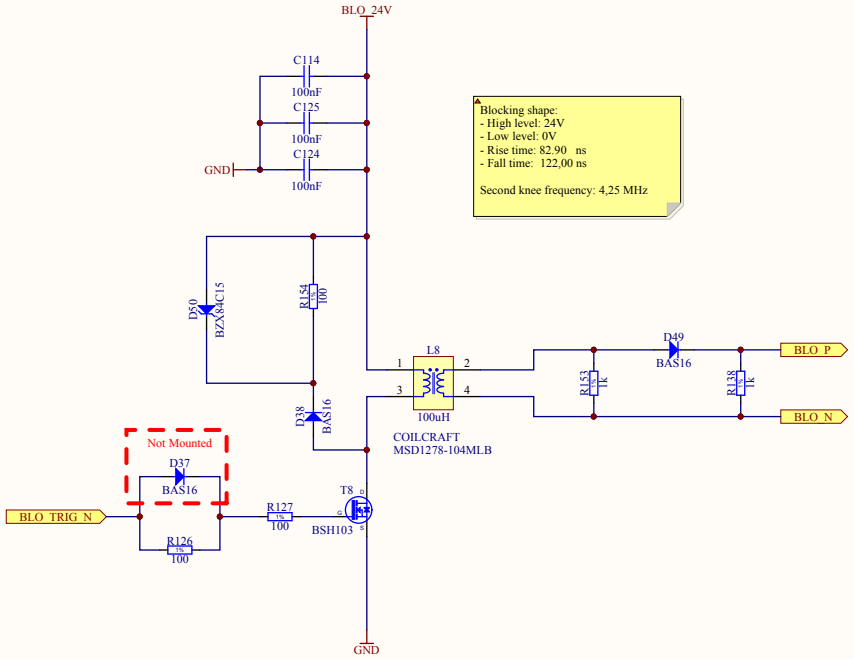

Project/Equipment	Standard Blocking Pulse Repeater		
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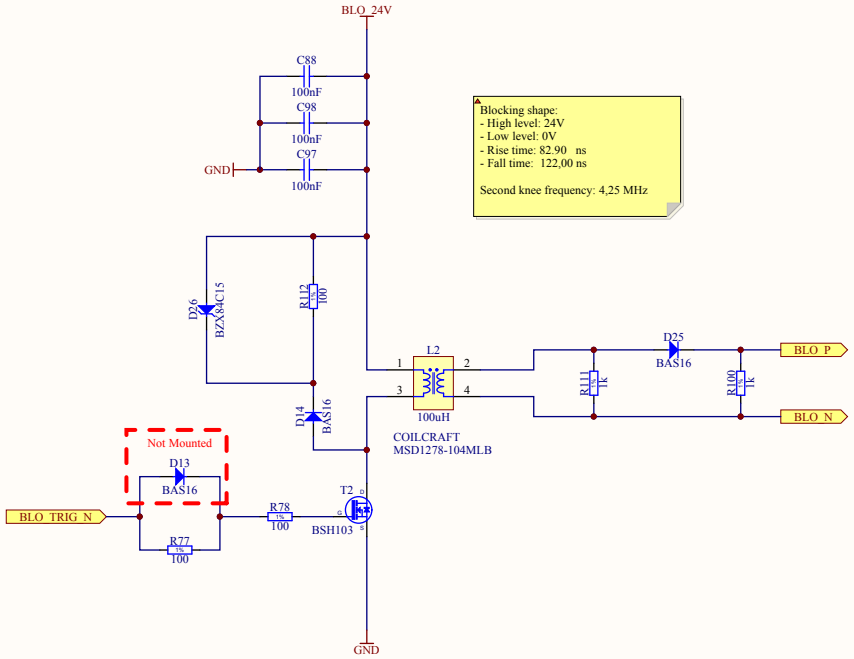

Project/Equipment	Standard Blocking Pulse Repeater		
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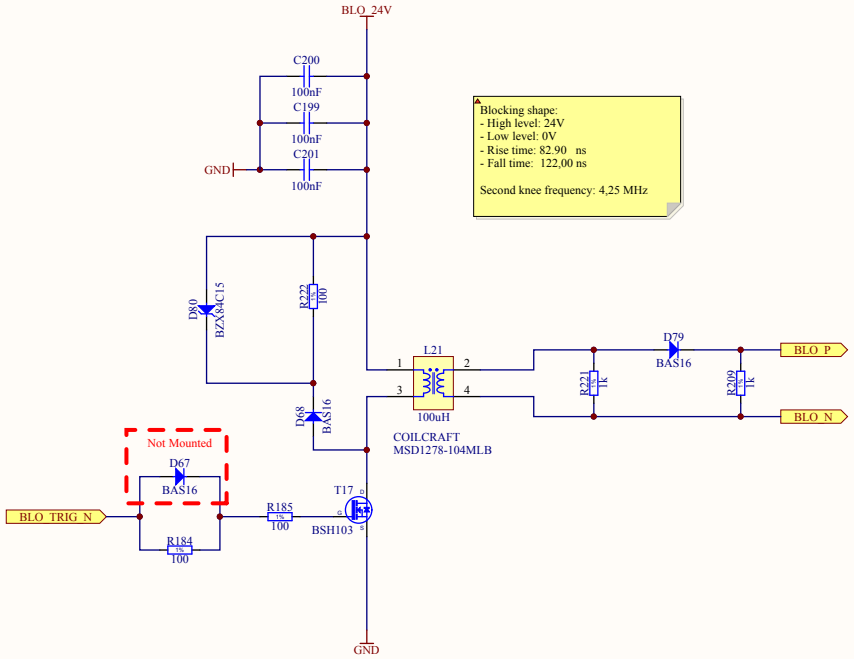

Project/Equipment	Standard Blocking Pulse Repeater		
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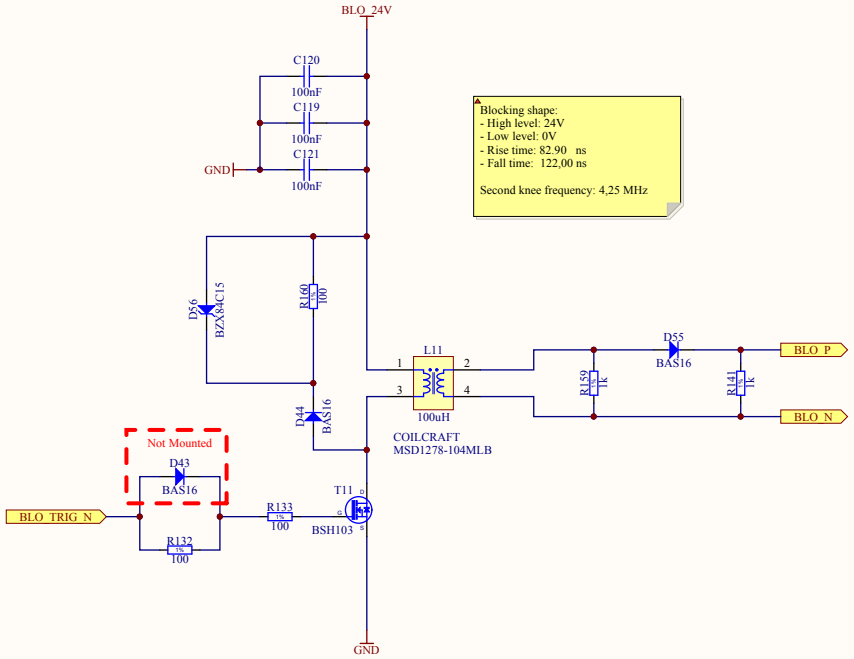

Project/Equipment	Standard Blocking Pulse Repeater		
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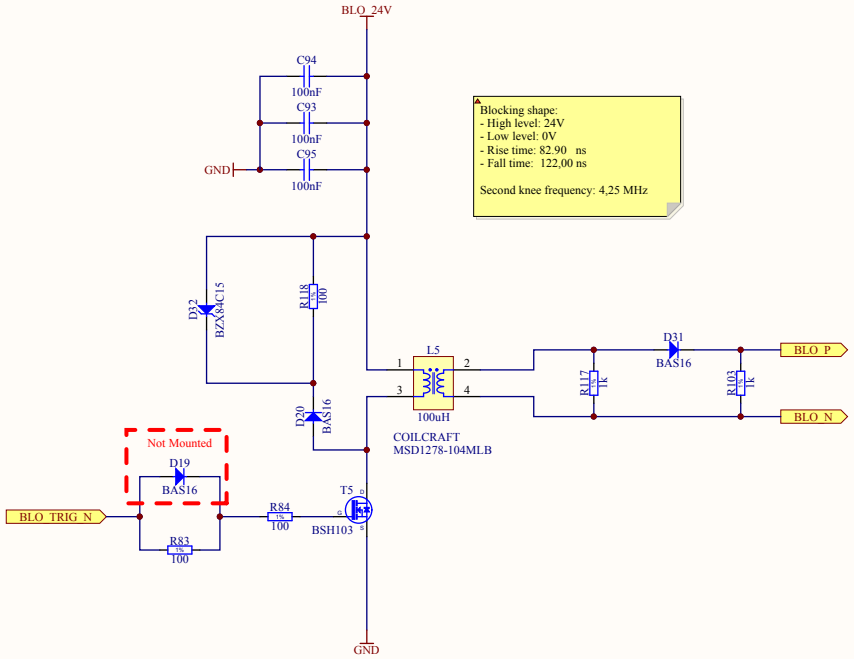

Project/Equipment	Standard Blocking Pulse Repeater		
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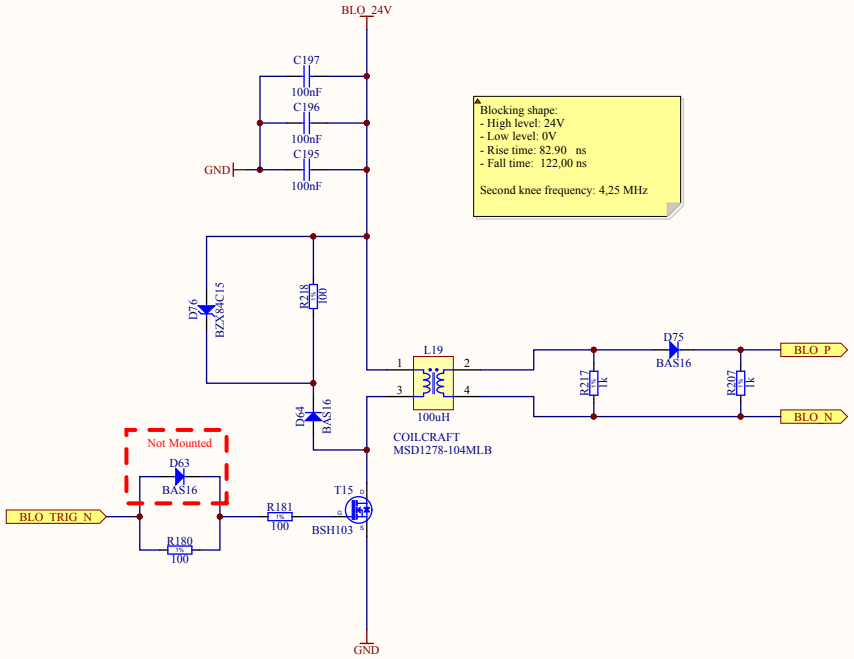

Project/Equipment	Standard Blocking Pulse Repeater		
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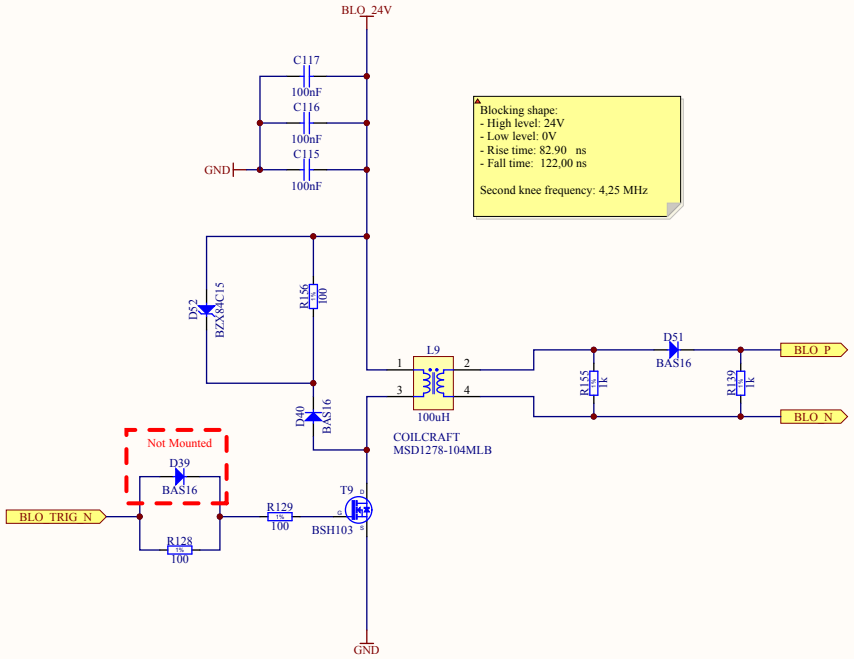

Project/Equipment	Standard Blocking Pulse Repeater		
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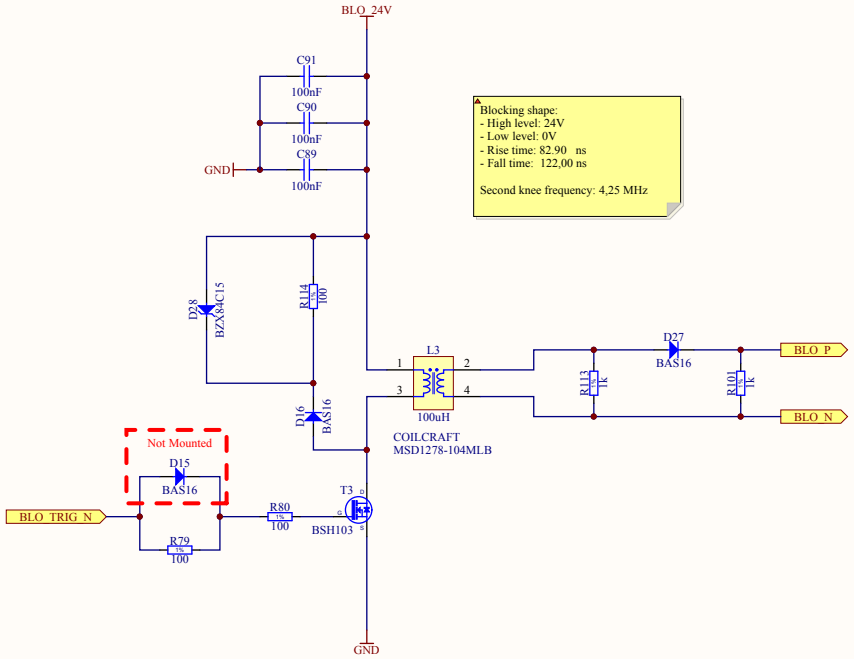

Project/Equipment	Standard Blocking Pulse Repeater		
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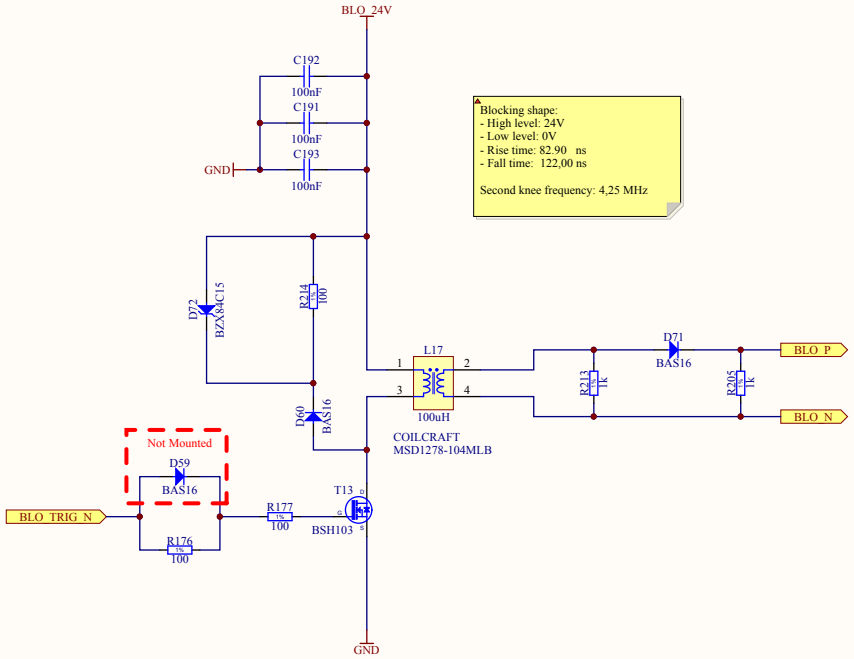

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
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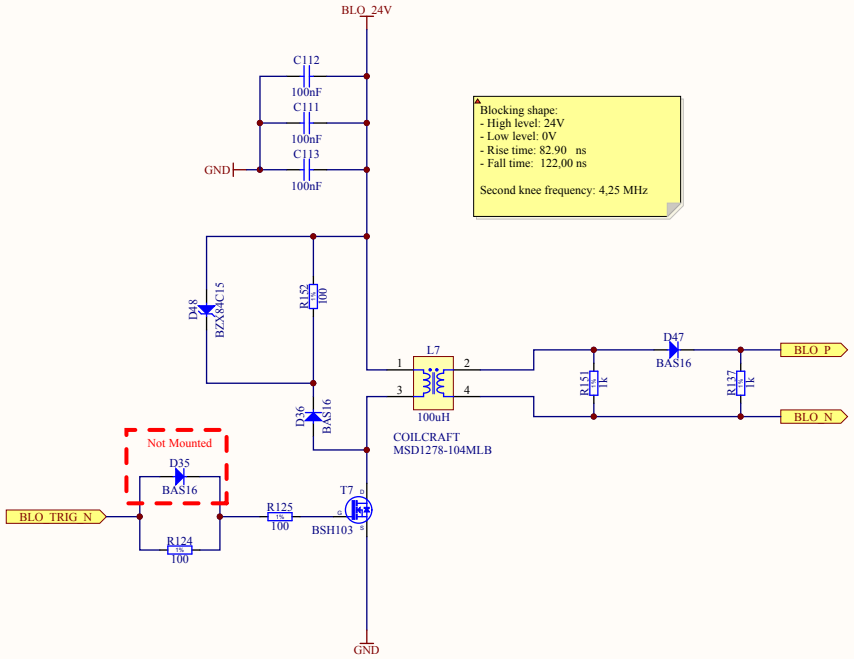

Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
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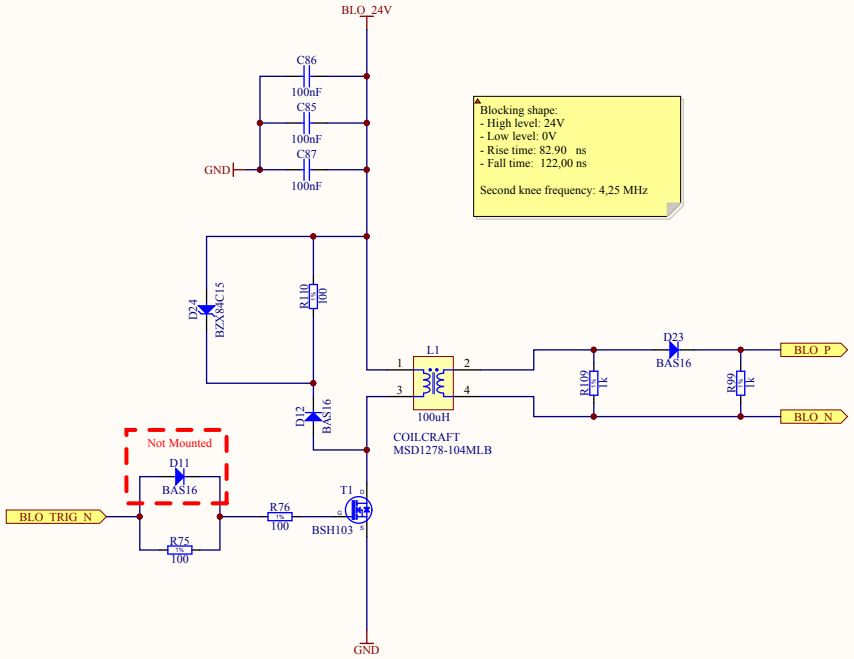
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
Document	**Conv-TTL-Blo OUTPUT UNIT**	Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	03/10/2012
		Check by B.Recordon	13/11/2012
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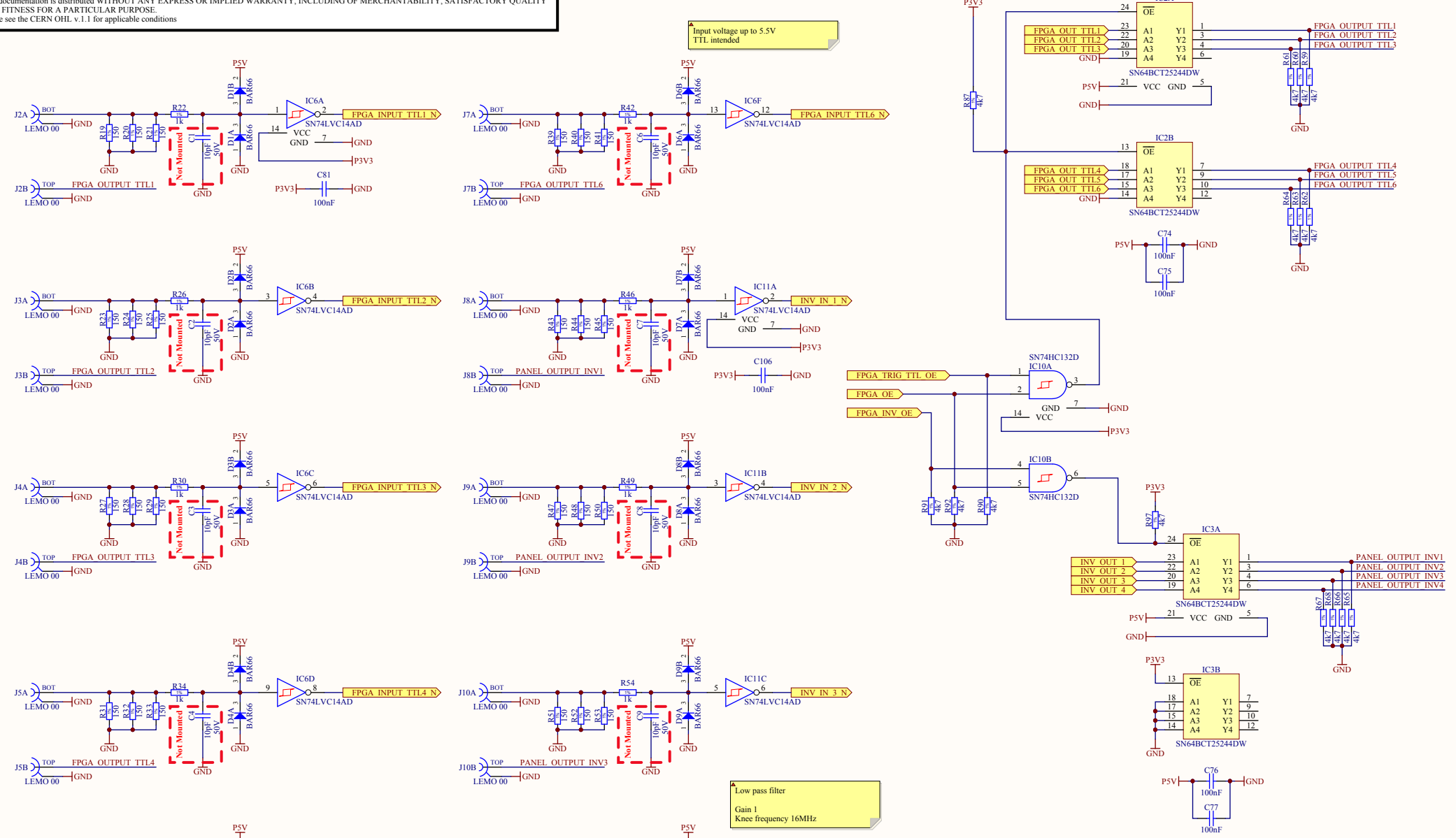
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3	Rev 1



Project/Equipment	Standard Blocking Pulse Repeater		
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		Check by B.Recordon	13/11/2012
		Last Mod. -	13/11/2012
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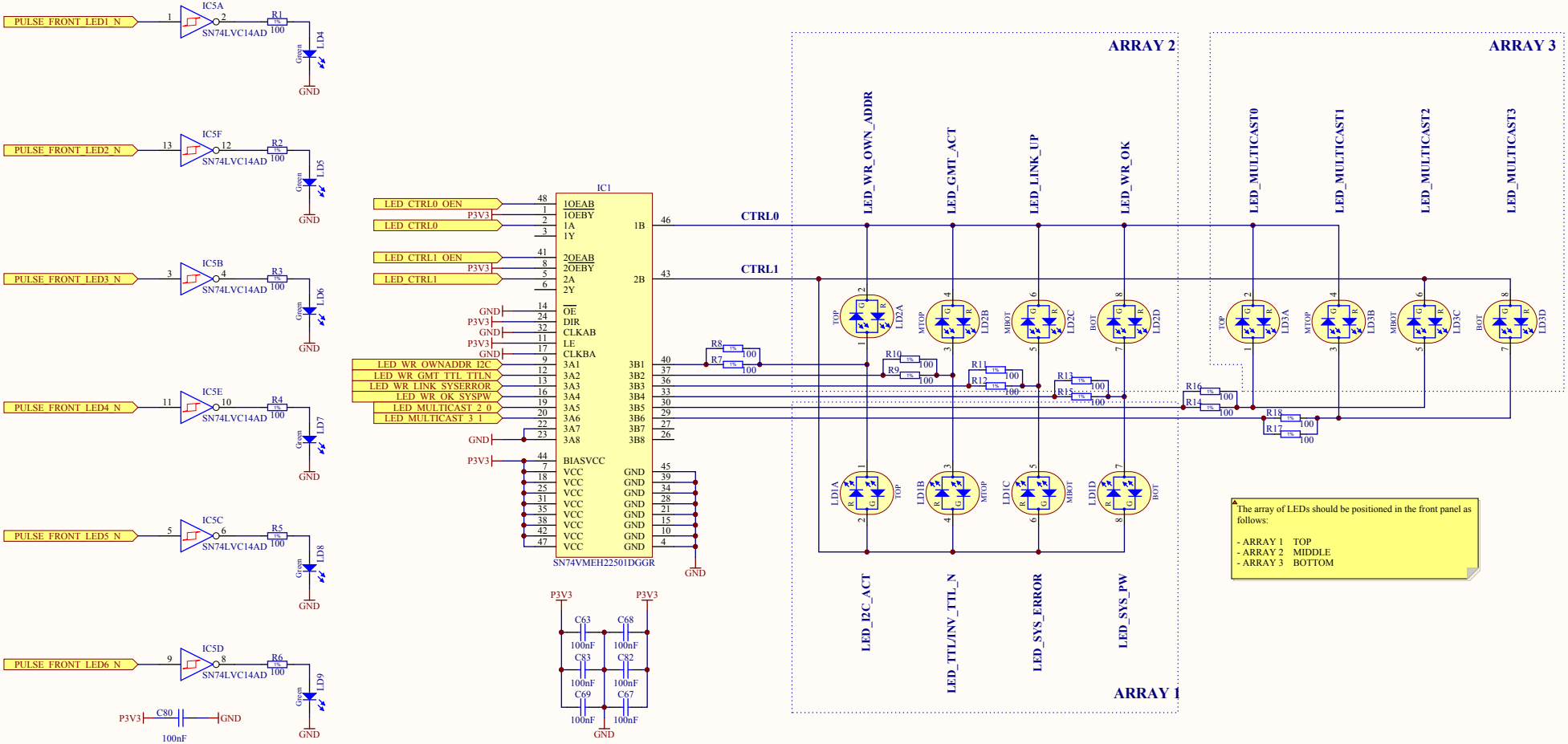
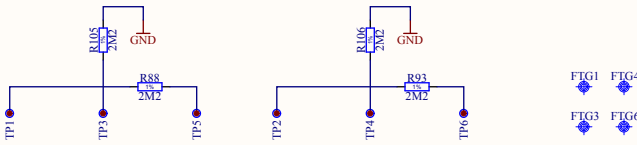
BE-CO CERN	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-02446-V2-0	Size A3 Rev 1



ESD discharge strips (top and bottom of the card)



Project/Equipment	Standard Blocking Pulse Repeater		
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