CONV-TTL-BLO Hardware Guide

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Revision history

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04-07-2013	0.1	First draft
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List of Abbreviations

RTM	Rear-Transition Module
IC	Integrated Circuit
PLL	Phase-Locked Loop
SFP	Small-Form-factor Pluggable (transceiver)

1 Introduction

This document explains in detail the hardware of the TTL to blocking converter system (Figure 1). A full pulse conversion system consists of three distinct boards:

- CONV-TTL-BLO – active front module, containing the circuits necessary to achieve all functionality of the system
- CONV-TTL-RTM – passive rear-transition module (RTM) motherboard, providing the connections from the CONV-TTL-BLO VME P2 connector to the rear panel
- CONV-TTL-RTM-BLO – piggyback board on the RTM, providing the LEMO connectors, pulse LEDs, and the screws to fix the rear panel

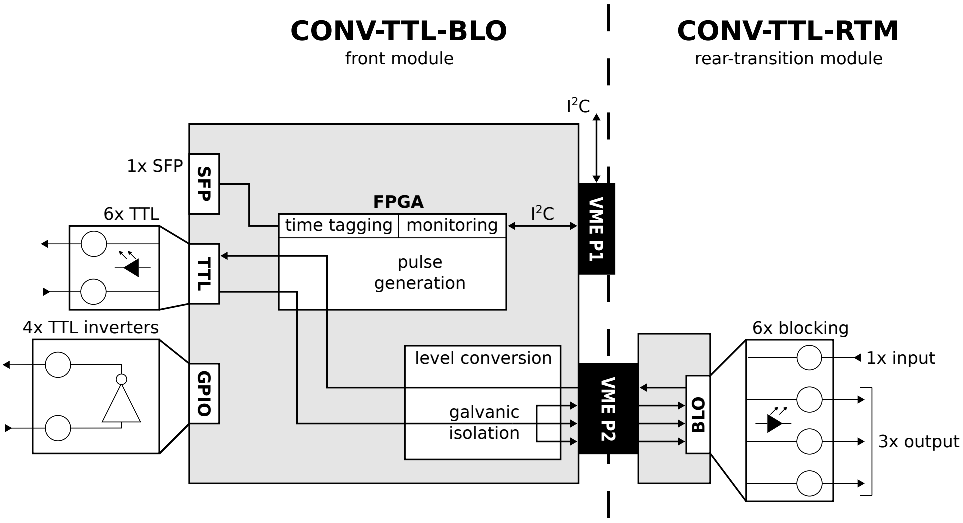

Figure 1: TTL to blocking pulse conversion system

The CONV-TTL-BLO can be used standalone without any RTM, if no blocking pulse replication is needed. This board contains all active circuitry needed to implement the functionalty of the system, from blocking pulse detection and generation, to communication over I^{2}C and time-tagging via White Rabbit [1].

An RTM system usually consists of both motherboard and piggyback and provide the connections to input blocking pulses to the CONV-TTL-BLO.

Additional documentation

- CONV-TTL-BLO User Guide [2]
- CONV-TTL-BLO HDL Guide [3]

2 Front module

A block diagram of the CONV-TTL-BLO front module is shown in Figure 2. The board contains all active circuitry needed within a converter system. The various blocks in Figure 2 are presented in subsections that follow.

The schematics of the CONV-TTL-BLO board can be found at [4].

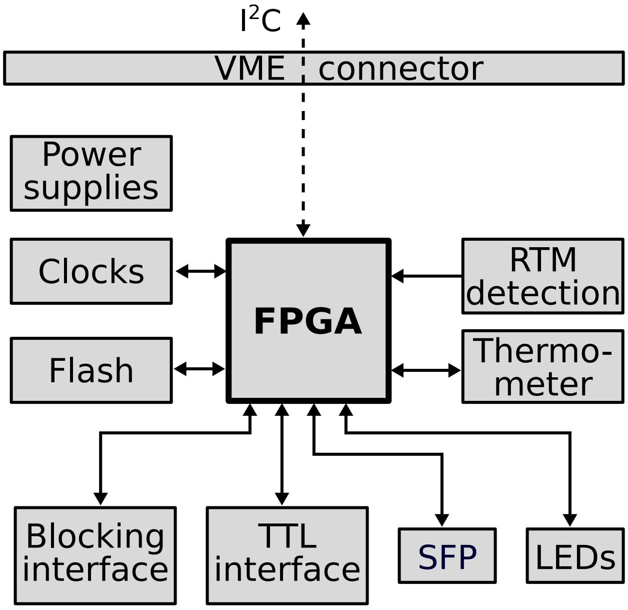

Figure 2: Block diagram of CONV-TTL-BLO board

2.1 VME connector

Schematics: page 8

The VME backplane consists in two connectors, P1 and P2. The following connections provided by the P1 connector are used on the CONV-TTL-BLO:

- the VME power supply pins (3.3 V, 5 V and 12 V)
- *SERCLK* and *SERDAT* pins, for I^{2}C communication

- the geographical addressing pins, also necessary for I^{2}C communication
- the active-low system reset line, connected to the FPGA for resetting the logic implemented therein

Serial communication lines, geographical addressing lines and the system reset line are isolated from the FPGA by means of a Texas Instruments SN74VMEH22501DGGR bus transceiver. Their use is based on the SVEC design [5] and is due to their compatibility to the VME standard.

Apart from the bus grant and IACK lines, which are daisy-chained, the rest of the VME signals are not used on the CONV-TTL-BLO board.

The user-defined part of the P2 connector is used for carrying signals from the CONV-TTL-BLO to the RTM and ultimately the piggyback. The following signals are routed via the VME P2 connector:

- blocking input signals (Section 2.6.1)
- blocking output signals (Section 2.6.2)
- RTM detection and rear panel pulse LED signals (Section 2.9)

2.2 Power supplies

Schematics: pages 2, 3

Various power levels are needed on the CONV-TTL-BLO board. They are listed in Table 1. All power supplies on the board are derived in some way from the 3.3 V, 5 V and 12 V VME power supplies.

Table 1: Voltage levels on CONV-TTL-BLO

Level	Description
1.2 V	Low-voltage power supply for the FPGA logic
3.3 V	V_{CC} for most of the devices on the board
5 V	Power supply for some circuits on-board (blocking input optocouplers, blocking output buffers, etc.)
24 V	Blocking-level power supply

First, the 5 V and 3.3 V VME supplies arriving on the VME connectors are filtered using two PI filters (schematic page 2). These filters assure noise immunity in the 50 MHz to 150 MHz band. The filtered power supplies are used throughout the logic.

The 1.2 V logic power supply is generated by a Texas Instruments TPS54312PWP Buck converter. This circuit can be found in page 2 of the schematics.

Finally, the 24 V blocking power supply (schematics page 3) uses a Texas Instruments TPS40210DGQR boost converter. The values various components around the converter were calculated using the first design example in the datasheet of the device [6].

2.3 Clock circuits

Schematics: page 5

There are multiple clock signals on the CONV-TTL-BLO (Table 2). A 20 MHz clock for the FPGA is generated directly from a tunable VCXO (OSC3). The second FPGA clock is a 125 MHz signal generated from a 25 MHz VCXO by means of a Texas Instruments CDCM61004RHBT PLL IC. Two of the other PLL's output channels are used to output dedicated 125 MHz dedicated clocks to the SFP and FPGA transceiver.

Table 2: Clocks on CONV-TTL-BLO

Clock	**Frequency**	**Description**
CLK20_VCXO	20 MHz	FPGA clock (from VCXO)
FPGA_CLK	125 MHz	FPGA clock (from PLL IC)
SFP_CLK	125 MHz	Dedicated SFP clock
FPGA_MGT_CLK	125 MHz	Dedicated clock for FPGA transceiver

Both VCXOs can be tuned by means of two Analog Devices DACs (IC17 and IC18), that can be controlled by the FPGA via a 3-wire SPI interface.

The 3.3 V power supply used by ICs on the clock generation part is a cleaner version of the board-wide 3.3 V supply. The cleaning is done by a four-pole LC filter.

The design of the clock circuits is based on the SPEC board design [7].

2.4 FPGA

Schematics: page 4

A Xilinx XC6SLX45T Spartan-6 FPGA is present on the CONV-TTL-BLO board. It is the core part of the blocking conversion system, since it is the device controlling all the components on the board.

The intended functionality of the FPGA is:

- generating output pulses as response to input pulse
- pulse logging

- clock conditioning
- remote reprogramming
- controlling the various panel LEDs to inform the user either of pulse arrival, or the status of the system.

For more details on the FPGA firmware and functionality, refer to the CONV-TTL-BLO HDL Guide [3].

2.5 TTL pulse repetition

Schematics: page 13

TTL and TTL-BAR pulses may arrive on front panels of CONV-TTL-BLO boards. The two signal types are described in Sections 4.1 and 4.2 of [2]. Signals arriving on an input channel go through an input stage consisting of Schmitt trigger circuits; they are then input to the FPGA, where the pulse gets regenerated and passed to the output stage.

2.5.1 TTL input stage

The input stage on a TTL pulse channel is shown in Figure 3. Pulses go through a Texas Instruments SN74LVC14AD Schmitt trigger inverter which isolates the FPGA from the channel input. The inverter is 5 V tolerant at the input, so TTL signals may be up to 5 V high. Anything above 5.6 V opens the BAR66 diode to the 5 V and protects the Schmitt trigger.

The input stage is 50 Ω terminated (the three 150 Ω resistors in parallel). Note that when no wire is plugged into the LEMO connector, the termination pulls the line low which becomes a continuous high-level when it comes out of the Schmitt trigger.

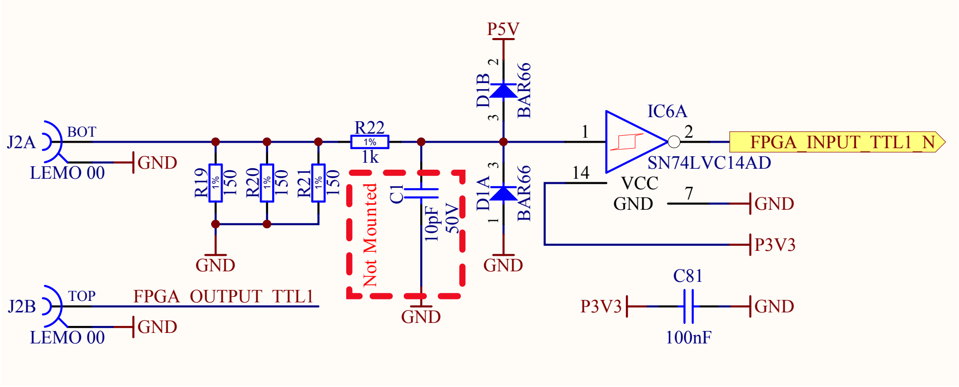

Figure 3: TTL pulse input stage

This input stage is repeated on each of the six TTL pulse replication channels of the CONV-TTL-BLO, as well as the four inverter channels.

2.5.2 TTL output stage

The output stage consists of Texas Instruments SN64BCT25244DW tri-state buffers driven by the FPGA. These buffers assure a high-impedance output on startup and assure the line can drive a 50 Ω load. Pull-down resistors at the output of the tri-state buffers assure a continuous low level at the output when the buffers are not enabled. Combined with the guaranteed tri-state output on startup, these resistors assure a continuous low-level at the output on startup.

The buffers' enable signals are controlled by two signals from the FPGA. These signals are NANDed together (IC10 NAND gate) and connected to the output enable active-low signals. When the FPGA does not drive the output enable line, it is pulled high by a pull-up resistor, to safeguard against spurious signals on the output of the channel.

2.6 Blocking pulse repetition

Schematics: pages 9-12

Blocking pulses arrive through the LEMO connectors on the rear panel. Through the RTM and the P2 connector, they arrive at the blocking input stage on the CONV-TTL-BLO, where an optocoupler is used to isolate the input signal from the logic levels of the FPGA. The input pulse then goes into the FPGA, where the pulse is regenerated in the same manner as TTL pulses. The regenerated pulse signal goes through a flyback converter output stage, where the logic levels of the FPGA are converted back into blocking level.

2.6.1 Blocking input stage

Schematics: pages 9, 10

The blocking input stage (Figure 4) contains the 50 Ω termination, a transient voltage suppressor diode to protect against high-voltage spikes from the RTM, a high-pass RC filter which prevents DC signals from passing to the Avago optocoupler. The optocoupler isolates the blocking-level stage from the logic stage on the FPGA side. Since the optocoupler is powered from 5 V, a Schmitt trigger (not shown in Figure 4) adapts the 5 V level to the 3.3 V level needed by the FPGA.

The minimum pulse level for this circuit is 3.8 V (see Appendix A.1).

The maximum 24 V pulse width that can be safely sustained by the input stage is 3.9 μs with a minimum period of 4.8 μs (see Appendix A.2).

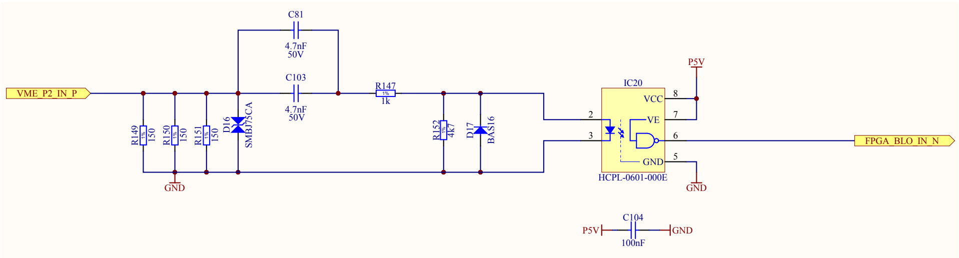

Figure 4: Blocking input stage

2.6.2 Blocking output stage

Schematics: pages 11, 12

The blocking output stage is a flyback converter design with a 1:1 conversion ratio, shown in Figure 5. The core part of the output stage is the flyback transformer assuring galvanic isolation at the output. The transformer is driven straight from the 24 V blocking supply and controlled via the BSH103 power MOSFET. The snubber circuit next to the transformer formed by the BAR66 diode and the Zener diode provides a means to dissipate the energy stored in the leakage inductance of the transformer when the MOSFET is on.

Upstream of the MOSFET's grid pin is a circuit similar to that in the TTL output stage. This circuit is shown in Figure 6. The tri-state buffers' outputs are high-impedance on startup, thus avoidiing spurious signals on blocking outputs. The pull-down resistors at the outputs ensure a low-level signal on the MOSFET's grid on startup.

The tri-state buffers are enabled by means of two signals from the FPGA: the output enable signal common with the TTL output enable, and a separate, blocking output enable signal. These two signals go through the IC10 NAND gate to enable the buffers. When the FPGA does not drive either of these signals, the output enable input of the buffers is kept high via the pull-up resistor.

The maximum pulse frequency that can be sustained without damaging the MOSFET is 210 kHz, with nominal blocking pulse widths of 1.2 μs [8].

Note that if the FPGA is improperly configured, a DC high-level signal on the power MOSFET's grid pin will yield a too high current passing through the MOSFET, which will lead to its failure. Make sure the FPGA pins driving the blocking output stage are properly configured to drive time-limited pulses or a DC low-level at the power MOSFET's grid, or that the blocking output enable signal from the FPGA is low, so as to keep the outputs of the tri-state buffers in high-impedance.

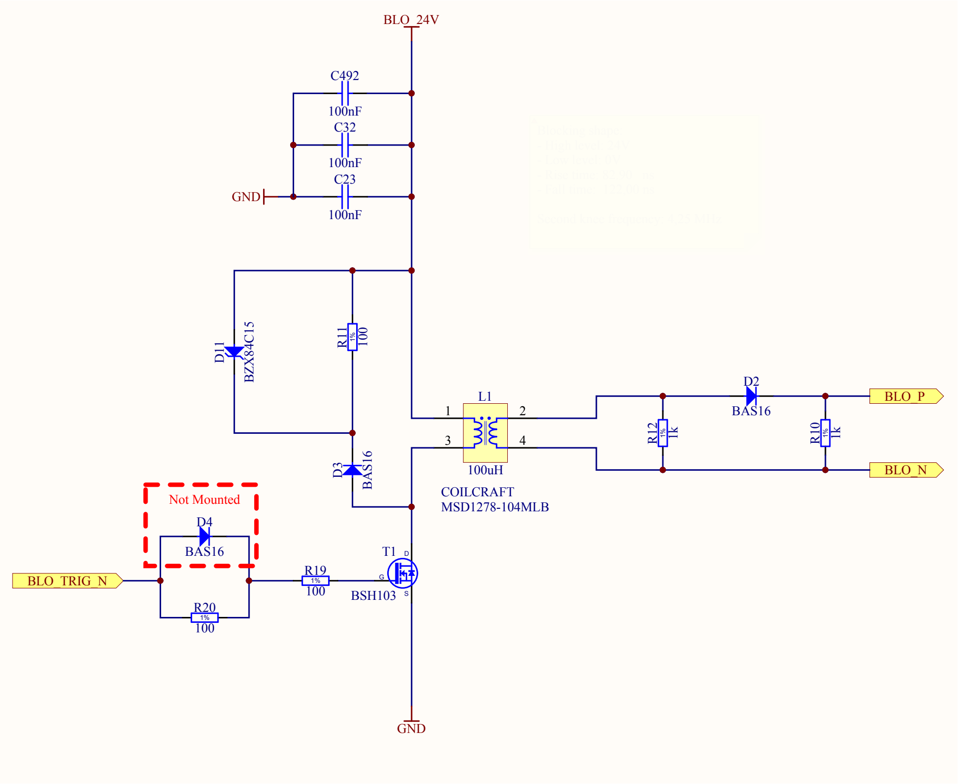

Figure 5: Blocking output stage

2.7 SFP connector

Schematics: page 6

The small form-factor pluggable (SFP) connector on the CONV-TTL-BLO front panel can be used to input an optic fiber cable that may be used for pulse time-tagging using White Rabbit.

2.8 Thermometer and flash chip

Schematics: page 7

A DS18B20U+ thermometer chip is provided on board. This chip can be used to provide a unique ID for the board and measure on-board temperature. It communicates to the FPGA via a Dallas one-wire interface and is powered from 3.3 V.

The Flash chip on-board is used to store FPGA configuration data. It is a Micron M25P32 SPI Flash memory chip with 32 Mbits storage capability.

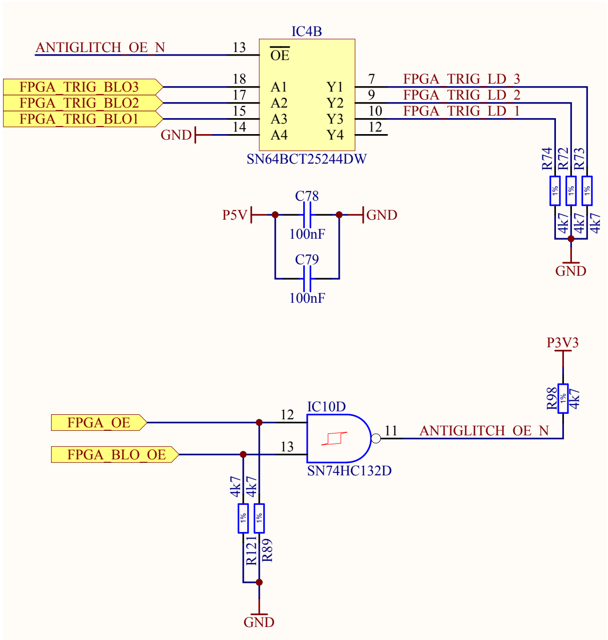

Figure 6: Blocking output tri-state buffers

2.9 RTM detection

Schematics: page 8

The RTM detection circuitry is shown in Figure 7. It works by connecting the RTM motherboard or piggyback detection lines to ground, based on the motherboard or piggyback used. Lines not connected to ground are pulled up to V$_{CC}$ by the pull-up resistor, which yields a low value after the Schmitt triggers. The outputs of the Schmitt triggers are connected directly to the FPGA inputs.

An up-to-date list of boards and their RTM detection line connections can be found at [9].

2.10 Status and pulse LEDs

Schematics: page 14

The circuit for driving the bicolor status LEDs is based on the SVEC design [5]. It consists of the same Texas Instruments SN74VMEH22501DGGR bus buffer chip used for buffering the VME signals. The control and data lines of the chip are driven by logic within the FPGA, which controls lighting of each of the LEDs. An example of how the LEDs can be driven using the FPGA is given in Section 5 of [3].

TTL (front panel) and blocking (rear panel) pulse LEDs are driven by the

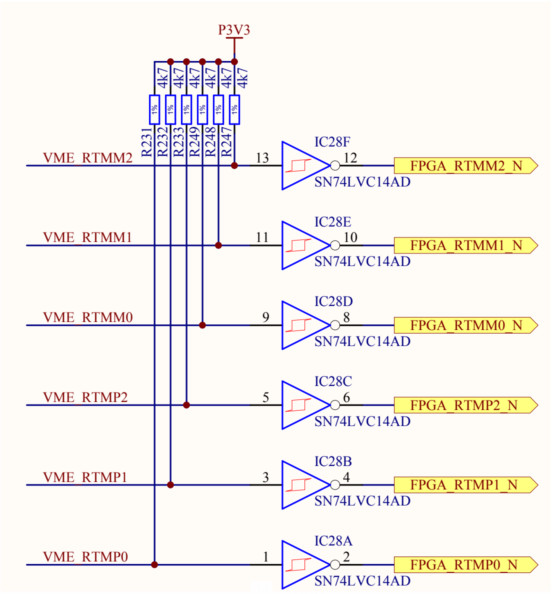

Figure 7: RTM detection circuit

FPGA via a SN7414 Schmitt trigger. In the case of the blocking LEDs, the output of the Schmitt trigger is connected directly to the VME P2 connector and through the RTM to the piggyback, where the current-limiting resistor and the LEDare located.

3 Rear-Transition Module

Rear transition modules (RTMs) are located on the rear side of the VME crate. An RTM in TTL to blocking converter systems is made up of two boards, the motherboard and the piggyback, containing only passive components. The two boards are detailed in the next subsections.

3.1 RTM Motherboard

The CONV-TTL-RTM motherboard [10] is the interface between the VME P2 connector and the RTM piggyback board. It provides a female connector to the VME backplane P2 connector and links the blocking and pulse LED signals from the CONV-TTL-BLO to the piggyback via a 100-pin connector.

RTM motherboards are used in both CONV-TTL-BLO and CONV-TTL-RS485 systems, with different piggybacks.

The motherboard also contains 47 V transient voltage suppressor diodes that inhibit high-voltage pulses arriving on piggyback LEMO connectors.

3.2 RTM Piggyback

The CONV-TTL-RTM-BLO piggyback [11], provides the actual connectors on rear panels of TTL to blocking converter systems. On each of the six blocking channels, there are four LEMO connectors (one input and three outputs) and one LED together with its corresponding current-limiting resistor. The connections for each of the LEMOs and LEDs are made via the 100-pin male connector, through the RTM motherboard, to the CONV-TTL-BLO.

Appendices

A Blocking input stage calculations

Figure 8 shows the blocking input stage, as a reference for the calculations below.

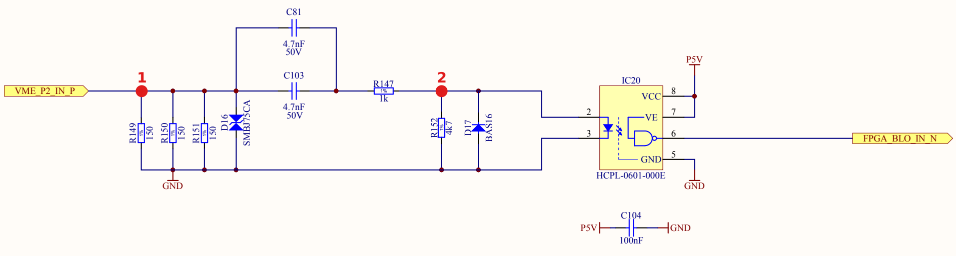

Figure 8: Blocking input stage

A.1 Minimum blocking pulse level

The optocoupler LED has a forward voltage of 1.5 V and therefore when the LED is on, the voltage in point 2 of Figure 8 is

$$V_2 = 1.5V \tag{1}$$

This means that for the LED to turn on, only

$$V_2 = \frac{R_{152}}{R_{152} + R_{147}} V_1 \tag{2}$$

$$V_1 = \frac{R_{152} + R_{147}}{R_{152}} V_2 \tag{3}$$

$$V_1 = \frac{5k7}{4k7} \times 1.5 = 1.82V \tag{4}$$

are needed at the blocking input. However, the LED needs to reach a certain intensity level before it triggers the output of the optocoupler. This translates into a threshold current for the LED, which is given in the optocoupler datasheet [12] to have a typical value of

$$I_{TH} = 2mA \tag{5}$$

Inputting this into the circuit calculation above, and knowing that when the LED is on a 0.31 mA current passes through R_{152} (1.5 V / 4k7 Ω), this yields a current of 2.31 mA passing through R_{147} ($I_{LED} + I_{R_{152}}$). This results in a minimum pulse level of

$$V_1 - V_2 = 2.31mA \times 1k\Omega \tag{6}$$

$$V_{1,min} = 3.8V \tag{7}$$

This value has been verified in practice to be the minimum input pulse level for which a pulse is generated at the output.

A.2 Maximum blocking pulse width calculation

Considering 24 V pulses at the blocking input (point 1 in Figure 8) and the fact that the forward voltage of the LED when conducting is 1.5 V ($V_2 =$ 1.5 V), this yields a 22.5 mA current going through R_{147}

$$I_{R_{147}} = \frac{24 - 1.5}{1k} = 22.5mA \tag{8}$$

Since this current is divided among R_{152} and the optocoupler LED and the current through R_{152} is

$$I_{R_{152}} = \frac{V_2}{R_{152}} = \frac{1.5}{4k7} = 0.31mA \tag{9}$$

the current through the LED is

$$I_{LED} = I_{R_{147}} - I_{R_{152}} \cong 22.2mA \tag{10}$$

Now, by considering the maximum input RMS current of 20 mA obtained from the optocoupler's datasheet [12], and knowing that the RMS current for the pulse wave is

$$I_{LED,RMS} = I_{LED}\sqrt{\delta} \tag{11}$$

this gives a maximum duty cycle of

$$\delta \cong 0.81 \tag{12}$$

With the minimum 4.8 μs pulse period at the output, this gives a maximum input pulse width of

$$t_{p,max} \cong 3.9\mu s \tag{13}$$

References

[1] "White Rabbit." http://www.ohwr.org/projects/white-rabbit.

[2] T.-A. Stana, "CONV-TTL-BLO User Guide." http://www.ohwr.org/documents/263, 06 2013.

[3] T.-A. Stana, "CONV-TTL-BLO HDL Guide." http://www.ohwr.org/documents/290, 07 2013.

[4] "CONV-TTL-BLO Schematics." https://edms.cern.ch/file/1278535/1/EDA-02446-V2-1_sch.pdf.

[5] "Simple VME FMC Carrier (SVEC)." http://www.ohwr.org/projects/svec.

[6] Texas Instruments, "TPS40210, TPS40211, 4.5 V to 52 V Input Current Mode Boost Controller." http://www.ohwr.org/documents/227.

[7] "Simple PCIE FMC Carrier (SPEC)." http://www.ohwr.org/projects/spec.

[8] C. G. Soriano, "Standard Blocking Output Signal Definition for CT-DAH board," Sept. 2011. http://www.ohwr.org/documents/109.

[9] "Rear Transition Module Detection." http://www.ohwr.org/projects/conv-ttl-blo/wiki/RTM_board_detection.

[10] "RTM Motherboard Schematics." https://edms.cern.ch/file/1281435/1/EDA-02452-V2-0_sch.pdf.

[11] "RTM Piggyback Schematics." https://edms.cern.ch/file/1178456/1/EDA-02453-V1-0_sch.pdf.

[12] Avago Technologies, "High CMR, High Speed TTL Compatible Optocouplers." http://www.avagotech.com/docs/AV02-0940EN.