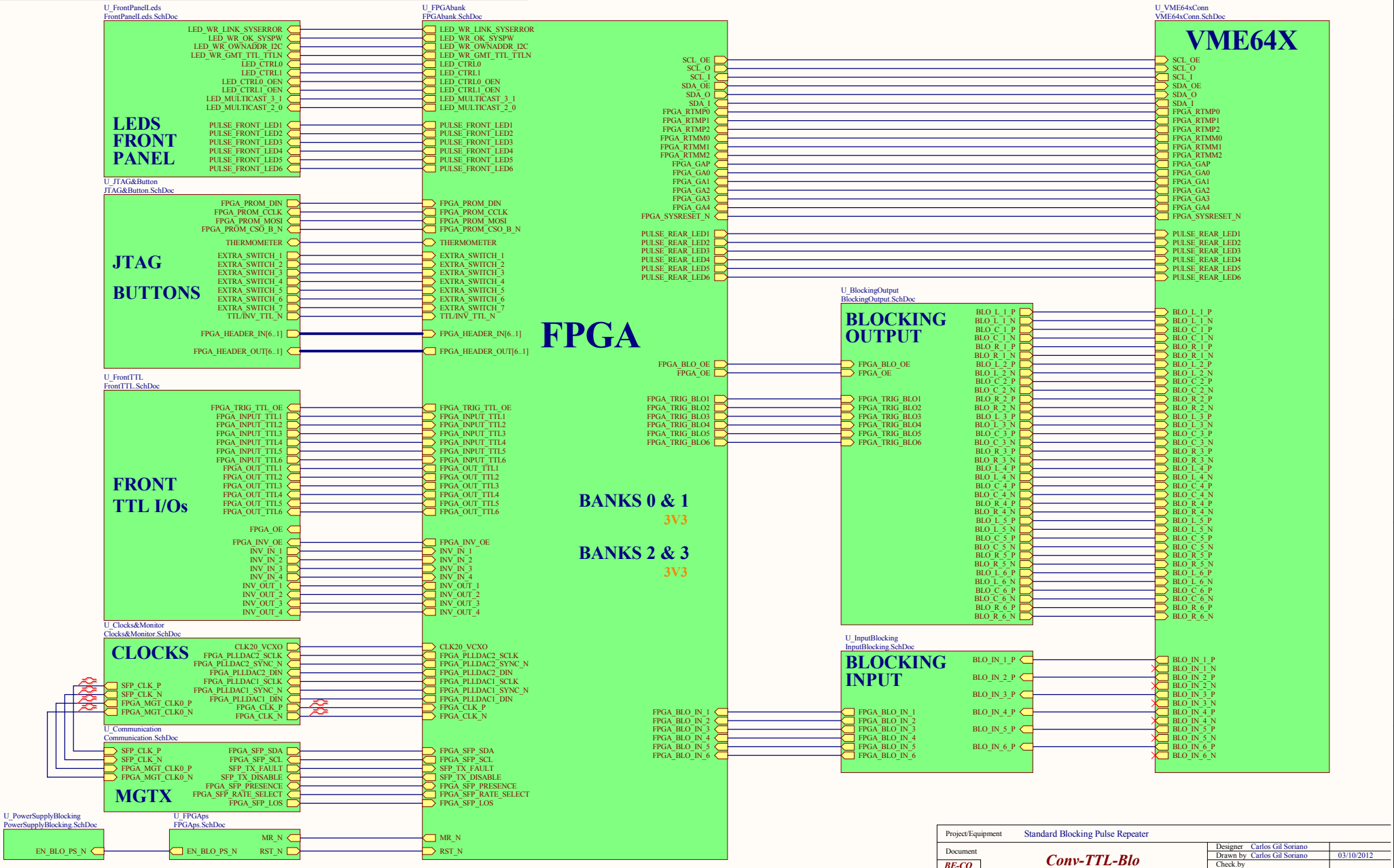



| | |
|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater |
| Document | Conv-TTL-Blo TOP |
| Designer | Carlos Gil Soriano |
| Drawn by | Carlos Gil Soriano 03/10/2012 |
| Check by | |
| Last Mod. | - 03/10/2012 |
| File | ConvTtlBlo_TOP.SchDoc |
| Print Date | 03/10/2012 18:02:10 |
| Sheet | 1 of 14 |
| Size | A3 |
| Rev | 0 |

BE-CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02446-V2-0

Efficiency of 85% and better

IC29 TPS54312PWP

IC30 TPS3808G01DBVT

Capacitor CT not mounted: delay of 570ms

IC11E IC11F SN74LVC14AD

Not Mounted

IC14G IC14H XC6SLX45T-3FGG484C

Voltages are:

| | |
|---|---|
| *** FPGA | |
| VCCO_0 | 3V3 |
| VCCO_1 | 3V3 |
| VCCO_2 | 3V3 |
| VCCO_3 | 3V3 |
| VCCaux | 3V3 |
| VCCint | 1V2 |
| *** PROM | |
| VCCaux | 3V3 |

Test points

Not Mounted

VCCO_int decoupling capacitors

VCCO_0 decoupling capacitors

VCCO_1 decoupling capacitors

VCCO_2 decoupling capacitors

VCCO_3 decoupling capacitors

VCCAUX decoupling capacitors

Closer as possible to GTP DUAL pins --bank 0 of FPGA.

| | |
|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater |
| Document | Conv-TTL-Blo FPGA PS |
| Designer | Carlos Gil Soriano |
| Drawn by | Carlos Gil Soriano 03/10/2012 |
| Check by | |
| Last Mod. | - 03/10/2012 |
| File | FPGAps.SchDoc |
| Print Date | 03/10/2012 18:02:10 |
| Sheet | 2 of 14 |
| Size | A3 |
| Rev | 0 |

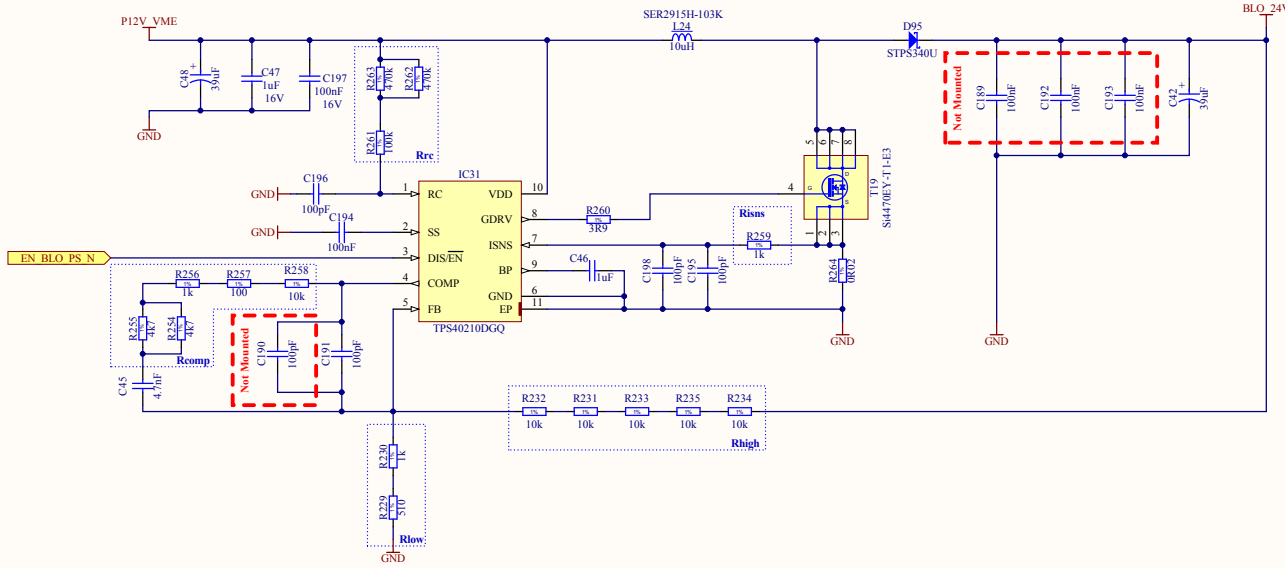
BE-CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

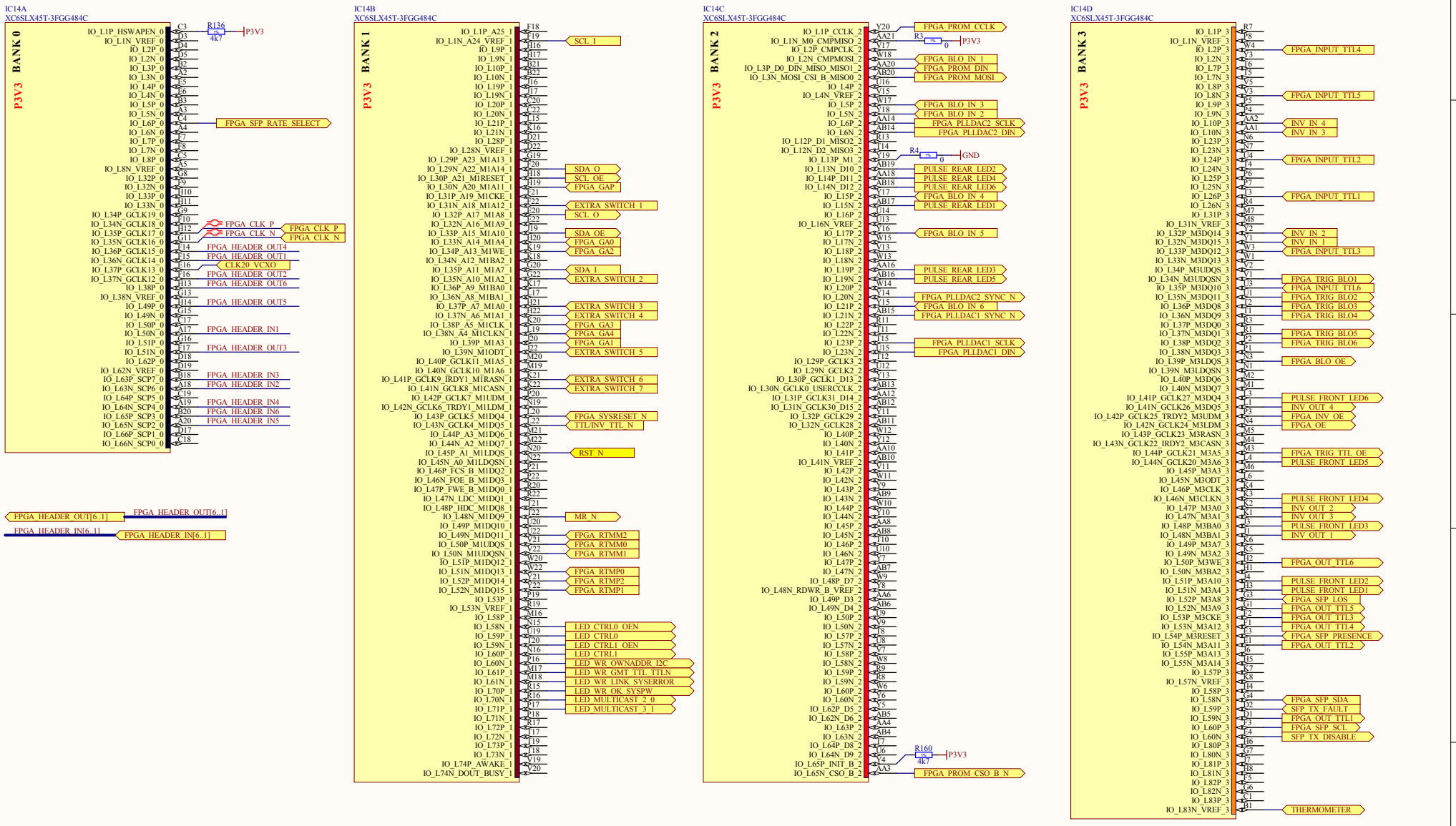
EDA-02446-V2-0

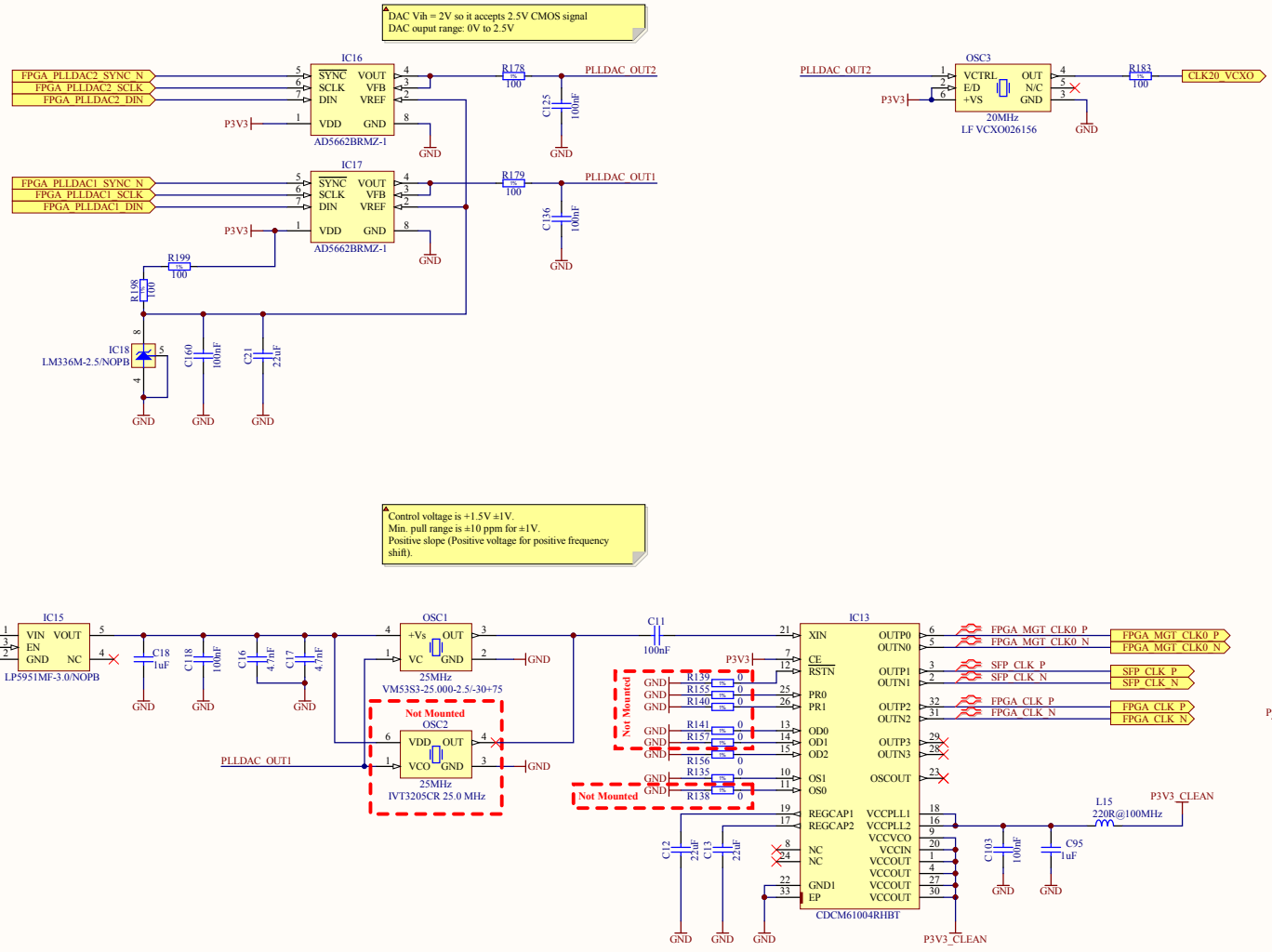
Standard Blocking Voltage

INPUT: 12V
OUTPUT: 24V@2,5A

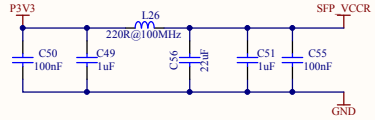


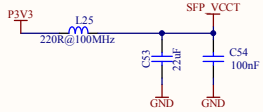

| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo BLOCKING PS | Designer Carlos Gil Soriano | |
| | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File PowerSupplyBlocking.SchDoc | |
| | | Print Date 03/10/2012 18:02:11 | Sheet 3 of 14 |
| BE-CO | European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 / Rev 0 |

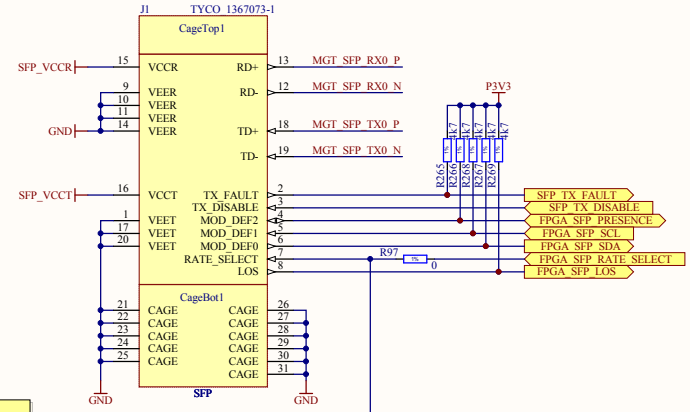




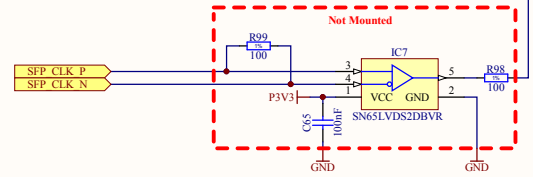

| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo CLOCKS | Designer Carlos Gil Soriano | |
| | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File Clocks&Monitor.SchDoc | |
| | | Print Date 03/10/2012 18:02:12 | Sheet 5 of 14 |
| BE-CO | European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 / Rev 0 |



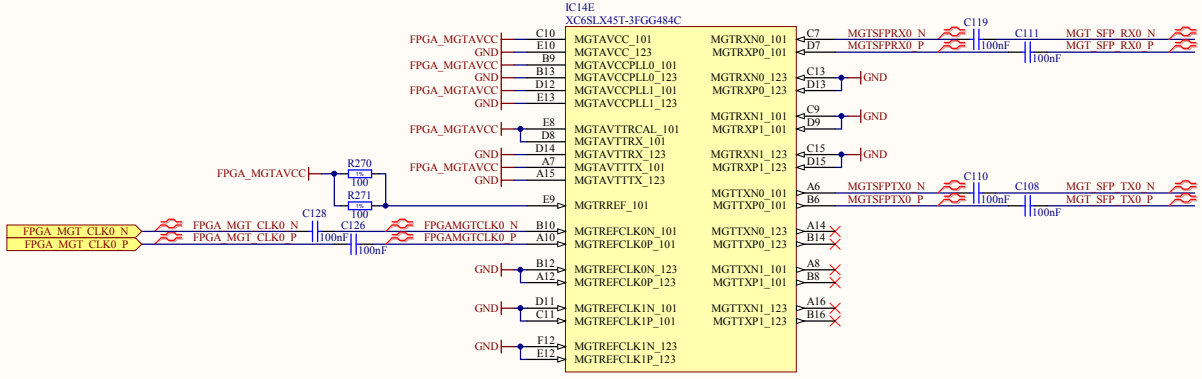




The LVDS receiver can be used to feed a clock to a "custom white rabbit copper SFP".

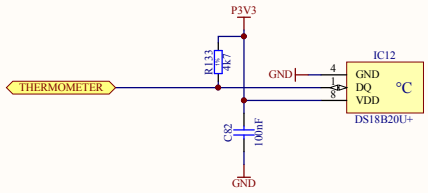



The trace length from the resistor pins to the FPGA pins MGTRREF and MGTVTTRCAL must be equal in length and geometry

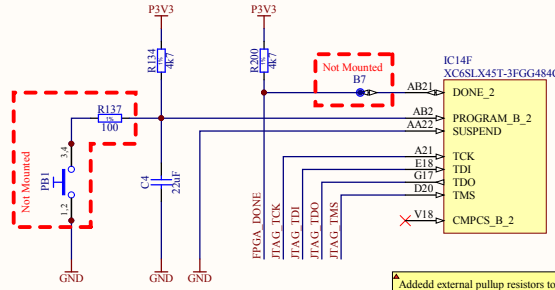


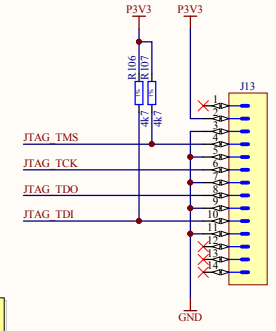

| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo MGTX | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File Communication.SchDoc | |
| | | Print Date 03/10/2012 18:02:12 | Sheet 6 of 14 |
| European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 | Rev 0 |

Thermometer will be used to have a FPGA unique ID



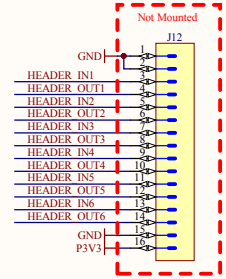

PROGRAM_B must be asserted low for more than 500ns



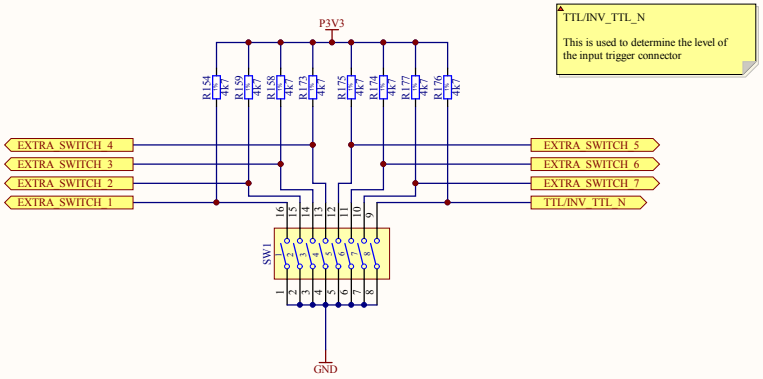

IC14I
XC6SLX45T-3FGG484C
NC U17
NC P15
NC T16

Addedd external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433
However as the JTAG TAP controller fsm is in reset always that TMS experiences two consecutives ones, we can leave it pulled up.
UG380 pg56: the four JTAG pins are internally pulled up.
Hence, there's no need of external ones.



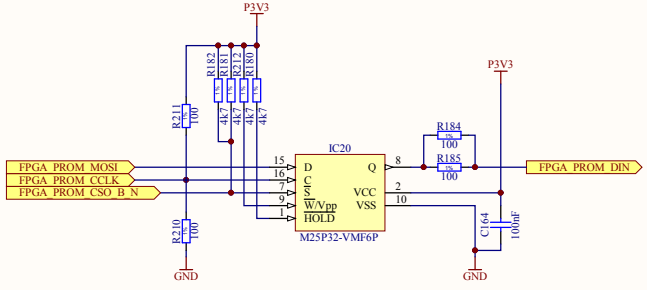

TTL/INV_TTL_N

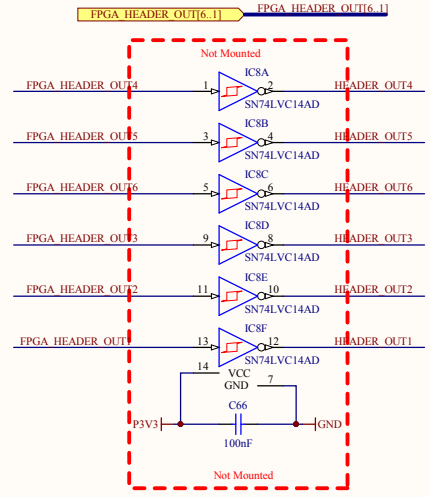
This is used to determine the level of the input trigger connector

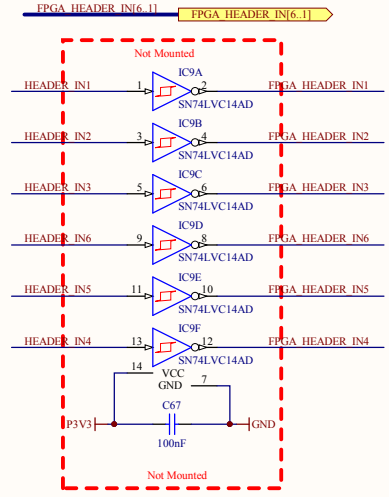



PROM MEMORY

W_N is 1 to allow writes in the memory



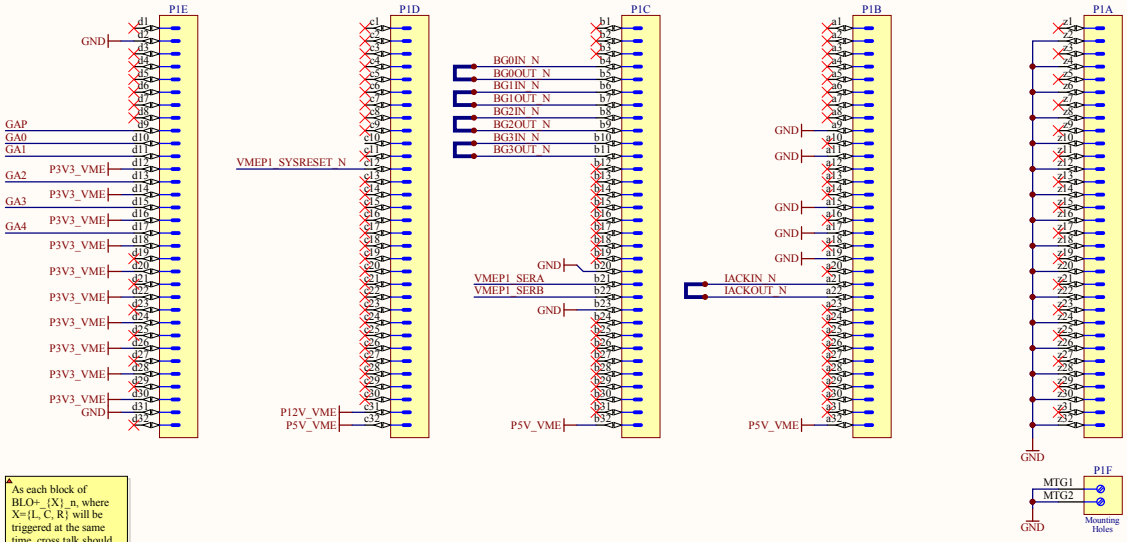




| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo JTAG | Designer Carlos Gil Soriano | |
| | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File JTAG&Button.SchDoc | |
| | | Print Date 03/10/2012 18:02:12 | Sheet 7 of 14 |
| BE-CO | European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 / Rev 0 |

Utility Bus Signal: see page 199
ANSI/VITA 1-1994

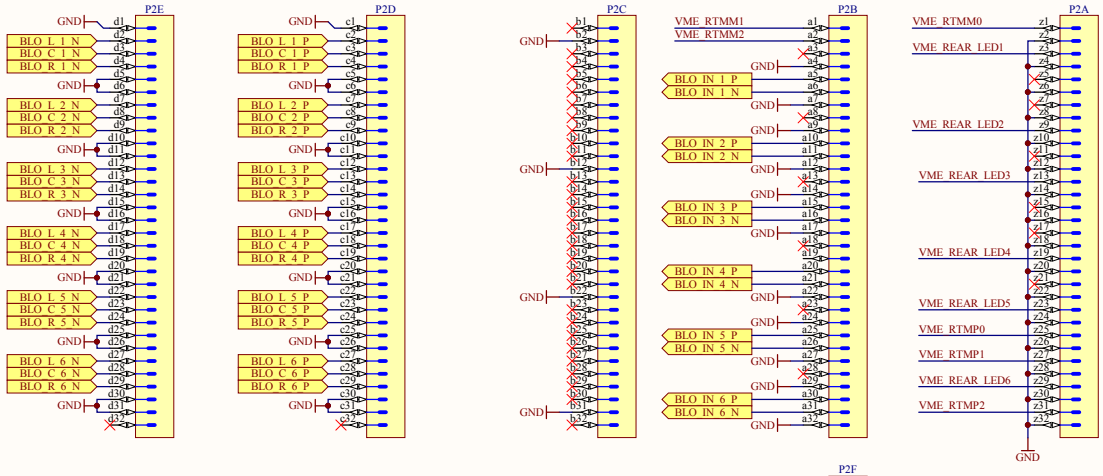
Output configurations in page 230
SYSRESET_N Open collector

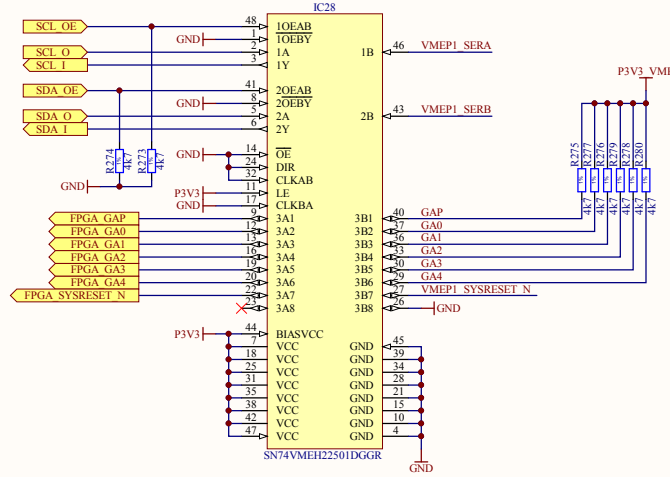


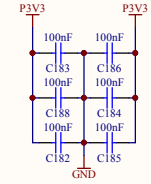

As each block of BLO+_{X}_n, where X={L, C, R} will be triggered at the same time, cross talk should not be so critical.
However, it would be better group the signals as it is shown and leave ground between sets of signals triggered by different sources.

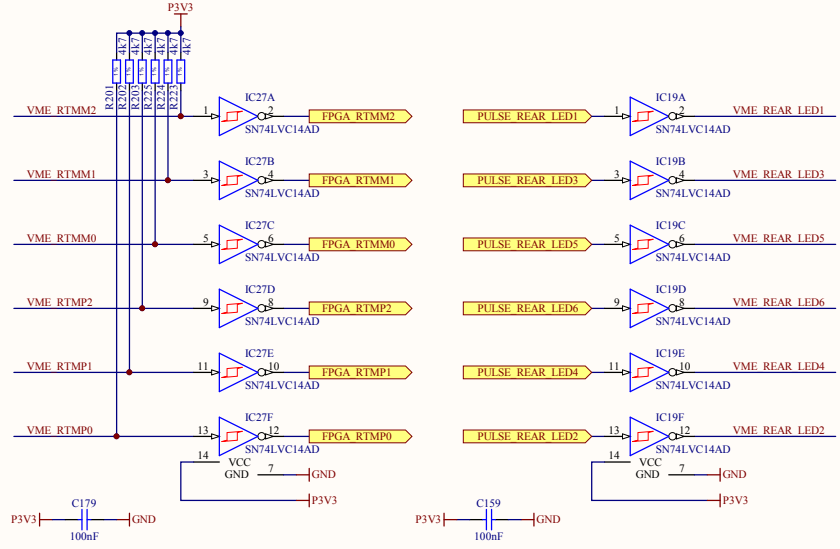
As input signals come from far away, the spectrum of this signal will have less high frequency components that the spectrum of the generated Standard Blocking in conv-ttl-blo
Signals with more spectral power in higher frequencies should be routed more carefully,so it is better to leave the easiest paths to them.
In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used.
Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

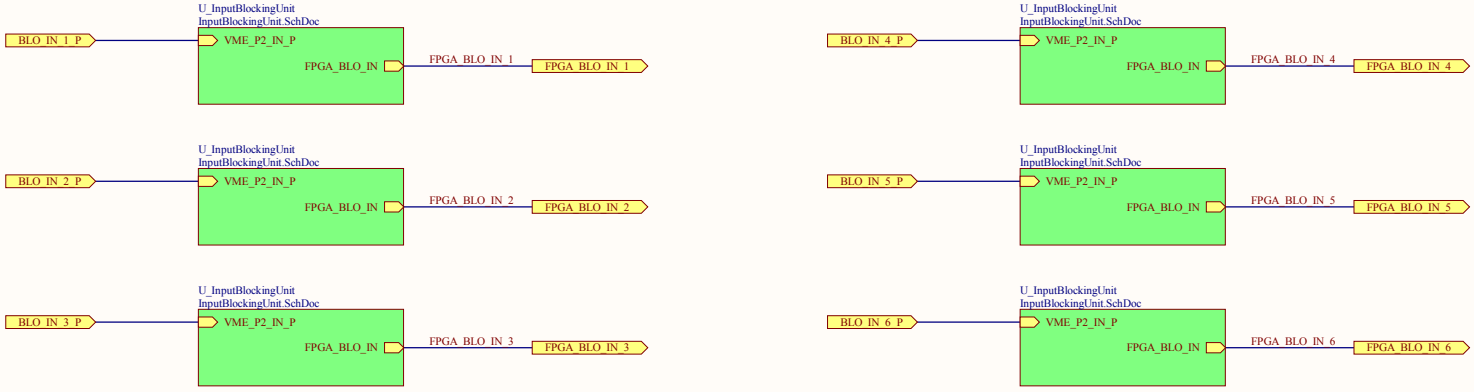



| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo VME64X | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File VME64xConn.SchDoc | |
| | | Print Date 03/10/2012 18:02:13 | Sheet 8 of 14 |
| European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 | Rev 0 |

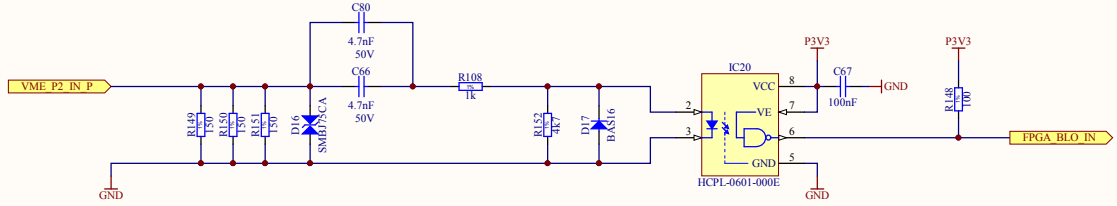



| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | **Conv-TTL-Blo** **INPUT BLO** | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File InputBlocking.SchDoc | |
| | | Print Date 03/10/2012 18:02:14 | Sheet 9 of 14 |
| European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 | Rev 0 |

Input waveforms:
nominal 24V Std.Blocking
minimum 4V Std.Blocking

high pass knee frequency: 170 KHz

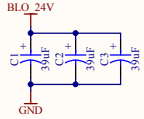
Minimum isolation voltage: 3750 V

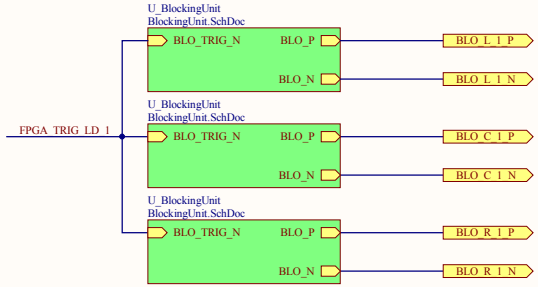


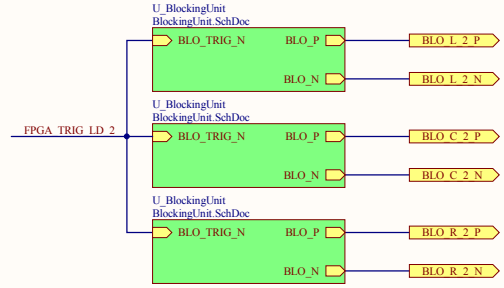

| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | **Conv-TTL-Blo INPUT UNIT** | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File InputBlockingUnit.SchDoc | |
| | | Print Date 03/10/2012 18:02:14 | Sheet 10 of 14 |
| European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 | Rev 0 |

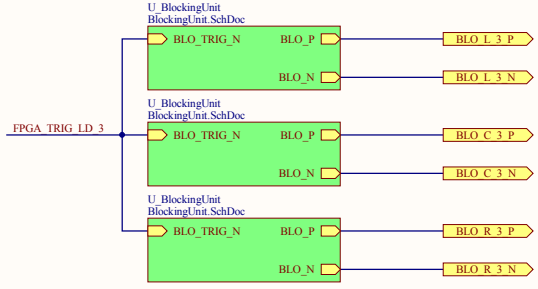
Antiglitch measures:

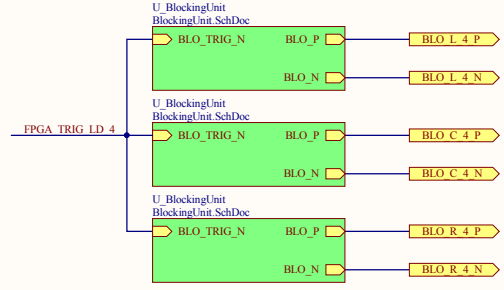
if ANTIGLITCH_OE_N is high the output is high impedance. Then, the pull-down resistors do the rest.

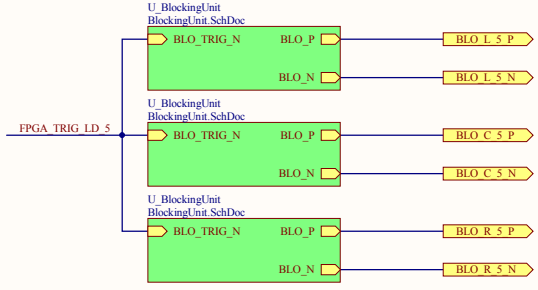


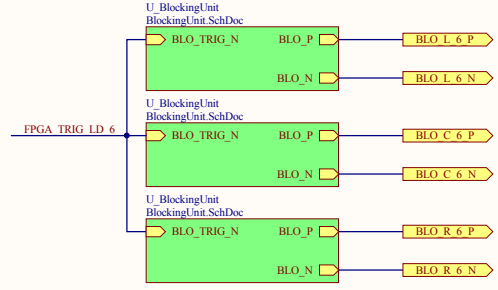



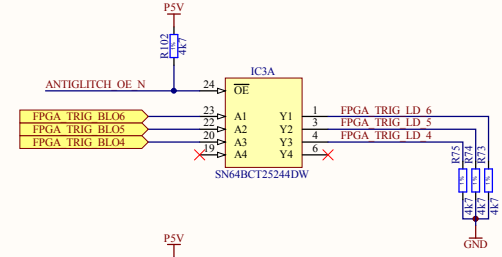



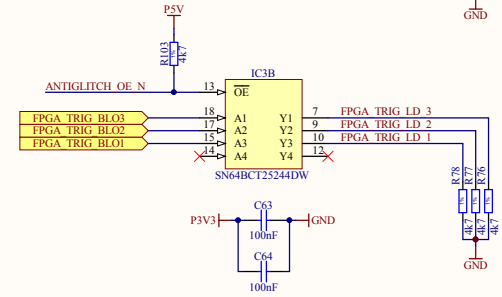



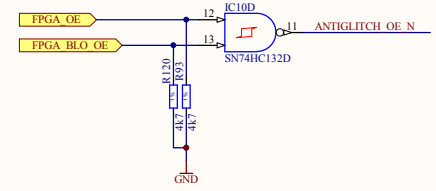



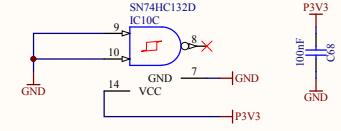



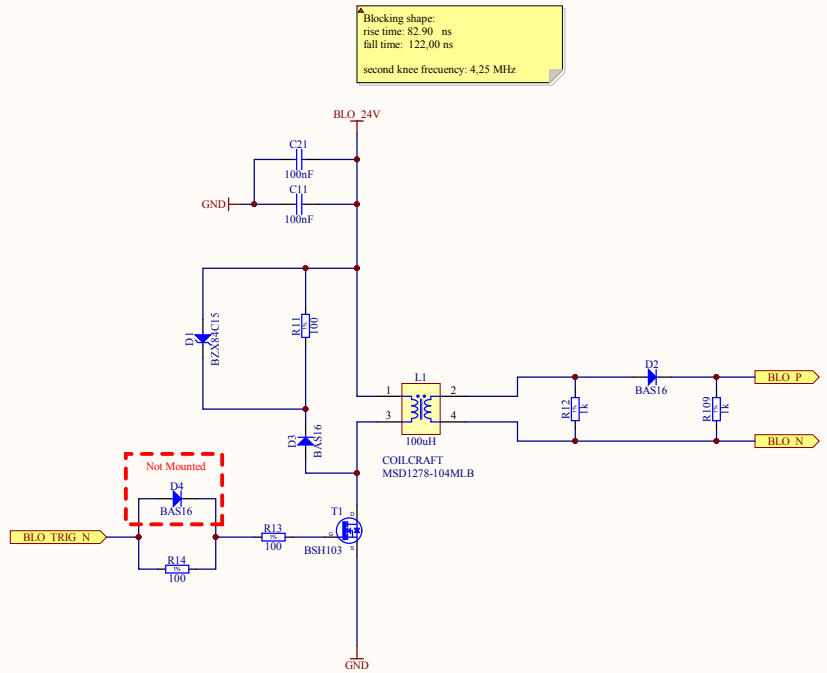



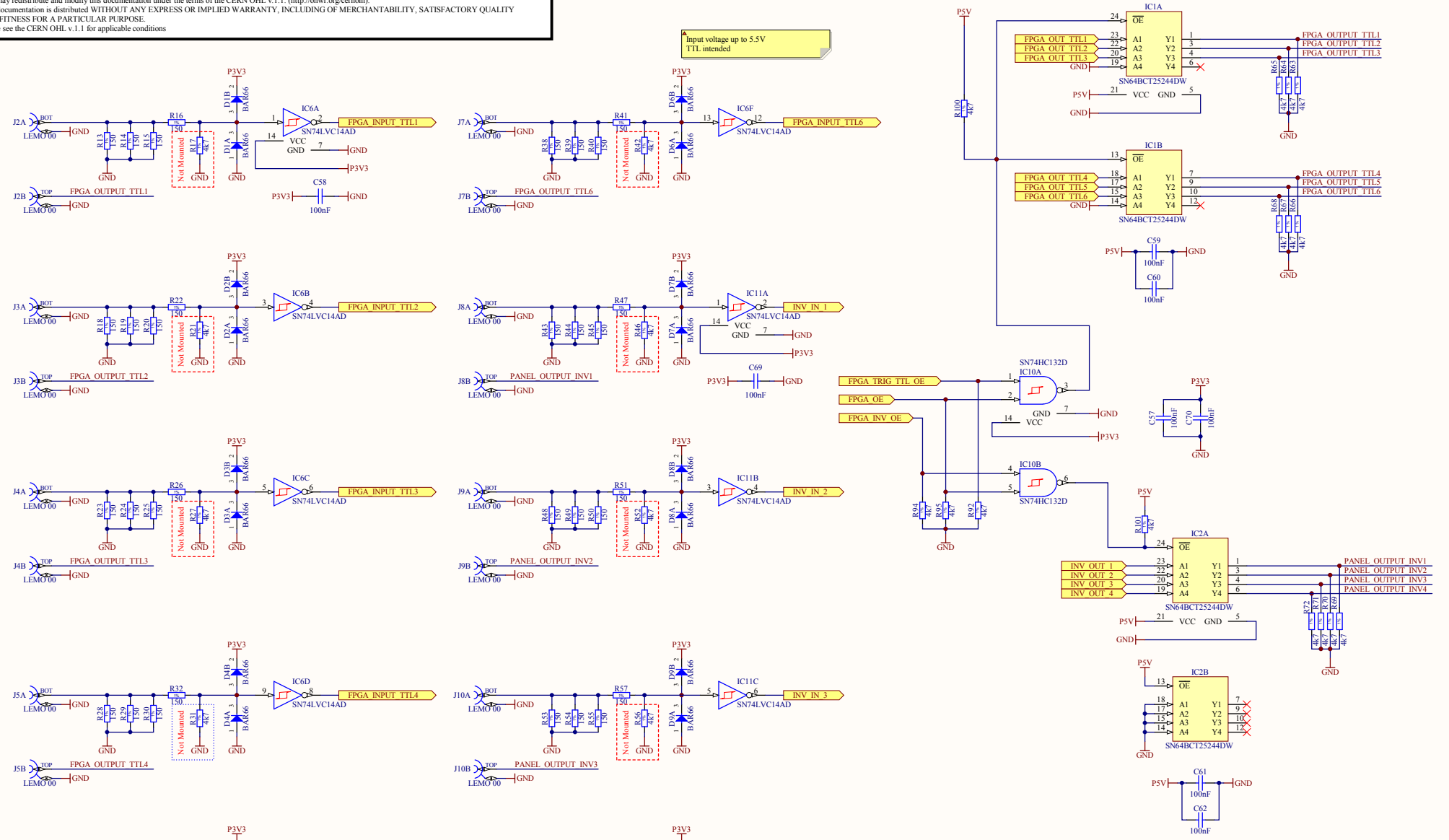




| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | **Conv-TTL-Blo OUTPUT BLO** | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File BlockingOutput.SchDoc | |
| | | Print Date 03/10/2012 18:02:14 | Sheet 11 of 14 |
| *European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland* | EDA-02446-V2-0 | Size A3 | Rev 0 |

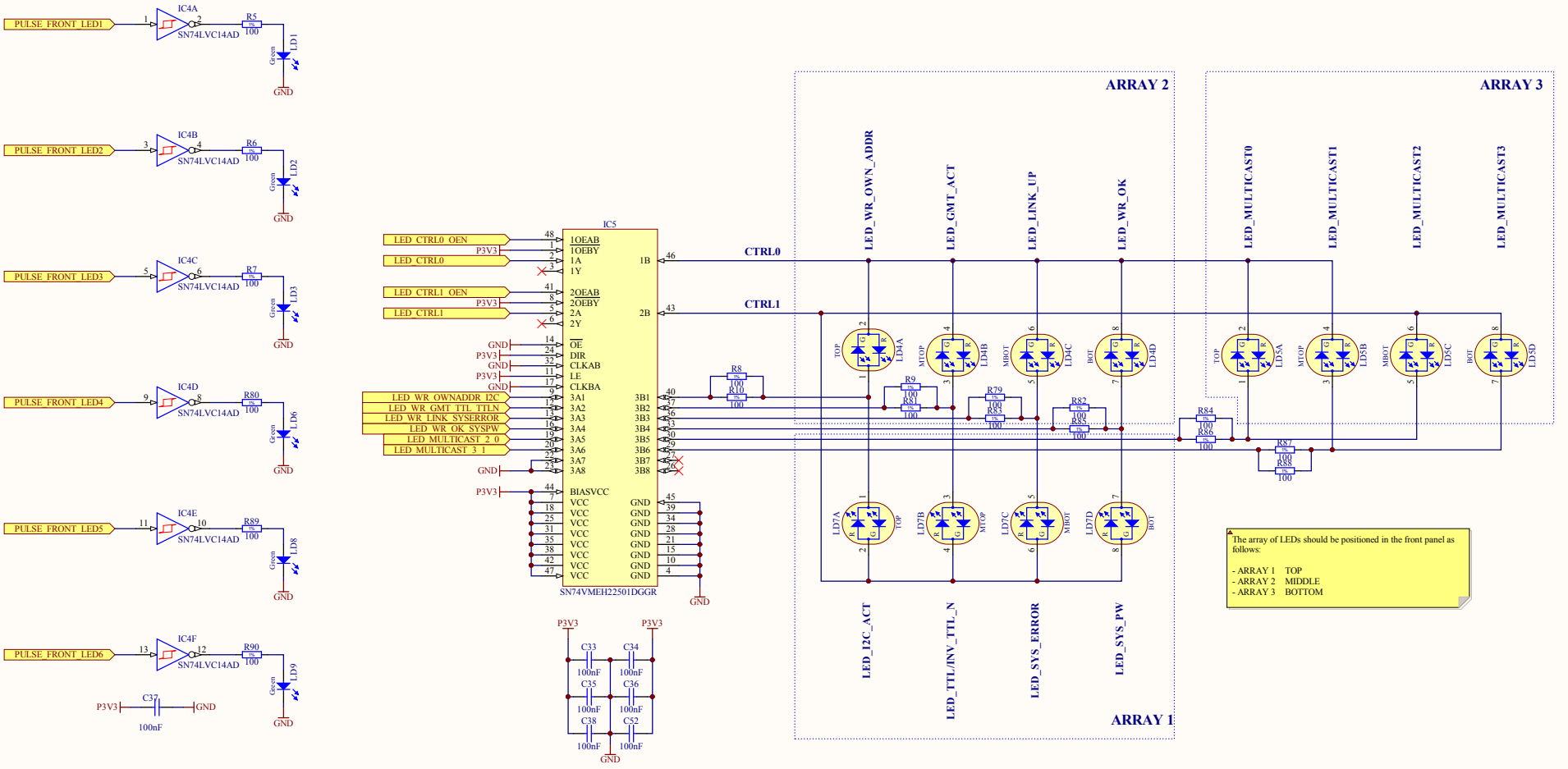



| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo OUTPUT UNIT | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File BlockingUnit.SchDoc | |
| | | Print Date 03/10/2012 18:02:15 | Sheet 12 of 14 |
| European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 | Rev 0 |

Input voltage up to 5.5V
TTL intended




| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | Conv-TTL-Blo FRONT TTL | Designer Carlos Gil Soriano | |
| | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File FrontTTL.SchDoc | |
| | | Print Date 03/10/2012 18:02:16 | Sheet 13 of 14 |
| BE-CO CERN | European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 / Rev 0 |




## ESD discharge strips (top and bottom of the card)

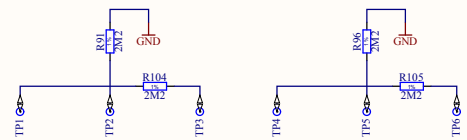



FIG1 FIG2
FIG3 FIG4
FIG5 FIG6

| | | | |
|---|---|---|---|
| Project/Equipment | Standard Blocking Pulse Repeater | | |
| Document | **Conv-TTL-Blo FRONT PANEL** | Designer Carlos Gil Soriano | |
| BE-CO | | Drawn by Carlos Gil Soriano | 03/10/2012 |
| | | Check by | |
| | | Last Mod. - | 03/10/2012 |
| | | File FrontPanelLeds.SchDoc | |
| | | Print Date 03/10/2012 18:02:17 | Sheet 14 of 14 |
| European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland | EDA-02446-V2-0 | Size A3 | Rev 0 |