

CONV-TTL-BLO

Test Log

Theodor-Adrian Stana
BE-CO-HT

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1 Daisy-chain test 1

The setup for this test is as shown in Fig. 1. A CTRV board is used to generate TTL pulses to the CONV-TTL-BLO after which this pulse is daisy-chained as shown in the figure. Both TTL and blocking pulses are generated in the daisy-chain; Fig. 1 highlights the channel where a switch from TTL to blocking or viceversa is made.

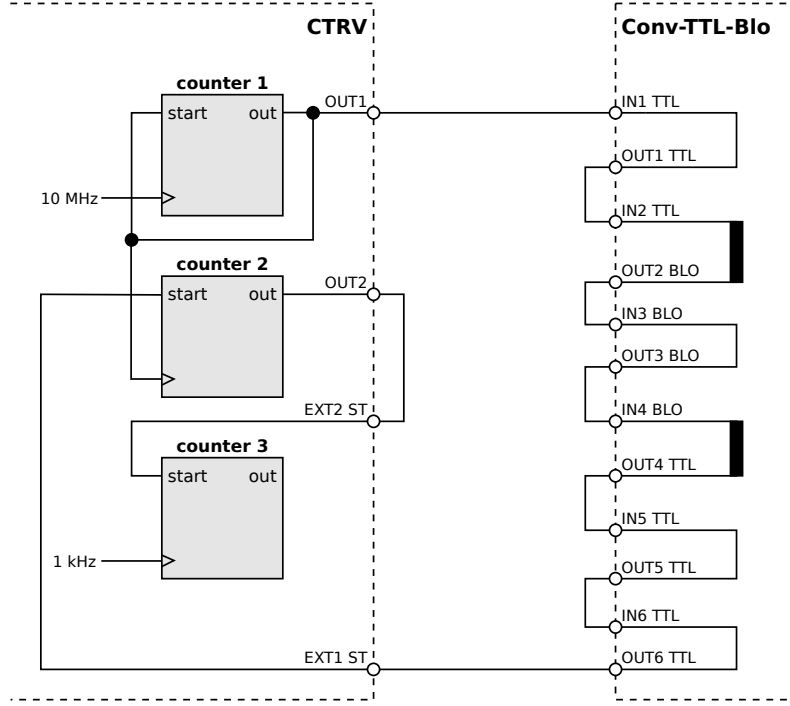


Figure 1: Setup for daisy-chain test 1

Three counters in the CTRV are used; the first is the one which generates the pulses to be sent through the daisy-chain. The output of the first counter is used as the start signal for itself and as the clock for the second-channel counter. The second channel counter is setup to output a DC-level signal (pulse width twice greater than the frequency); this signal is used as the start signal for the third-channel counter. The settings for all of the channels are shown in Table 1.

Table 1: CTRV counter settings

Chan	Pulse width	Freq	Max val
1	1 μ s	100 kHz	100
2	20 μ s (DC)	100 kHz	2
3	–	–	1

Each CTRV counter generates a pulse signal on the output when the counter reaches 0; the start signal causes the value of the counter to be reset and the counter to start counting down. Thus, the configuration in Table 1 yields 1 μ s pulses generated at a frequency of 100 kHz and passed through the daisy-chain. Since the channel 2 counter is configured with a max. value of two, a start pulse from the channel 1 counter starts the counting down and an arriving pulse from the CONV-TTL-BLO restarts the counter. If any pulse is missed by the CONV-TTL-BLO through the daisy-chain, the output of channel 2 counter goes high and this causes the channel three counter to trigger an interrupt. The CTRV is monitored for interrupts using the *ctrvtest* program; any missed pulses (any interrupts) are time-tagged by the program, thus showing when a pulse was missed.