CONV-TTL-BLO
User Guide

Theodor-Adrian Stana
BE-CO-HT

March 8, 2013

Abstract

This document describes the CONV-TTL-BLO board, a Blocking pulse repeater board in double height VME format. It replaces all the following boards:

- 8 channel repeater
- 16 channel repeater
- CTDAC
- LA-BLO-TTL
- LAF-BLO-TTL
- LASB-TTL-BLO
- LA-GATE
- LA-TTL-BLO
- LAPF-TTL-BLO [1]

[1] These boards have a 4 μs pulse width.

Contents

List of Figures

List of Tables

List of abbreviations

FPGA	Field-Programmable Gate Array
RTM	Rear Transition Module
RTMM	RTM Motherboard
RTMP	RTM Piggyback
SFP	Small form-factor pluggable (in the context of SFP connectors)

1 Introduction

CONV-TTL-BLO is a board intended for replicating blocking and TTL pulses, offering six totally independent replication channels. The shape of the pulses is defined in Sec. 4. CONV-TTL-BLO works together with two more boards: CONV-TTL-RTM and CONV-TTL-RTM-BLO.

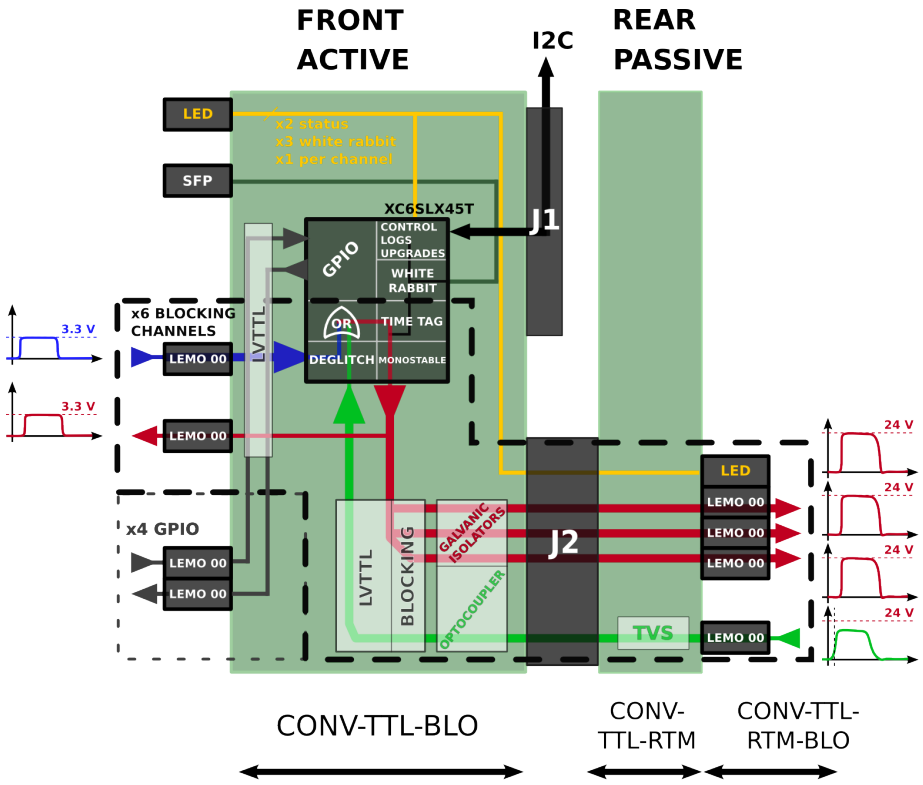

Figure 1: Pulse Repetition system

CONV-TTL-BLO contains all the active circuitry and is connected as a front module to a VME64x backplane. CONV-TTL-RTM and CONV-TTL-RTM-BLO are both connected to the rear part of the crate and provide, in the rear panel, the connectivity of the I/O blocking lines. Every channel offers, in the rear panel, three blocking pulse outputs and one blocking pulse input.

CONV-TTL-RTM is a motherboard attached to the rear transition module (RTM) of the P2 VME64x connector. It connects CONV-TTL-BLO to CONV-TTL-RTM-BLO and provides overvoltage protection for all the I/Os of all the channels.

CONV-TTL-RTM-BLO is an RTM piggyback (RTMP) board mounted

on CONV-TTL-RTM. It contains all the LEMO 00 connectors and channel LEDs that are offered in the rear panel.

Table 1: Boards for Blocking repetition

Board	**Connection**	**Front panel ports**
CONV-TTL-BLO	Front	SFP TTL Blocking triggers TTL Blocking output replica inverters
CONV-TTL-RTM	Back	-
CONV-TTL-RTM-BLO	Back	Blocking Pulse input Blocking Pulse outputs

2 Getting Started

This section provides a description on testing CONV-TTL-BLO boards for basic functionality. The following steps should be followed in order to test the board.

1. Plug in a front module card to the ELMA crate. Turn on power to the crate and program the Spartan-6 FPGA.
2. Check that the *PW* LED lights *green* and the *ERR* LED lights *red*. The *TTL_N* LED may also be lit. If it is and the LED is *green*, then the LEVEL switch is set for INV-TTL pulses.
3. Make sure the LEVEL switch is set for TTL pulses (see Sec. 5.1.1).
4. First, connect one end of a cable with LEMO 00 connectors at both ends to the TTL input port of channel 1 on the front panel.
5. Configure a pulse generator to output TTL level pulses (*max. 5V*) at a frequency of about 1 Hz with a pulse length of approx. 1 μs and connect the other end of the cable to the pulse generator. The LED of the corresponding channel should light for 96 ms when a pulse arrives. A TTL pulse should be replicated at the TTL output of channel 1. Check (using e.g., an oscilloscope) that the TTL pulse has a width of 1 μs and a 3.3 V amplitude.
6. Connect a CONV-TTL-RTM board (with attached CONV-TTL-BLO-RTM) to the back-plane of the ELMA, on the same VME slot as the front module. The *ERR* LED should turn off. The rear panel pulse status LED on channel 1 should be lit for 96 ms to signal pulses are being output on the channel. Check that the pulse width on the output connectors of the rear panel is approx. 1 μs and the amplitude 24 V.

7. Disconnect the LEMO cable from the front panel and configure the pulse generator for 15 V pulse amplitude, keeping the pulse width to approx. 1 μs.

8. Connect the LEMO cable to the input port of channel 1 on the rear panel. Measure that the output pulse on channel 1 is a blocking level pulse with approx. 1 μs pulse width and 24 V in amplitude.

9. Finally, measure on the front panel of the front module that on channel 1 the output pulse is 1 μs long and 3.3 V.

10. Repeat steps 4-9 for all remaining five channels.

3 Front and Rear Panels

Two panels exist in the context of the pulse repeater boards. The first of these is the *front panel*, which corresponds to CONV-TTL-BLO boards and offers various status LEDs, as well as various connectors for TTL and INV-TTL pulses and White Rabbit. The second is the *rear panel*, located on the other side of the backplane and corresponding to CONV-TTL-RTM-BLO boards. The rear panel offers blocking pulse connectors and status LEDs for pulse arrival confirmation.

3.1 Front panel

The front panel of CONV-TTL-BLO boards is shown in Fig. 2. It consists of status LEDs and several ports, divided in four sections from top to bottom:

- System status LEDs;
- Small form-factor pluggable (SFP) connector;
- TTL pulse connectors;
- INV-TTL pulse connectors.

3.1.1 System status LEDs

In the current version of the CONV-TTL-BLO boards, only several of the system status LEDs present on the board are used, due to limited firmware support in the FPGA. The implemented LEDs are presented in Table 2. Unimplemented system status LEDs are off by default.

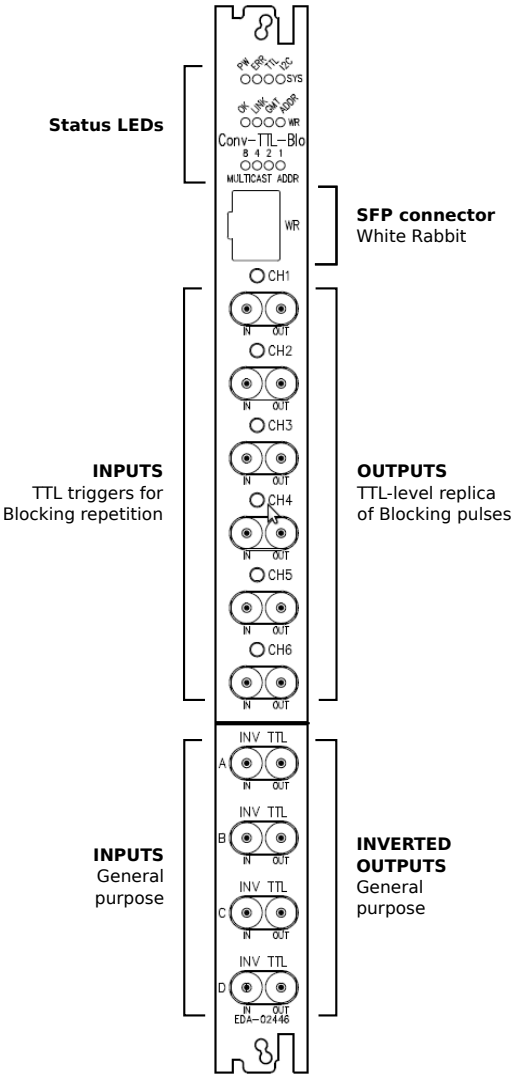

Figure 2: CONV-TTL-BLO panel (front panel)

Table 2: System status LEDs on CONV-TTL-BLO front panels

LED	Description
PW	Power LED. Lights *green* when a valid CONV-TTL-BLO firmware is loaded to the FPGA.
ERR	Error LED. Lights *red* when no rear transition module board is present.
TTL_N	Negated-TTL status LED. Lights *green* when negated TTL logic is selected via the 8^{th} position of the on-board selection switch.

3.1.2 SFP connector

This connector is used to add White Rabbit support to the CONV-TTL-BLO boards. If an optic fibre cable is connected to this socket, White Rabbit precise time-stamping can be added to CONV-TTL-BLO. Four status LEDs above the connector are provisioned to show the status of the White Rabbit link.

White Rabbit is currently not supported in the CONV-TTL-BLO firmware.

3.1.3 TTL triggers

One side of the dual LEMO 00 (type EPY) connector on the CONV-TTL-BLO boards are used for the TTL trigger inputs. By connecting an external trigger source to one of these connectors, a Blocking pulse is generated at the rear panel and a TTL-level pulse is generated at the front panel. The triggers can be either TTL, or INV-TTL level.

All input channels are line-terminated with 50Ω resistors.

3.1.4 Repeated TTL pulses

The other side of the dual LEMO 00 connector is used to output a TTL-level replica of the blocking pulse received at the rear panel, or of the trigger signal arrived on the front panel. The pulse width of this output is similar to the pulse output in the rear panel; the rise time and top pulse level are however different from the Blocking output.

When the pulse is output, the LED of the corresponding channel blinks for 96 ms.

TTL output lines are not internally terminated.

3.1.5 General purpose

Four dedicated inverted-TTL connectors can be found in the lower part of the front panel. Inverted-TTL outputs are not internally terminated.

3.2 Rear panel

The rear panel on CONV-TTL-BLO-RTM boards is shown in Fig. 3. It contains the input and output connectors, as well as pulse status LEDs for six blocking-level pulse channels. A blocking-level pulse at the input connector of a channel is repeated at the three outputs of the same channel in blocking level and TTL level at the output connector of the corresponding channel on the front panel.

When a pulse is repeated on the output connector of a channel, the pulse status LED is lit for 96 ms.

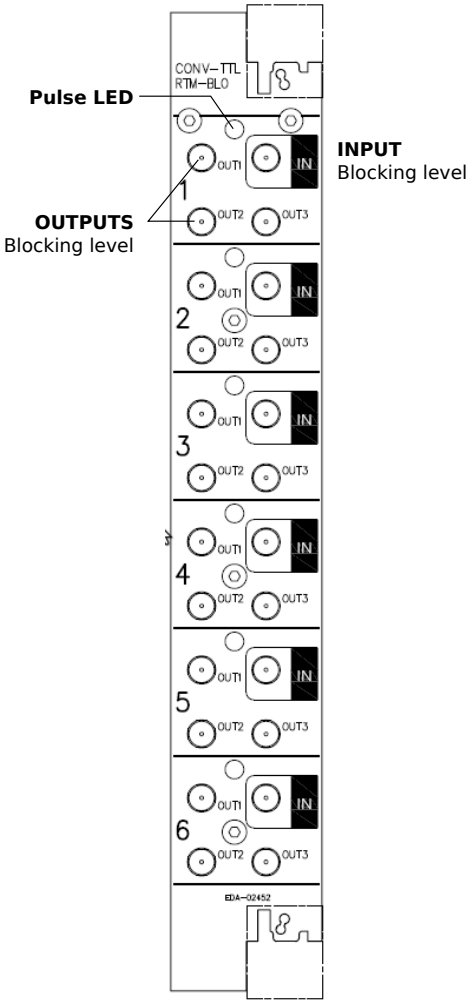

Figure 3: CONV-TTL-BLO-RTM panel (rear panel)

4 Output Pulse Signal

In order for CONV-TTL-BLO boards to work as repeaters, logic is implemented in the on-board FPGA that reacts to a trigger at either rear or front panel and generates a pulse at the output.

Extensive work was made by Carlos Gil-Soriano to research existing boards at CERN and define a standard for pulse levels in repeater boards [1]. Based on this document and on further tests with two of the existing repeater boards at CERN, output pulse widths and amplitudes were selected for the converter boards.

Three types of pulses are defined in the context of CONV-TTL-BLO boards. They differ only in signal amplitude and signal rise and fall times, due to the circuitry used to generate them; pulse widths are the same for all three types. Table 3 presents the different types of pulses and Fig. 4 shows a graphic representation of the pulse signal.

Table 3: Trigger sources

Type	**Pk-pk amplitude**	**Comments**
TTL	3.3 V	
INV-TTL	3.3 V	Inverted version of TTL pulse
Blocking	24 V	

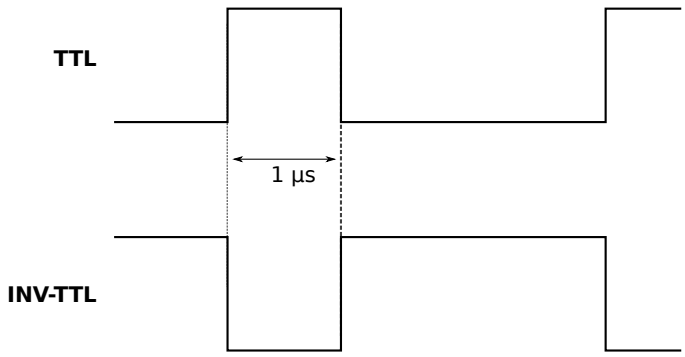

Figure 4: Pulse signal shape

5 Converter Boards

This section gives further information about the three boards which when coupled together can be used to replicate blocking-level pulses.

5.1 CONV-TTL-BLO

A picture of the CONV-TTL-BLO mainboard is presented in Fig. **??**. This board represents the main part of the converter system; all of the active circuitry involved in pulse repetition is present on this board. The Spartan-6 FPGA is the core part of the board, reacting to pulses at either the TTL inputs arriving on front panels, or blocking pulses arriving on rear panels through the RTM system, and generating pulses for the output channels, both blocking and TTL.

board picture

5.1.1 TTL and INV-TTL inputs

TTL and INV-TTL level pulses arrive through the LEMO connectors. The pulses are passed through a Schmitt trigger buffer circuit to smooth out transitions and then passed to the FPGA. The buffer circuit is shown in Fig. 5 and is common to the six TTL input channels and the four INV-TTL input channels.

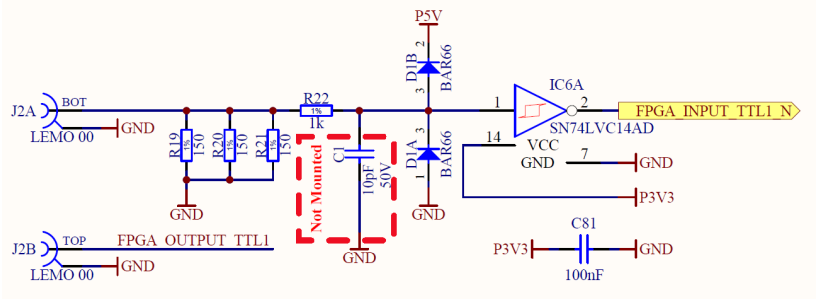

Figure 5: TTL and INV-TTL input circuit

Since a signal at the input can be both TTL and INV-TTL, a switch (called the *LEVEL* switch) is provided on the board to select between the two. The switch (shown in Fig. **??**) is checked in the FPGA logic and the output pulse per each channel is adjusted according to its status.

As can be seen in Fig. **??**, when the switch is in the upper position, it indicates that the signal on TTL and INV-TTL inputs is TTL level. When the switch is in the lower position, this indicates an INV-TTL level at TTL and INV-TTL inputs.

LEVEL switch pic

A board can only have TTL *or* INV-TTL inputs at one time on *any* channel, not both. The LEVEL switch indicates which of the two it is. Since there is only one LEVEL switch on CONV-TTL-BLO boards, it is not possible to set the type of signal per each channel.

5.1.2 Blocking inputs

After their arrival in the rear panel through the RTMP LEMO connectors, blocking pulses pass through an input circuit, shown in Fig. 6. This circuit's function is to adjust the voltage level of the blocking pulse to a level more suitable for input to the FPGA. A transient voltage suppressing diode at the input offers protection against any voltage spikes at the input, while the optocoupler provides the voltage adjustment.

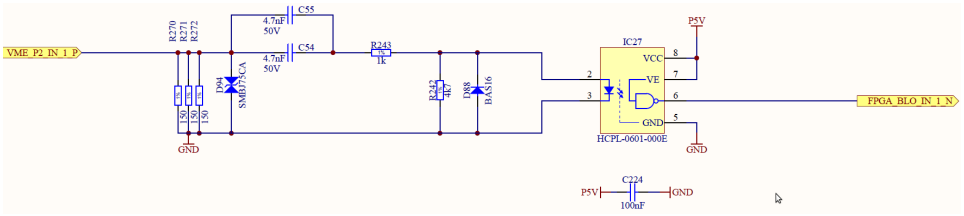

Figure 6: Blocking input circuit

Signal levels expected at the input match those of the blocking standard definition [1]. **The minimum signal level that the optocoupler is sensitive to is 5 V.**

The output of this circuit is further passed through a Schmitt-trigger buffer to smooth out transitions. Since the buffer is the same inverting buffer present in the TTL input circuits, the inverted pulse signal coming out of the circuit in Fig. 6 is once again inverted, and the FPGA receives the recovered pulse signal in normal polarity.

5.1.3 Blocking outputs

The blocking output circuit is shown in Fig. 7. The circuit is a typical flyback topology [2], with the Coilcraft inductor providing a galvanically isolated pulse at the output. Rise and fall times of the pulse signals are controlled mainly by the resistors at the gate of the MOSFET transistor

6 FPGA Logic

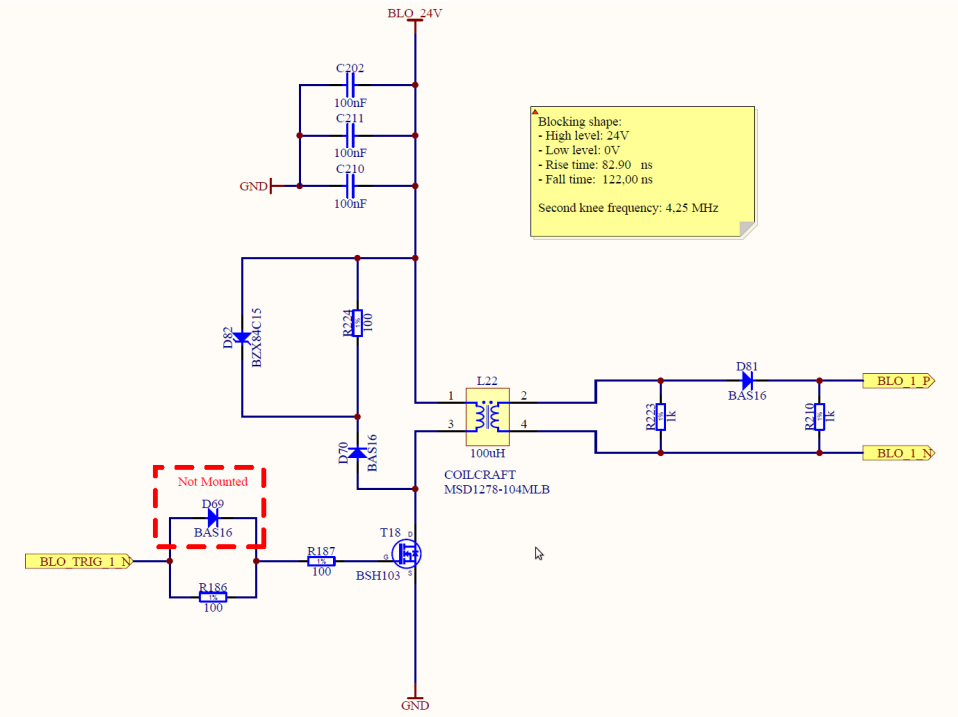

Figure 7: Blocking output circuit

References

[1] C. G. Soriano, "Standard Blocking Output Signal Definition for CTDAH board," Sept. 2011. `http://www.ohwr.org/documents/109`.

[2] "Under the Hood of Flyback SMPS Designs." `http://focus.ti.com/asia/download/Topic_1_Picard_42pages.pdf`.