CONV-TTL-BLO
User Guide

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Revision history

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List of Abbreviations

FPGA	Field-Programmable Gate Array
I^2C	Inter-Integrated Circuit
PG	Pulse Generator
RTM	Rear Transition Module
SFP	Small Form-factor Pluggable (connector)
VME	VERSAmodule Eurocard

1 Introduction

CONV-TTL-BLO is a board intended for replicating TTL and blocking pulses. The main features of the board are:

- VME64x form-factor
- Six independent pulse replication channels, each channel capable of replicating
  - TTL to blocking
  - TTL-BAR to blocking
  - Blocking to TTL
  - Blocking to TTL-BAR
  - Blocking to blocking
  - TTL to TTL
  - TTL-BAR to TTL-BAR
- Four general-purpose inverter channels
- SFP connector for White Rabbit [1]
- Can use I^2C lines on VME P1 connector for remote monitoring
- Status LEDs
- Pulse LEDs for each replication channel

CONV-TTL-BLO is a VME64x front-module that can be used standalone as a TTL or TTL-BAR pulse repeater using the six replication channels, or as a TTL to TTL-BAR (TTL-BAR to TTL) converter using the four general-purpose inverter channels.

By combining the CONV-TTL-BLO with the CONV-TTL-RTM rear-transition module (RTM) and the associated CONV-TTL-RTM-BLO piggyback board in the rear part of the VME crate, a flexible six-channel pulse conversion system can be obtained. Such a system is shown in Figure 1. TTL pulses arriving on an input TTL channel are regenerated in the FPGA and sent on the channel's TTL output, as well as on the three blocking outputs on the RTM. Similarly, blocking pulses arriving on a blocking input channel are regenerated in the FPGA and replicated on both the TTL and blocking outputs of the channel.

CONV-TTL-BLO contains all active circuitry in a pulse conversion system. It handles pulse generation and conversion from/to blocking. CONV-TTL-RTM is a passive module used as an interface from the rear part of the VME crate to the front module.

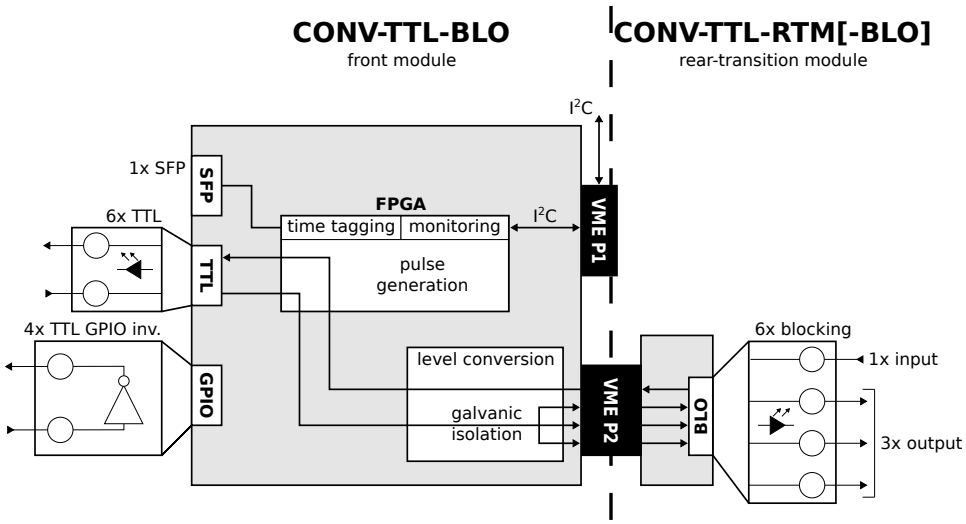


Figure 1: Simplified block diagram of the pulse conversion system

2 Front and rear panels

Two panels exist in the context of the pulse repeater boards. The first of these is the *front panel*, which corresponds to CONV-TTL-BLO boards and offers various status LEDs, as well as various connectors for TTL-level pulses and White Rabbit. The second is the *rear panel*, located on the other side of the VME backplane and corresponding to CONV-TTL-RTM-BLO boards. The rear panel offers blocking pulse connectors and status LEDs for pulse replication confirmation.

2.1 Front panel

The front panel of CONV-TTL-BLO boards is shown in Figure 2. It consists of status LEDs and several ports; these are, from top to bottom:

- System status LEDs;
- Small form-factor pluggable (SFP) connector;
- TTL pulse connectors and associated pulse LEDs;
- General-purpose inverter channels.

2.1.1 System status LEDs

There are twelve bicolor status LEDs on the CONV-TTL-BLO front panel. The implemented status LEDs are presented in Table 1. Unimplemented system status LEDs are *off*.

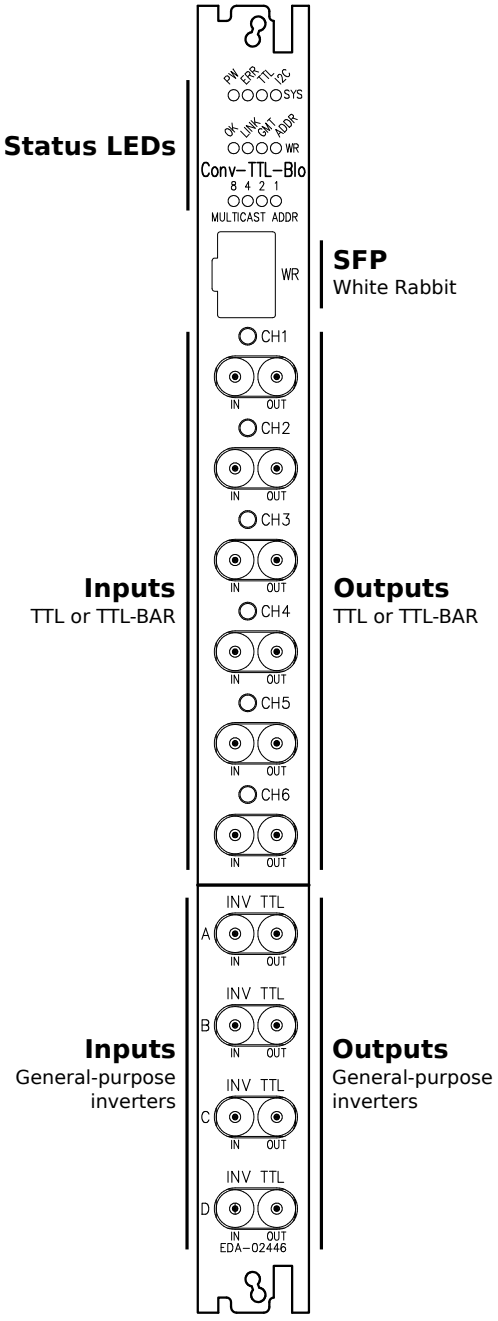


Figure 2: CONV-TTL-BLO panel (front panel)

Table 1: System status LEDs on CONV-TTL-BLO front panels

LED	Description
PW	Power LED. Lights *green* when a valid CONV-TTL-BLO firmware is loaded to the FPGA.
ERR	Error LED. Lights *red* when no RTM board is present, *off* if a valid RTM is present.
TTL	TTL status LED. Lights *green* when TTL logic is selected via the on-board selection switch, *off* when TTL-BAR logic is selected.
I2C	I^2C status LED. Flashes *green* when an I^2C transfer is taking place. Lights *red* when a transfer error occurs, or when the CONV-TTL-BLO register being addressed does not exist. Turns *off* after a successful transfer has ended.

2.1.2 SFP connector

This connector is used to add White Rabbit support to the CONV-TTL-BLO boards. If an optic fibre cable is connected to this socket, White Rabbit precise time-stamping can be added to CONV-TTL-BLO. Four status LEDs above the connector are provisioned to show the status of the White Rabbit link.

White Rabbit is currently not supported by the FPGA firmware.

2.1.3 TTL inputs and outputs

Six of the LEMO 00 connectors on the CONV-TTL-BLO board are TTL repeater channels. Both front-panel inputs and outputs are TTL-level (0-3.3 V). The signal type and the inputs and outputs can be either TTL or TTL-BAR, as selected by the TTL switch (SW2.4, see Section 4.2).

A simplified diagram of pulse repetition is shown in Figure 3, more details can be found in Section 4.3. If a TTL (TTL-BAR) pulse arrives on a channel input, it gets replicated on the output of the same channel in TTL (TTL-BAR), as well as the blocking outputs of the same channel on the rear panel, if a CONV-TTL-RTM board with an attached CONV-TTL-RTM-BLO is present. Similarly, if a blocking pulse arrives on the back panel, it is replicated on the TTL output channel.

Each TTL replication channel has a pulse LED which flashes shortly whenever a pulse is replicated on the channel.

All TTL input channels are terminated with 50Ω resistors; TTL output channels are not terminated.

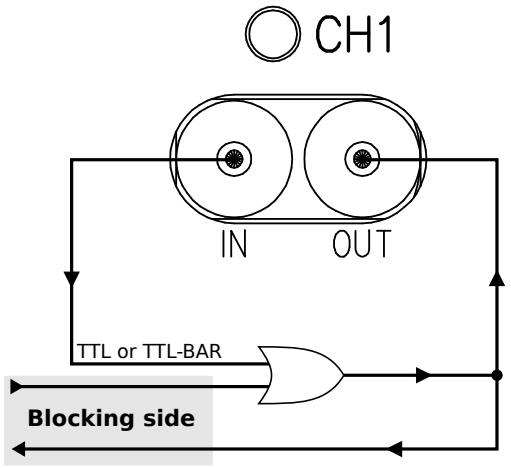


Figure 3: Pulse repetition on front channel

2.1.4 General-purpose inverters

Four general-purpose TTL inverter channels can be found in the lower part of the front panel. The output of a channel is always an inverted version of the channel input (Figure 4). No regeneration is performed on the input signal, nor is it in any way connected to the blocking outputs on the RTM. The input signal is simply passed through an inverter and presented at the channel output (see Figure 1).

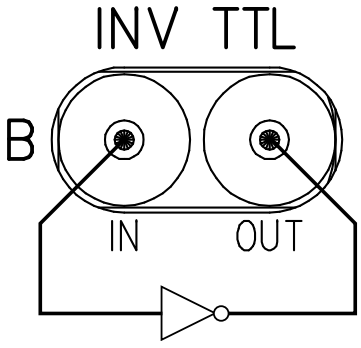


Figure 4: TTL general-purpose inverter channel

All general-purpose inputs are terminated with 50Ω resistors; the outputs are not terminated.

2.2 Rear panel

The rear panel on CONV-TTL-BLO-RTM boards is shown in Figure 5. It contains the input and output connectors, as well as pulse status LEDs for six

blocking-level pulse channels. A blocking-level pulse at the input connector of a channel is repeated at the three outputs of the same channel in blocking level and in TTL level at the output connector of the corresponding TTL channel on the front panel.

All blocking input channels have internal line-termination with 50Ω resistors. Blocking outputs are not line-terminated. Each output on a channel has a separate blocking driver.

When a pulse is repeated on the output connector of a channel, the pulse status LED flashes briefly.

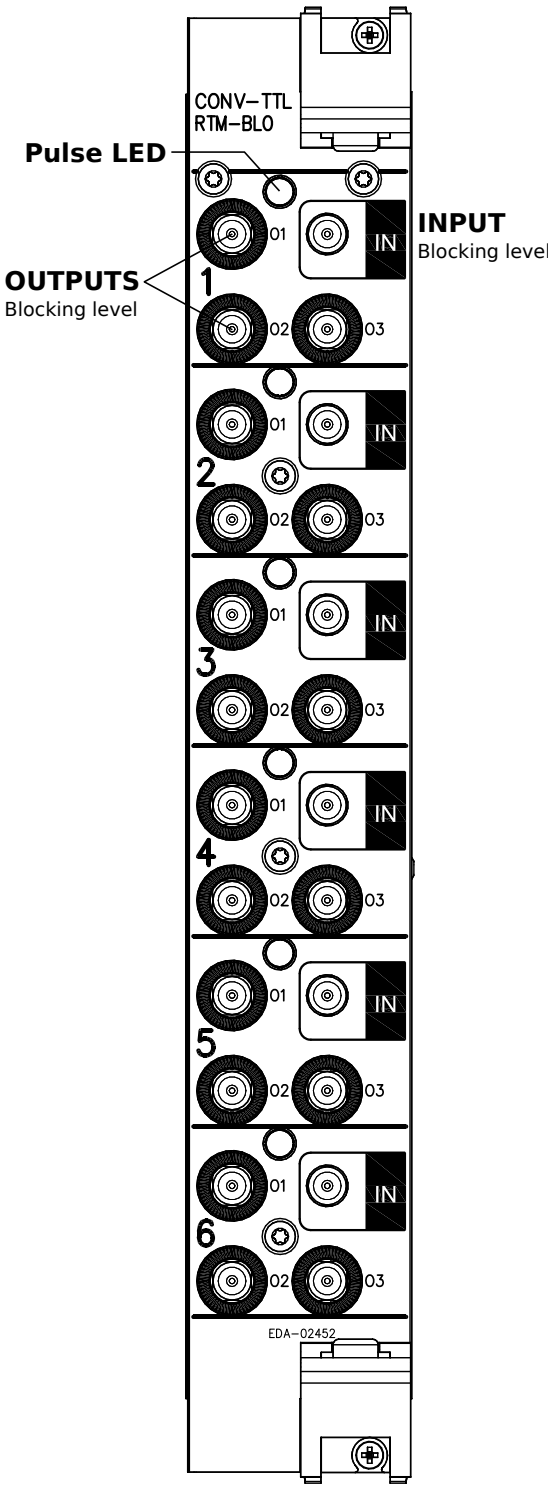


Figure 5: CONV-TTL-BLO-RTM panel (rear panel)

3 On-board switches

There are eight switches provided on-board the CONV-TTL-BLO board, shown in Figure 6. Table 2 lists the used switches.

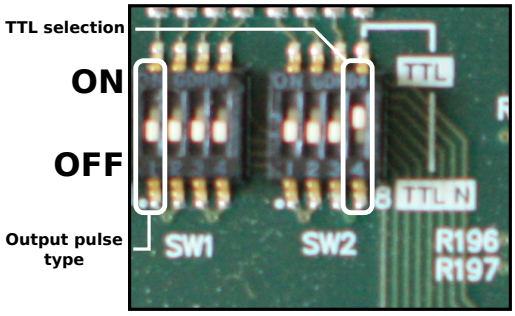


Figure 6: Switches on the CONV-TTL-BLO board

Table 2: Switches on CONV-TTL-BLO

Switch	Description
SW1.1	Selects the between jitter-free and glitch-filtered pulses (see Section 4.3) **ON** – glitch-filtered, with output jitter **OFF** – glitch-sensitive, without output jitter
SW2.4	TTL/TTL-BAR selection switch (see Section 4.2) **ON** – TTL channels receive and generate TTL pulses **OFF** – TTL channels receive and generate TTL-BAR pulses

Note that both switches are board-wide switches; selecting one position or the other yields a selection valid for all six pulse replication channels.

The default position of the switches is **OFF**.

4 Pulse replication

4.1 Pulse signal definition

Three pulse types are defined in the context of CONV-TTL-BLO, depending on signal amplitude, rise and fall times; pulse widths and frequencies are the same. TTL and TTL-BAR pulses are input and output on the front panel of the boards. TTL-BAR is essentially an inverted version of TTL signals. Blocking pulses [2] are input and output on the ear panel (via a CONV-TTL-RTM).

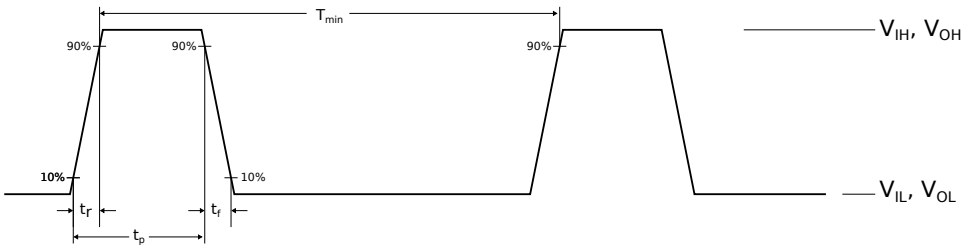


Figure 7: Pulse signal characteristics

Table 3: TTL and TTL-BAR pulse characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input pulse high-level amplitude (1)	1	3.3	5.5	V
V_{IL}	Input pulse low-level amplitude		0		V
V_{OH}	Output pulse high-level amplitude		3.3		V
V_{OL}	Output pulse low-level amplitude		0		V
t_p	Pulse width		1.2		μs
T_{min}	Period of pulse signal (2)	4.8			μs
t_r	Rise time		140		ns
t_f	Fall time		160		ns

Note 1: Min. pulse amplitude for which a t_p wide pulse is replicated at the output.
Note 2: Max. pulse frequency dictated by blocking output max. frequency. All voltages are referred from 0 V; unless otherwise noted, all values are typical values.

The various characteristics of the pulse signals are defined in Figure 7 and outlined in Table 3 for TTL and TTL-BAR pulses and in Table 4 for blocking pulses.
Note 1: Min. pulse amplitude for which a t_p wide pulse is replicated at the output.
Note 2: Max. pulse frequency dictated by blocking output max. frequency.

Table 4: Blocking pulse characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input pulse high-level amplitude (1)	5.5	24	V	
V_{IL}	Input pulse low-level amplitude	0.5	4.5	V	
V_{OH}	Output pulse high-level amplitude	3.3	24	V	
V_{OL}	Output pulse low-level amplitude	0	0	V	
t_p	Pulse width	1.2	1.2	μs	
T_{min}	Min. period of pulse signal (2)	4.8	4.8	μs	
t_r	Rise time	6.4	140	ns	
t_f	Fall time	3	160	ns	

All voltages are referred from 0 V; unless otherwise noted, all values are typical values.

4.2 TTL vs. TTL-BAR

The two signal types that may be replicated on the front panel are inverted versions of one another, as Figure 8 shows.

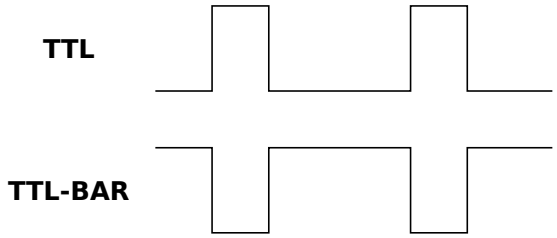
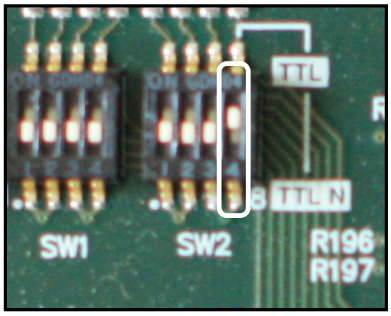


Figure 8: TTL and TTL-BAR signals

Selection between which of the two signal types is repeated on the front panel is done by means of the TTL selection switch, SW2.4 (Figure 9). When the switch is **ON**, TTL pulses arriving on the front panel input or blocking pulses arriving on the rear panel input are replicated to TTL pulses on the front panel. When the switch is **OFF**, TTL-BAR pulses arriving on the front panel or blocking pulses arriving on the rear panel are replicated to TTL-BAR pulses on the front panel.

The TTL selection switch is valid board-wide, i.e., if it is set for TTL inputs (**ON**), TTL signals should be input on all TTL channels. Inputting TTL-BAR signals on a channel while the TTL/TTL-BAR selection switch is set to TTL introduces a delay of one pulse width on the generated TTL pulse.



ON: TTL pulses
on input and output

OFF: TTL-BAR pulses
on input and output

Figure 9: TTL/TTL-BAR selection switch

4.3 Pulse replication mechanism

Figure 10 shows a diagram of how pulses are replicated on a channel inside the FPGA. The figure also shows the shape of the different types of pulse signals after they pass through a part of the circuit. The grey DC signals are the signals when no wire is plugged into a channel.

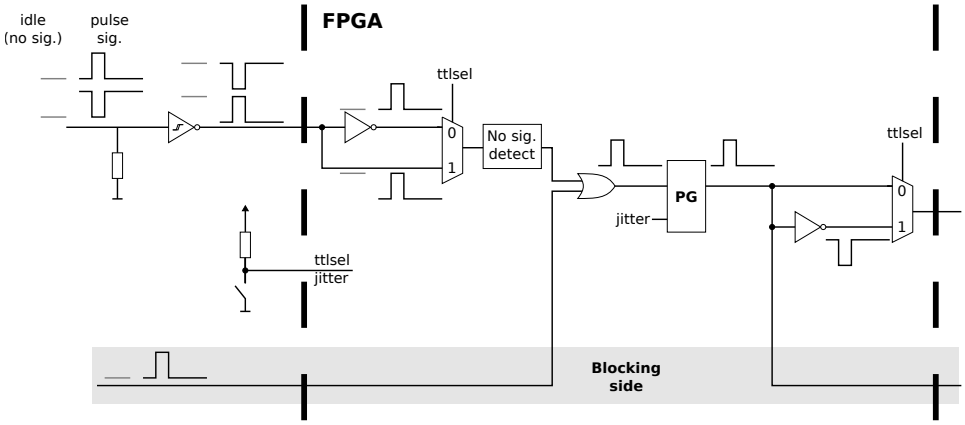


Figure 10: Pulse repetition mechanism

The pulse generator (PG) block in the FPGA generates TTL pulses at its output on the rising edge of its input. It therefore expects TTL pulses at its input. The rest of the logic external to this block is used to accomodate for TTL-BAR and blocking pulses.

First, the OR gate at the PG input indicates the condition for a pulse to be regenerated. When a pulse arrives at either of the two inputs, TTL/TTL-BAR (front panel) or blocking (rear panel), a pulse is generated on the output.

On the blocking side, the voltage level of blocking pulses arriving on the RTM is adapted to a voltage level suitable for the FPGA by on-board circuitry external to the FPGA. What ends up in the FPGA is a TTL type

pulse, so this may be passed directly to the PG's input through the OR gate. The output of the PG block is passed to the FPGA output and to the three blocking pulse outputs of a channel, where the blocking-level pulse is generated.

On the TTL side, pulse signals go through a Schmitt trigger inverter buffer to the FPGA. The termination resistor pulls the input line to ground when there is no signal, so this gets inverted to V_{cc} by the Schmitt trigger. Based on the setting of the TTL switch (see Section 4.2), the multiplexer assures a TTL signal at the OR gate input.

The block at the multiplexer output detects the lack of a signal by checking for a continuous high level on the line. This is important when the TTL selection switch is set to TTL-BAR, since no signal would mean a DC high-level signal appears at the OR gate input and this signal would inhibit pulses arriving from the blocking side.

4.4 Pulse jitter and delay

As outlined in Section 3, the PG block is capable of generating either jitter-free, or glitch-filtered pulses. SW1.1 (Figure 11) selects between the two options.

ON: Type 1, glitch-sensitive, non-jittery pulses

OFF: Type 2, glitch-filtered, jittery pulses

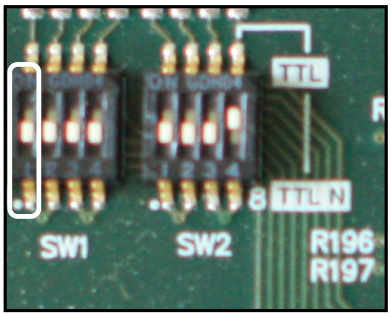


Figure 11: Pulse jitter selection switch

When SW1.1 is in the **OFF** (default) position, jitter-free pulses are generated, since the pulse signal is replicated at the output without being sampled with an on-board clock. This however also means that any glitch pulse wider than 8 ns will trigger pulse generation at the output.

Placing SW1.1 in the **ON** position will enable glitch filtering on the PG block. The pulse signal is in this case sampled with a 125 MHz on-board clock and passed through a glitch filter which rejects any pulses narrower than 40 ns, but introduces an 8 ns jitter at the output, as shown in Figure 12.

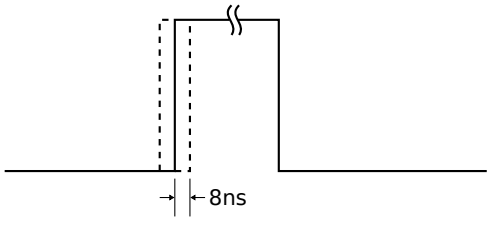


Figure 12: Output pulse jitter

5 Communicating with the CONV-TTL-BLO

It is possible to communicate to the CONV-TTL-BLO remotely via the VME P1 I^2C interface. This section describes how to connect to the VME64x crate and communicate to the board.

5.1 The ELMA I^2C protocol

In order to connect to a CONV-TTL-BLO board in an ELMA VME crate, a higher-level protocol based on I^2C is defined [3]. The protocol uses the serial lines on the VME P1 connector (*SERCLK*, *SERDAT*).

By this protocol, 2^{12} (12 address bits) 32-bit registers can be read from or written to byte by byte. The user accesses the VME crate using Telnet and sends commands which the ELMA SysMon board translates to I^2C transfers to the board.

Two telnet commands (see Table 5) can be used to transfer data to the board. As their names suggest, *readreg* reads a board register, whereas *writereg* writes to a board register.

Table 5: The *readreg* and *writereg* commands

Command	**Description**
writereg *slot reg val*	Writes the value *val* to register number *reg* of board in slot number *slot*
readreg *slot reg*	Returns the value of register number *reg* of board in slot number *slot*

The register numbers are integer numbers starting from one. The actual addresses sent to the board are word-aligned starting from 0x000. For example, *reg 1* translates to address 0x000, *reg 2* to 0x004 and so on. The following relation exists between ELMA *reg* numbers to on-board register addresses:

$$addr = (reg - 1) * 4$$

An example of retrieving the CONV-TTL-BLO ID from *reg 1* of a CONV-TTL-BLO plugged into VME slot 1 of the crate *some-crate* is given

below. If the board is present in slot 1, the command should yield the ASCII string **BLO2**.

```
tstana@tstana-unit:~$ telnet some-crate
Trying 137.138.192.90...
Connected to some-crate.cern.ch.
Escape character is '^]'.
login:user
password:**********
%>readreg 1 1
 Read Data: 424C4F32
%>
```

First, a telnet connection is open with the crate, after which the *readreg* command is issued to read the value of *reg 1* (address 0x000). The value of the register can be confirmed to be the hex value of the ASCII string **BLO2**, so the board is indeed present in the slot.

Another example of running the same command, this time with the board removed from the crate, is given below. As expected, when the board is removed, it can no longer acknowledge the I^2C access, thus the message:

```
Connected to some-crate.cern.ch.
Escape character is '^]'.
login:user
password:**********
%>readreg 1 1
 Not Acknoledged!
%>
```

5.2 Memory map

The memory map of registers accessible through the ELMA protocol is given in Table 6.

Table 6: CONV-TTL-BLO memory map

Address	ELMA reg	Description
0x000	1	Board ID register *access*: R/W *default*: 0x424C4F32 (ASCII **BLO2**)

Appendices

A Getting started with the CONV-TTL-BLO

This section provides a description on testing CONV-TTL-BLO boards for basic functionality. The following steps should be followed in order to test the board.

1. (**Optional**) Plug in a CONV-TTL-RTM board with a CONV-TTL-RTM-BLO piggyback into the rear part of the VME crate.
2. Remove the CONV-TTL-BLO board from its ESD-protecting bag.
3. If TTL or TTL-BAR pulses are to arrive on the front panel inputs, set the TTL switch (SW2.4, see Section 4.2) to the appropriate position:
   - TTL pulses – set the switch to the **ON** position;
   - TTL-BAR pulses – set the switch to the **OFF** position (default).
4. Insert the CONV-TTL-BLO board into the VME crate and power on the crate.
5. Check that the ***PW*** status LED is lit ***green***. If there is no RTM in the rear side of the crate, the ***ERR*** LED will light ***red***. The ***TTL*** status LED should also be lit ***green*** if you set the TTL switch to the **ON** position in the previous step.
6. Input a TTL (or TTL-BAR) signal into a front panel input channel. When a pulse arrives on the input, it is replicated on the output of the same channel. If an RTM board is present in the rear part of the VME crate, the pulse will also be replicated on the three blocking outputs of the same channel on the rear-panel. The channel pulse LED on both the front and rear panels flash briefly when a pulse arrives.
7. (**Optional**) Input a blocking signal on a rear panel channel; the pulse LED of the channel will flash and the pulse will be replicated on the three blocking outputs of the same channel, as well as the TTL channel output on the front panel. If the TTL switch is **OFF**, the pulse is replicated in TTL-BAR.

References

[1] "White Rabbit." http://www.ohwr.org/projects/white-rabbit.

[2] C. G. Soriano, "Standard Blocking Output Signal Definition for CTDAH board," Sept. 2011. http://www.ohwr.org/documents/109.

[3] ELMA, "Access to board data using SNMP and I2C." http://www.ohwr.org/documents/227.

[4] "Conv TTL Blocking webpage on OHWR." http://www.ohwr.org/projects/conv-ttl-blo.

[5] "CONV-TTL-BLO Schematics." https://edms.cern.ch/file/1278535/1/EDA-02446-V2-1_sch.pdf.