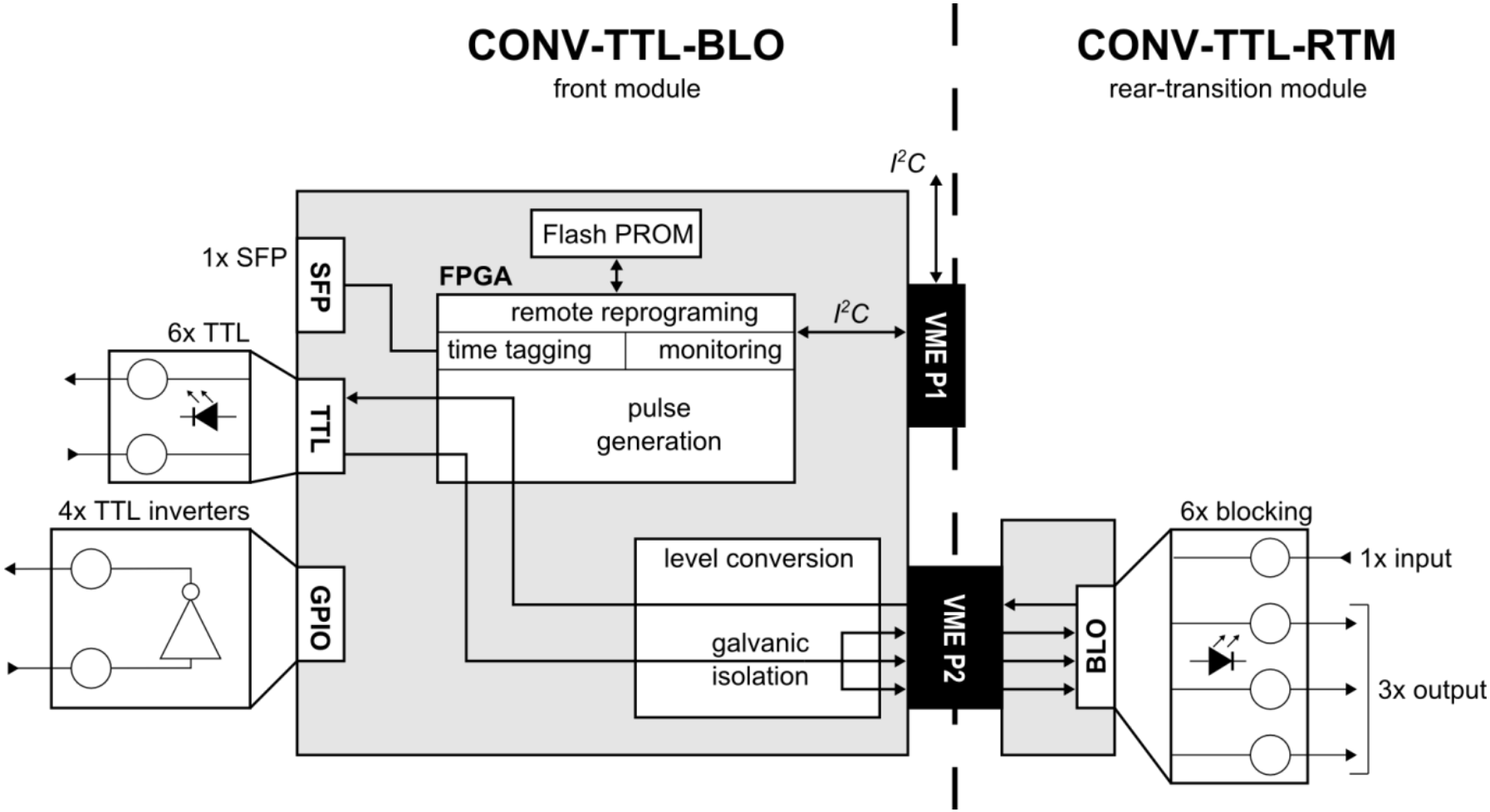
Update and design review

CONV-TTL-BLO

Overview

- Reminder – what the CONV-TTL-BLO is
- Current status
- Future plans
- Design review

Reminder


CONV-TTL-BLO
front module
CONV-TTL-RTM
rear-transition module
I²C
Flash PROM
FPGA
remote reprograming
time tagging
monitoring
pulse
generation
I²C
VME P1
1x SFP
SFP
6x TTL
TTL
4x TTL inverters
GPIO
level conversion
galvanic
isolation
VME P2
BLO
6x blocking
1x input
3x output

Current status – hardware

- Hardware finally mature
  - Thoroughly tested (pulse repetition)
    - Long-term tests in our lab
    - Tested externally by Etienne Carlier
  - PTS for front module
- **23 systems** available
  - Front modules – assembled, tested and ready to use
  - RTMs – 8 fully assembled, 15 w/o the rear panels
- Now in series production
  - **100 systems**
  - Front modules will be tested with PTS in assembly factory in Villaz

Current status – HDL

- Release version 2.0
  - Basic pulse repetition with or without glitch filtering (switch)
  - Remote reprogramming
  - Basic status readout
    - Board there
    - RTM there
    - Switch status
    - f/w version
  - **VBCP (VME Board Control Protocol)**
- Should probably work on version numbering

Future plans

- Hardware
  - PTS for RTM
  - Finish 100 systems production and testing
  - Place in stock for use
  - More testing
    - ESD
    - I^2C behavior while in a 21x crate
- HDL
  - Add further diagnostics features (pulse counters)
  - Add WR support
- Repo cleanup

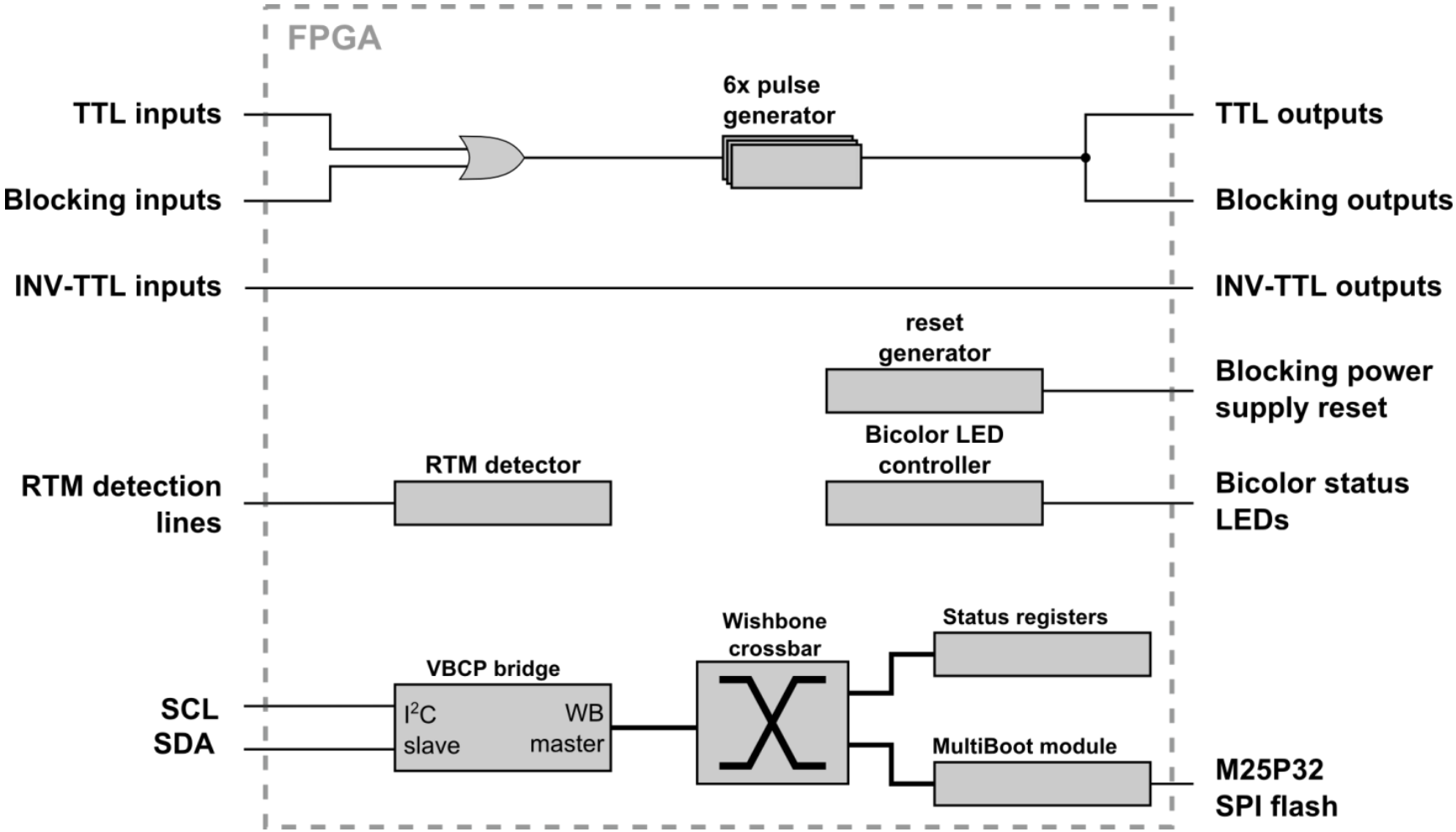
Design review (1)

- Documentation
  - .pdf
    - User guide
    - HDL guide
    - I²C slave
    - VBCP to Wishbone bridge
    - MultiBoot
  - Webpages
    - Main project: http://cern.ch/go/T9Wn
    - Gateware project: http://cern.ch/go/6jX6
    - MultiBoot: http://cern.ch/go/8jDG
    - Releases and children: http://cern.ch/go/Zgm7

Design review (2)

- **Code**
  - **15 files** (2 generated by wbgen)
  - **4020 lines** of VHDL code
    - Including wbgen-generated code

Design review (3)



Design review – folder structure

- ip_cores/
- conv-ttl-blo/ *main proj folder*
  - doc/
    - userguide/
  - conv-ttl-blo-gw/ *gateware sub-proj*
    - doc/
      - hdlguide/
      - <modules in own folder>
    - hdl/
      - <module folders>

Design review – get started

- Clone conv-ttl-blo repo
- Get the g/w subproject
  - git submodule init
  - git submodule update
- For the g/w folder structure, check the chapter in the HDL guide (*conv-ttl-blo-gw/doc/hdlguide/*)

Design review – organizational

- Deadline: **13.11.13** (two weeks)
- How to do it
  - Text files with the feedback
  - Repository branch
  - Send by mail