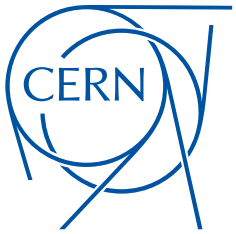
CONV-TTL-RS485 Hardware Guide

Decembre 21, 2017



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Revision history

Date	Version	Change
21-12-2017	1	*D. Bouhired* First draft

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List of Abbreviations

FPGA	Field-Programmable Gate Array
RTM	Rear-Transition Module
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit (bus)
PLL	Phase-Locked Loop
RTM	Rear Transition Module
SFP	Small-Form-factor Pluggable (transceiver)
TVS	Transient Voltage Suppressor (diode)
SVEC	Simple VME FMC Carrier
SPEC	Simple PCIe FMC Carrier
VME	Versa Module Eurocard

1 Introduction

This document explains in detail the hardware of the TTL to RS485 converter system (Figure 1). A full pulse conversion system consists of three distinct boards:

- CONV-TTL-RS485 – active front module, containing the circuitry necessary to achieve all functionality of the system
- CONV-TTL-RTM – passive rear-transition module (RTM) motherboard, providing the connections from the CONV-TTL-RS485 VME P2 connector to the rear panel
- CONV-TTL-RTM-RS485-DB9 - piggyback board on the RTM, providing the D-Sub9 connectors, pulse LEDs, and the screws to fix the rear panel. It can repeat on 2 channels (CH1 and CH2), with 1 input and 5 outputs for each one of them
- CONV-TTL-RTM-RS485-OPT - Active rear-transition module (RTM), plugging directly onto the CONV-TTL-RS485 VME P2 connector. It provides optical connectivity with ST connectors, pulse LEDs, and the screws to fix the rear panel. It can repeat on 3 channels (CH1 and CH2), with 1 input and 2 outputs for each channel

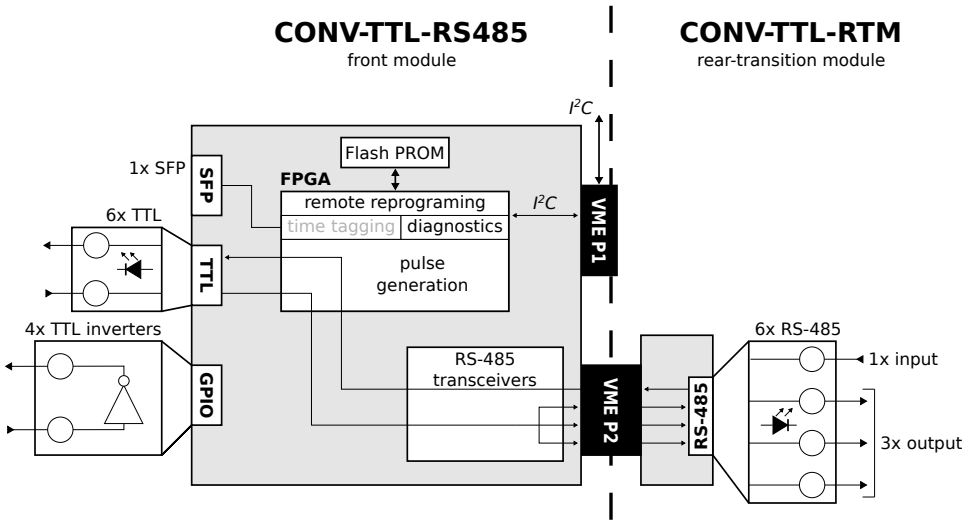

Figure 1: TTL to RS485 pulse conversion system

The CONV-TTL-RS485 can be used standalone without any RTM, if no RS485 or optical pulse replication is needed. This board contains all active circuitry needed to implement the functionalty of the system, from

RS485 or TTL pulse detection and generation, to communication over I^2C and time-tagging via White Rabbit [1].

An RTM system usually (but not always, in the case of the optical RTM) consists of both motherboard and piggyback and provide the connections to input RSD485 pulses to the CONV-TTL-RS485.

Note that, as the optical RTM design is more involved, it is more fully described in its own documentation. As this RTM converts RS485 from the P2 connector to optical signals, and input on its optical receivers, to RS485 signals, this document will only focus on TTL conversion to and from RS485. Optical conversion will not be further discussed in this document)

1.1 Additional documentation

- CONV-TTL-RS485 OHWR Project Page [2]
- CONV-TTL-RS485 Schematics on CERN EDMS [3]
- CONV-TTL-RTM-RS485-DB9 Schematics on CERN EDMS [4]
- CONV-TTL-RS485 User Guide [5]
- CONV-TTL-RS485 HDL Guide [6]

2 Front module

A block diagram of the CONV-TTL-RS485 front module is shown in Figure 2. The board contains all active circuitry needed within a converter system. The various blocks in Figure 2 are presented in subsections that follow.

The schematics of the CONV-TTL-RS485 board can be found at [3].

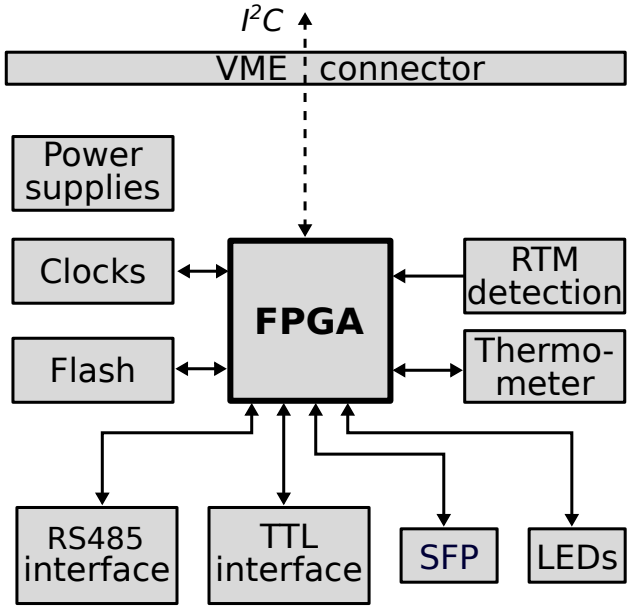

Figure 2: Block diagram of CONV-TTL-RS485 board

2.1 VME connector

Schematics: page 5

The VME backplane consists in two connectors, P1 and P2. The following connections provided by the P1 connector are used on the CONV-TTL-RS485:

- the VME power supply pins (3.3 V and 5 V)
- *SERCLK* and *SERDAT* pins, for I^2C communication
- the geographical addressing pins, also necessary for I^2C communication
- the active-low system reset line, connected to the FPGA for resetting the logic implemented therein

Serial communication lines, geographical addressing lines and the system reset line are isolated from the FPGA by means of a Texas Instruments SN74VMEH22501DGGR bus transceiver. Their use is based on the SVEC design [7] and is due to their compatibility to the VME standard.

Apart from the bus grant and IACK lines, which are daisy-chained, the rest of the VME signals are not used on the CONV-TTL-RS485 board.

The user-defined part of the P2 connector is used for carrying signals from the CONV-TTL-RS485 to the RTM. The following signals are routed via the VME P2 connector:

- RS485 input signals (Section 2.6.1)
- RS485 output signals (Section 2.6.2)
- RTM detection and rear panel pulse LED signals (Section 2.9)

2.2 Power supplies

Schematics: pages 2, 3

Three power levels are needed on the CONV-TTL-RS485 board. They are listed in Table 1. All power supplies on the board are derived in some way from the 3.3 V and 5 V VME power supplies.

Table 1: Voltage levels on CONV-TTL-RS485

Level	Description
1.2 V	Low-voltage power supply for the FPGA logic
3.3 V	V_{CC} for most of the devices on the board
5 V	Power supply for some circuits on-board (Eg: TTL input and output stage)

First, the 5 V and 3.3 V VME supplies arriving on the VME connectors are filtered using two PI filters (schematic page 2). These filters assure noise immunity in the 50 MHz to 150 MHz band. The filtered power supplies are used throughout the logic.

The 1.2 V logic power supply is generated by a Texas Instruments TPS54312PWP Buck converter. This circuit can be found in page 2 of the schematics.

2.3 Clock circuits

Schematics: page 4

There are multiple clock signals on the CONV-TTL-RS485 (Table 2). A 20 MHz clock for the FPGA is generated directly from a tunable VCXO (OSC3). The second FPGA clock is a 125 MHz signal generated from a 25 MHz VCXO by means of a Texas Instruments CDCM61004RHBT PLL IC. Two of the other PLL's output channels are used to output dedicated 125 MHz dedicated clocks to the SFP and FPGA transceiver.

Table 2: Clocks on CONV-TTL-RS485

Clock	Frequency	Description
CLK20_VCXO	20 MHz	FPGA clock (from VCXO)
FPGA_CLK	125 MHz	FPGA clock (from PLL IC)
SFP_CLK	125 MHz	Dedicated SFP clock
FPGA_MGT_CLK	125 MHz	Dedicated clock for FPGA transceiver

Both VCXOs can be tuned by means of two Analog Devices DACs (IC17 and IC18), that can be controlled by the FPGA via a 3-wire SPI interface.

The 3.3 V power supply used by ICs on the clock generation part is a cleaner version of the board-wide 3.3 V supply. The cleaning is done by a four-pole LC filter.

The design of the clock circuits is based on the SPEC board design [8].

2.4 FPGA

Schematics: page 3

A Xilinx XC6SLX45T Spartan-6 FPGA is present on the CONV-TTL-RS485 board. It is the core part of the conversion system, since it is the device controlling all the components on the board.

The intended functionality of the FPGA is:

- generating output pulses as response to input pulse
- pulse logging
- clock conditioning
- remote reprogramming
- controlling the various panel LEDs to inform the user either of pulse arrival, or the status of the system.

For more details on the FPGA firmware and functionality, refer to the CONV-TTL-RS485 HDL Guide [6].

2.5 TTL pulse repetition

Schematics: page 7

TTL and TTL-BAR pulses may arrive on front panels of CONV-TTL-RS485 boards. The two signal types are described in Sections 4.1 and 4.2 of [5]. Signals arriving on an input channel go through an input stage consisting of Schmitt trigger circuits; they are then input to the FPGA, where the pulse gets regenerated and passed to the output stage.

2.5.1 TTL input stage

The input stage on a TTL pulse channel is shown in Figure 3. Pulses go through a Texas Instruments SN74LVC14AD Schmitt trigger inverter which isolates the FPGA from the channel input. The inverter is 5 V tolerant at the input, so TTL signals may be up to 5 V high. Anything above 5.6 V opens the BAR66 diode to the 5 V and protects the Schmitt trigger.

The input stage is 50 Ω terminated (the three 150 Ω resistors in parallel). Note that when no wire is plugged into the LEMO connector, the termination pulls the line low which becomes a continuous high-level when it comes out of the Schmitt trigger.

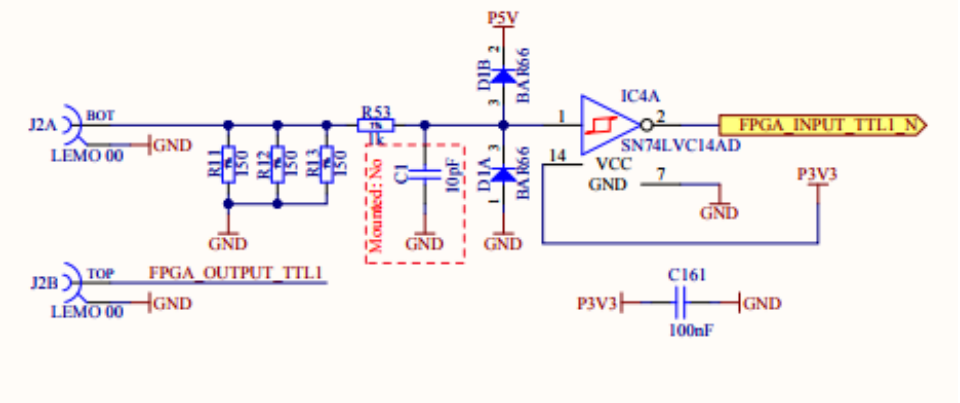

Figure 3: TTL pulse input stage

This input stage is repeated on each of the six TTL pulse replication channels of the CONV-TTL-RS485, as well as the four inverter channels.

2.5.2 TTL output stage

The output stage (Figure 4) consists of Texas Instruments SN64BCT25244DW tri-state buffers driven by the FPGA. These buffers assure a high-impedance output on startup and assure the line can drive a 50 Ω load. Pull-down resistors at the output of the tri-state buffers assure a continuous low level at

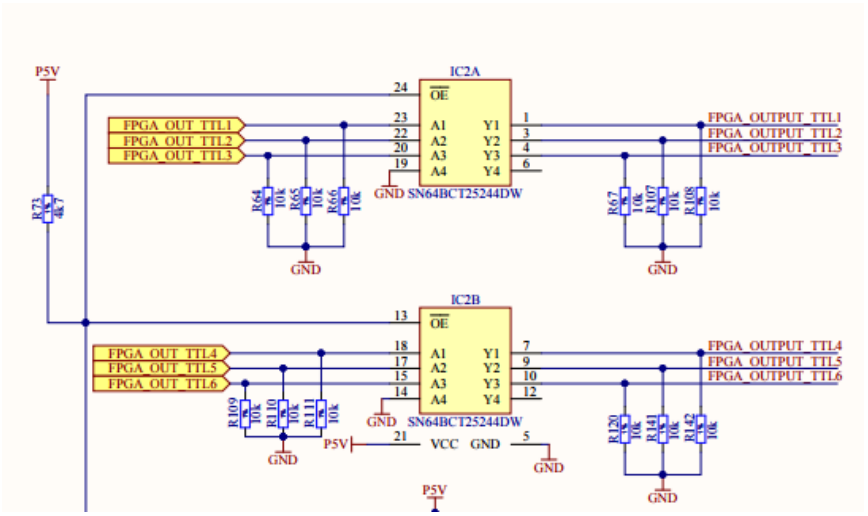

Figure 4: TTL pulse output stage

the output when the buffers are not enabled. Combined with the guaranteed tri-state output on startup, these resistors assure a continuous low-level at the output on startup.

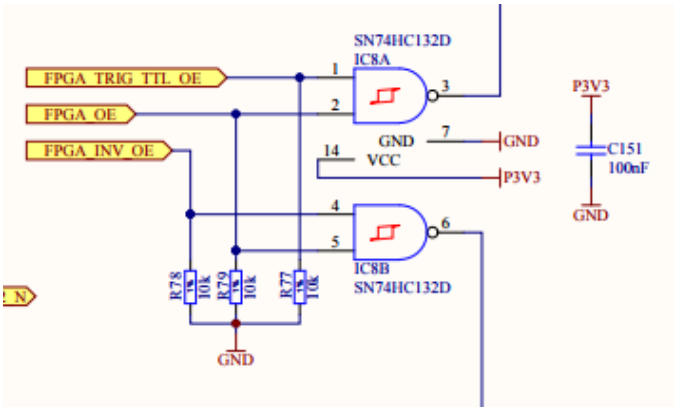

Figure 5: TTL pulse output enable signals

The buffers' enable signals are controlled by two signals from the FPGA. These signals are NANDed together (IC8 NAND gate, see Figure 5) and connected to the output enable active-low signals. When the FPGA does not drive the output enable line, it is pulled high by a pull-up resistor, to safeguard against spurious signals on the output of the channel.

2.6 RS485 pulse repetition

Schematics: pages 9-12

RS485 pulses are handled through the P2 connectors on the VME backplane (These are effectively coming from the DB9 connectors on the rear panel of the CONV-TTL-RTM-RS485-DB9, or converted from the optical input of the optical RTM).

They arrive at the RS485 input stage on the CONV-TTL-RS485 and each has a dedicated RS485 transceiver. Similarly the RS485 output is the result of the same transceiver taking TTL pulses coming from the FPGA and converting these to an RS485-compliant pair. During the PCB layout process, care has been taken to route these RS485 pairs in full differential mode.The pairs have differential impedance of 100 Ω.

2.6.1 RS485 input stage

Schematics: pages 9-10

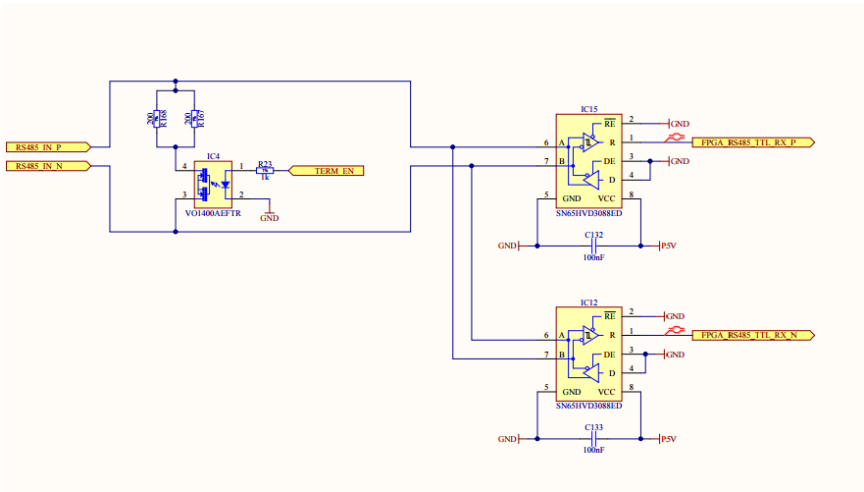

Figure 6: RS485 pulse input stage

Texas instrument's SN65HVD3088ED [9] was selected after several other solutions were considered [10]. It is is a low-power, half-duplex RS485 device, that is one of the fastest on the market (20Mbps).

The input stage uses two RS485 transceivers for each channel, as shown in Figure 6. This was added in order to implement a monitoring function on the state of the input link.

A low level differential signal can be interpreted in several ways:

- No cable is not connected
- The link is experiencing a lot of attenuation

- A DC supression device, such a transformer, has been connected TO the link.

The SN65HVD3088ED datasheet [9] shows that the input differential thresholds $V+_{in}$ and $V-_{in}$ are both negative. By connecting receivers with the differential pins swapped a voltage range between $[-V-_{in}, V-_{in}]$ can be defined in which a fault detection can be issued by ANDing the R pins of the two receivers (this is performed inside the FPGA). Further information can be found in this technical document from Texas Instruments [11].
The input stage also offers optional input termination. This is activated by one of the dip switches present on the board (see Section 3 of [5]). This input termination signal is then used to engage a solid state relay (The VO1400AEFTR), thereby enabling the 100 Ω termination. This relay can also be seen on Figure 6.

2.6.2 RS485 output stage

Schematics: pages 11-12

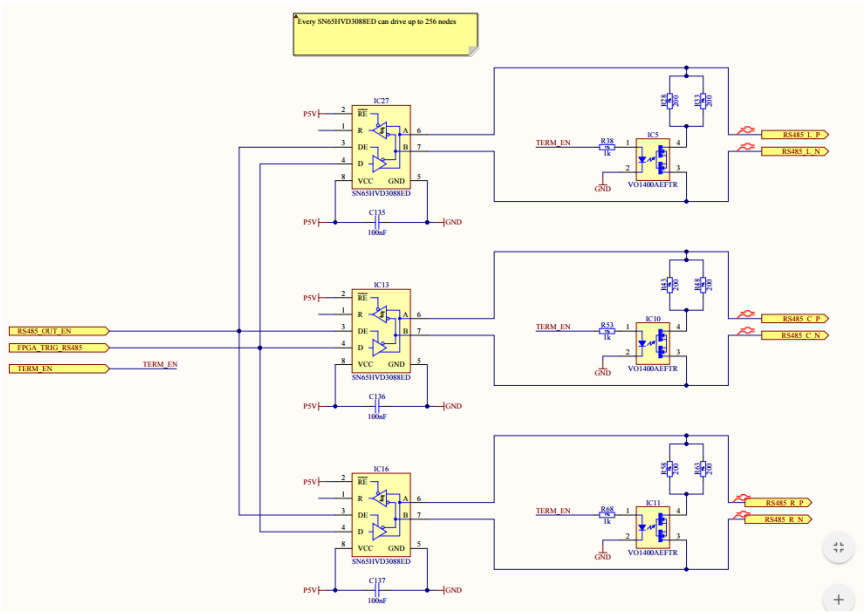

Figure 7: RS485 pulse output stage

Each RS485 output for each channel has its dedicated transceiver capable of driving 256 nodes. Additionally, each output channel has a selectable 100 Ω termination, which can be enabled by the output termination switches (see Section 3 of [5]). Setting the input or output termination enable switch to the ON position enables a connection via a solid-state relay, just as in the

input stage, which in turns enables the termination connection as shown in Figure 7.

Note that the motherboard has been designed to offer 6 RS485 channels, each with 1 input and 3 outputs. This effectively means that one RS485 chip is used for each output port, a maximum of three per channel. Since the CONV-TTL-RTM-RS485-DB9 board only implements 2 of the possible 6 channels, and since it can offer up to 5 outputs per channel, more transceivers were therefore required for a single channel. To accomplish this, and only when this particular RTM is recognised by the FPGA in the front module (Through the RTM detection lines), RS485 transceivers from unused channels are called upon to process the 2 additional inputs per channel. This operation is performed by the FPGA, which copies signals to the desired ports, allowing the re-use of hardware resources.

2.7 SFP connector

Schematics: page 6

The small form-factor pluggable (SFP) connector on the CONV-TTL-RS485 front panel can be used to input an optic fiber cable that may be used for pulse time-tagging using White Rabbit.

2.8 Thermometer and flash chip

Schematics: page 13

A DS18B20U+ thermometer chip is provided on board. This chip can be used to provide a unique ID for the board and measure on-board temperature. It communicates to the FPGA via a Dallas one-wire interface and is powered from 3.3 V.

The Flash chip on-board is used to store FPGA configuration data. It is a Macronix MX25L3233F SPI Flash memory chip with 32 Mbits storage capability.

2.9 RTM detection

Schematics: page 5

The RTM detection circuitry is shown in Figure 8. It works by connecting the RTM motherboard or piggyback detection lines to ground, based on the motherboard or piggyback used. Lines not connected to ground are pulled up to V_{CC} by the pull-up resistor, which yields a low value after the Schmitt triggers. The outputs of the Schmitt triggers are connected directly to the FPGA inputs.

An up-to-date list of boards and their RTM detection line connections can be found at [12].

2.10 Status and pulse LEDs

Schematics: page 8

The circuit for driving the bicolor status LEDs is based on the SVEC design [7]. It consists of the same Texas Instruments SN74VMEH22501DGGR bus buffer chip used for buffering the VME signals. The control and data lines of the chip are driven by logic within the FPGA, which controls lighting of each of the LEDs. An example of how the LEDs can be driven using the FPGA is given in Section 5 of [6].

TTL (front panel), INV channels (front panel) and rear panel pulse LEDs are driven by the FPGA via a SN7414 Schmitt trigger. In the case of the RTM LEDs, the output of the Schmitt trigger is connected directly to the

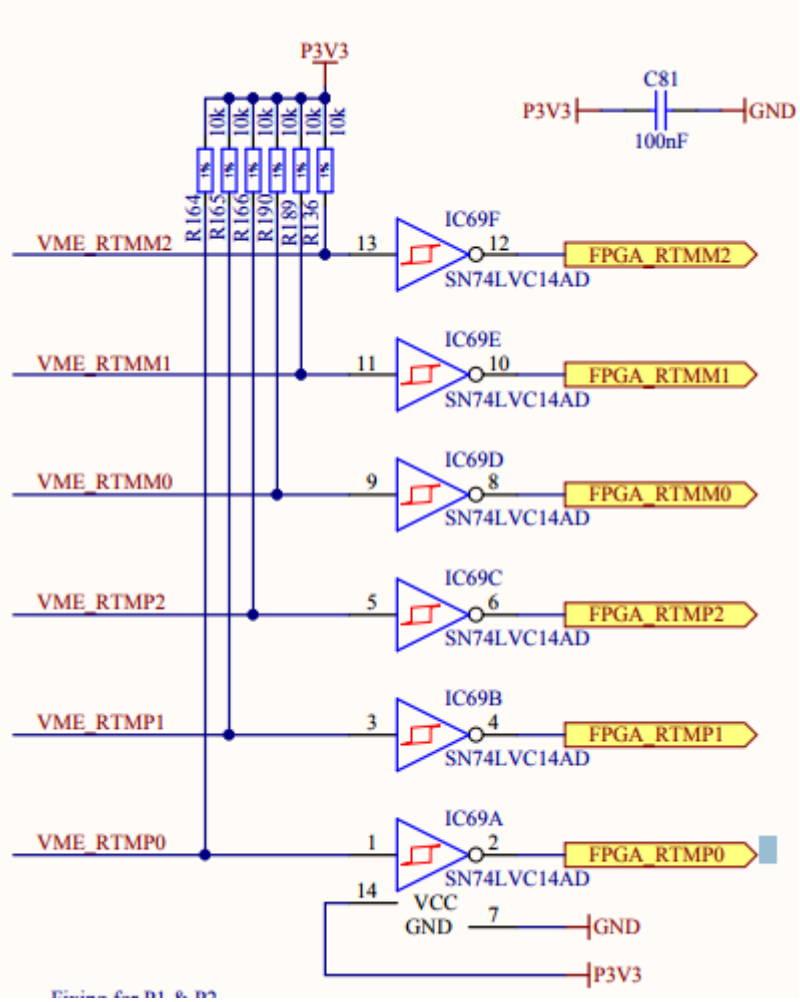

Figure 8: RTM detection circuit

VME P2 connector and through the RTM to the piggyback, where the current-limiting resistor and the LED are located.

2.11 PCB version

The PCB version is necessary to the operation of the burst mode. Indeed the FPGA reads out the hardware version, and depending on whether the board is v4 and later or v3 earlier, will enable or disable this functionality accordingly. The PCB version is provided to the FPGA via a resistor network offering 4 bits for the version number and 2 bits for potential revisions. The circuit is shown in Fig. 9.

Board version can be read as 4 bits, 1s when the resistors are pulled up, 0s when they are pulled down. Board revision is available in 2-bits, read-out

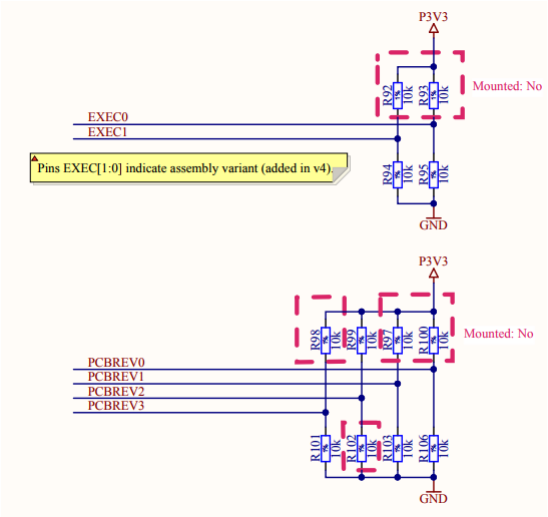

Figure 9: Hard-wired PCB versioning

in the same way. For example, Fig. 9 shows a v4.0 board. Note that PCB identification is not available in boards v3 and earlier, and therefore will be read as all zeroes in the FPGA.

3 Rear-Transition Module

Rear transition modules (RTMs) are located on the rear side of the VME crate. An RTM in TTL to RS485 converter systems is made up of two boards, the motherboard and the piggyback, containing only passive components. The two boards are detailed in the next subsections.

3.1 RTM Motherboard

The CONV-TTL-RTM motherboard [13] is the interface between the VME P2 connector and the RTM piggyback board. It provides a female connector to the VME backplane P2 connector and links the RS485 and pulse LED signals from the CONV-TTL-RS485 to the piggyback via a 100-pin connector.

RTM motherboards are used in both CONV-TTL-BLO [**?**]ctb-proj) and CONV-TTL-RS485 systems, with different piggybacks.

The motherboard also contains 47 V transient voltage suppressor (TVS) diodes that inhibit high-voltage pulses arriving on piggyback LEMO connectors. The first two production versions have the 100 nF capacitor soldered on top of these TVS diodes, as shown in Figure 10. These were added to resolve the common-impedance coupling problem [14] that was observed when these were connected to CONV-TTL-BLO [**?**]ctb-proj). These capac-

itors are not required for CONV-TTL-RS485 applications, and needn't be discussed further in this document.

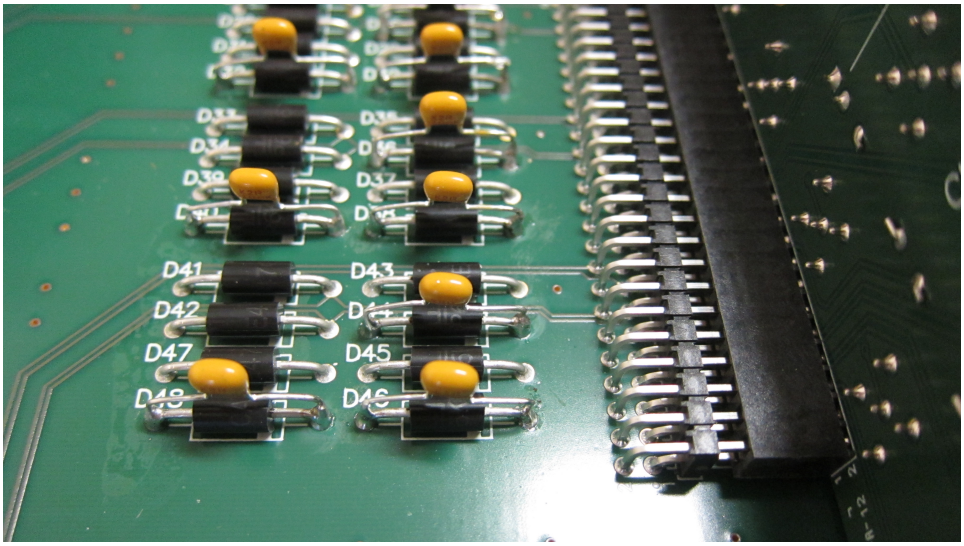

Figure 10: Capacitors straddled on the TVS diodes on some RTMM cards

3.2 RTM Piggyback

The CONV-TTL-RTM-RS485-DB9 piggyback [4], provides the actual connectors on rear panels of TTL to RS485 converter systems.

On each of the two RS485 channels, there are six female D-sub9 connectors (one input and five outputs) and one LED together with its corresponding current-limiting resistor. The connections for each of the DB9 connectors and LEDs are made via the 100-pin male connector, through the RTM motherboard and to the CONV-TTL-RS485. Note that a CONV-TTL-RS485 RTM can support up to 6 repetition channels. This is the case for, the functional but now unsupported design, of the LEMO 2-pin version of the RTM piggyback [15]. However, since this card will be used at CERN for timing signal distribution, it became clear the requirement for single signal fanout was more important than a multi-channel capability. It was therefore decided to use the limited space on the rear panel to increase the number of output ports per channel, while reducing the number of independent channels.

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[6] C. BE-CO-HT, "CONV-TTL-RS485 HDL Guide." http://www.ohwr.org/documents/?, 12 2017.

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