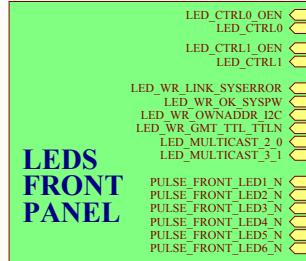


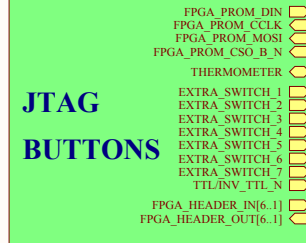
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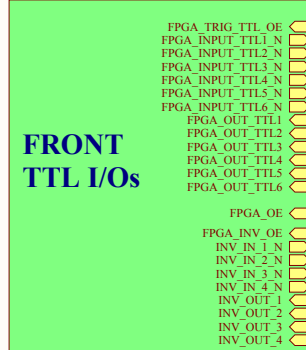
U_FrontPanelLeds
FrontPanelLeds.SchDoc



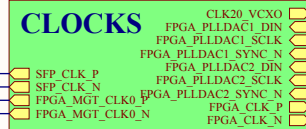
U_JTAG&Button
JTAG&Button.SchDoc



U_FrontTTL
FrontTTL.SchDoc



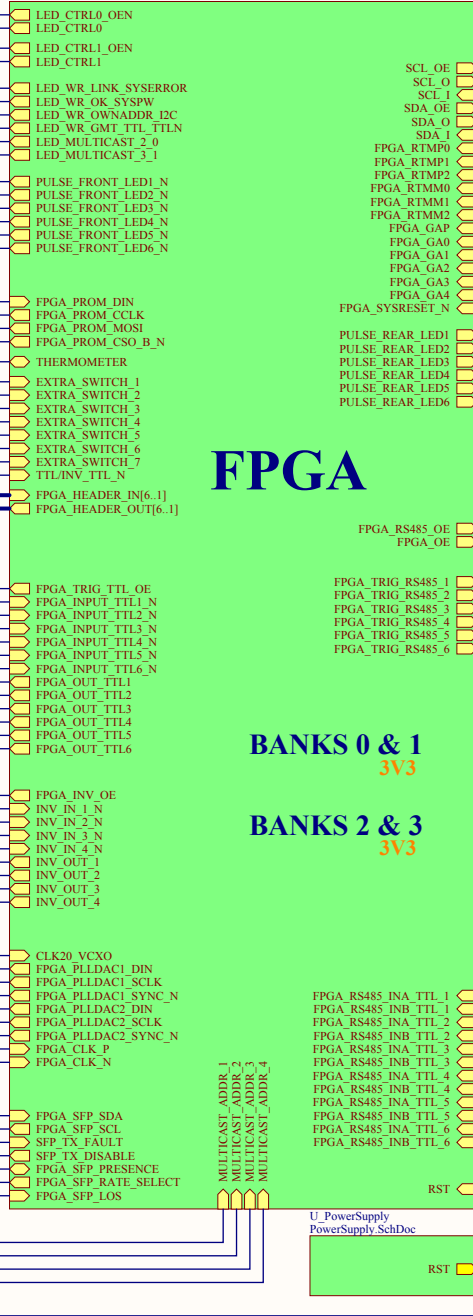
U_Clocks&Monitor
Clocks&Monitor.SchDoc



U_Communication
Communication.SchDoc



U_FPGAbank
FPGAAbank.SchDoc



FPGA

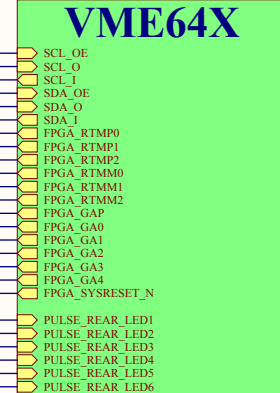
BANKS 0 & 1
3V3

BANKS 2 & 3
3V3

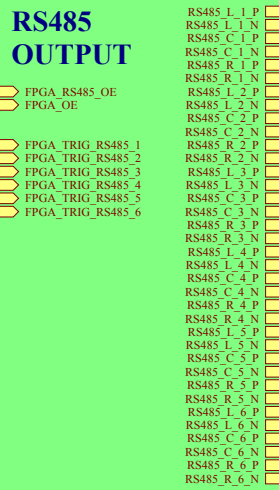
U_PowerSupply
PowerSupply.SchDoc



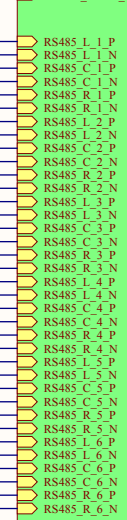
U_VME64xConn
VME64xConn.SchDoc



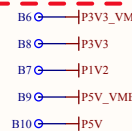
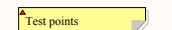
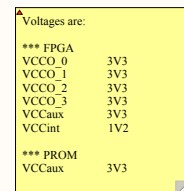
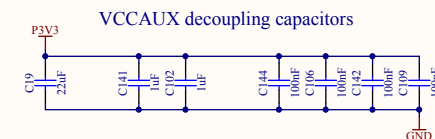
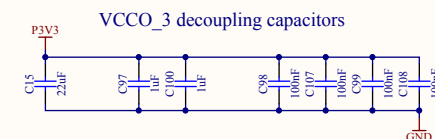
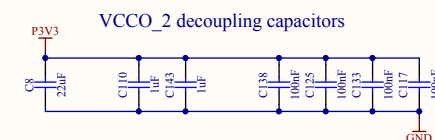
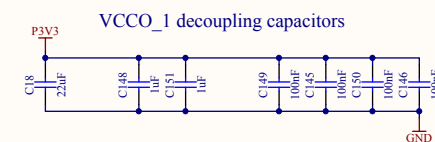
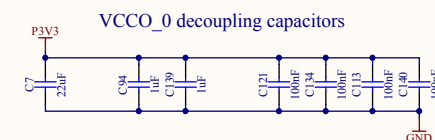
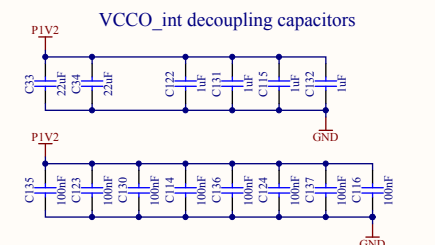
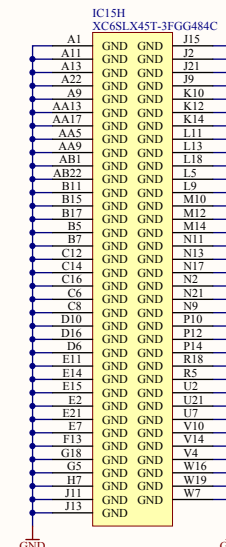
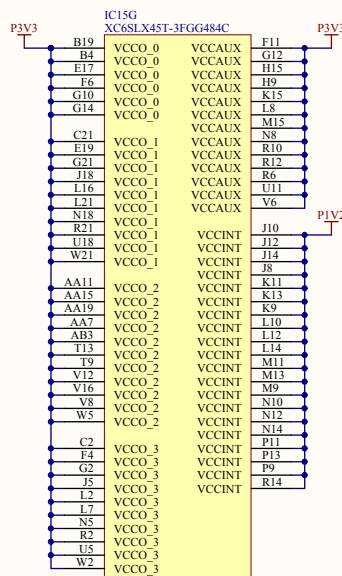
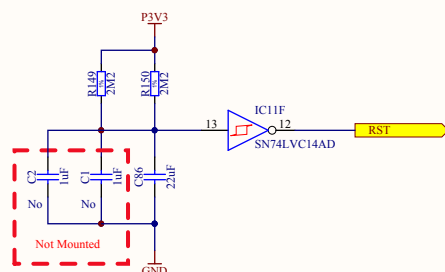
U_Output RS485
Output RS485.SchDoc



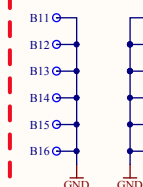
U_Input RS485
Input RS485.SchDoc



Project/Equipment *		Document		Designer: Carlos Gil Soriano	12/03/2012
BE-CO		CONV-TTL-RS485 TOP		Drawn by: Carlos Gil Soriano	14/08/2012
CERN		European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Check by: B. Recordon	14/08/2012
				Last Mod. -	14/08/2012
				File: convTTLrs485_TOP.SchDoc	
				Print Date: 14/08/2012 17:26:17	Sheet 1 of 13
		EDA-02541-V1-0		A3	5



Mounted: No

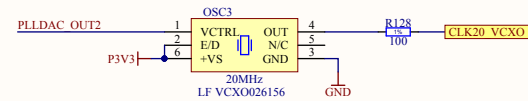
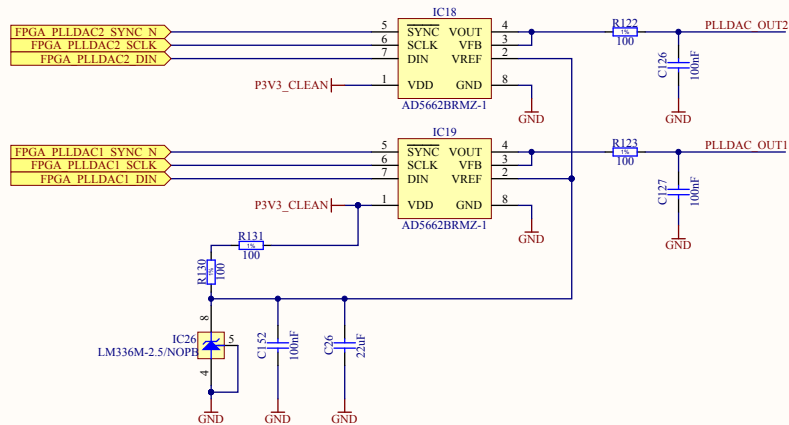


Nearby VME P2 RS485 inputs

Nearby Front Panel

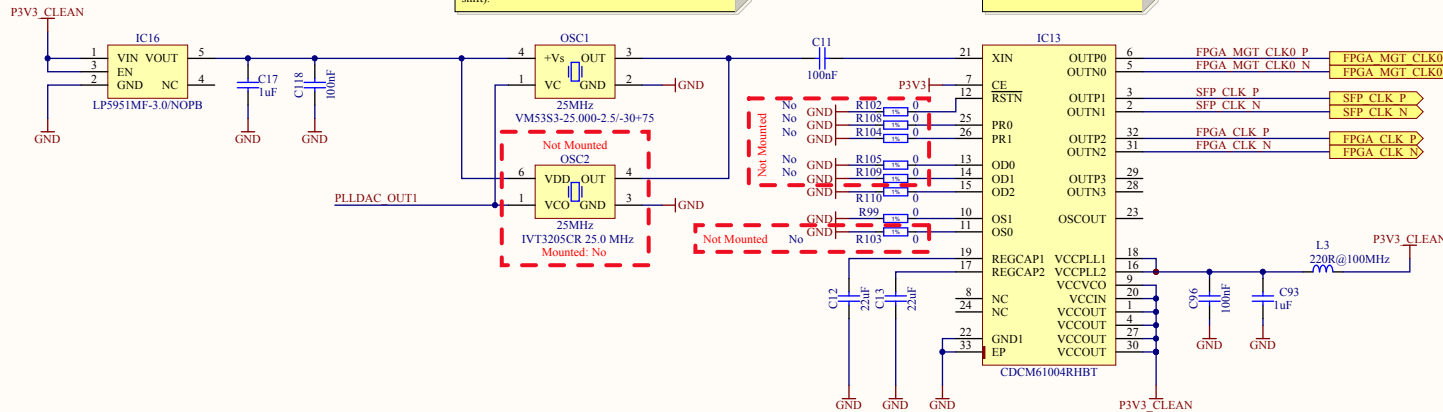
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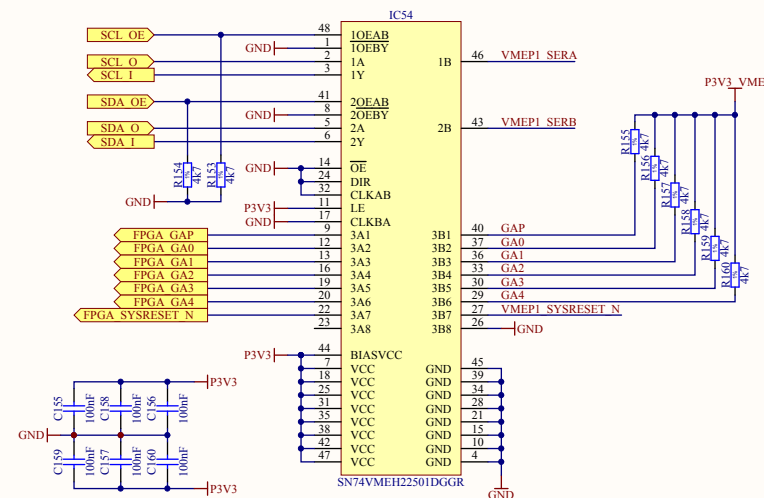
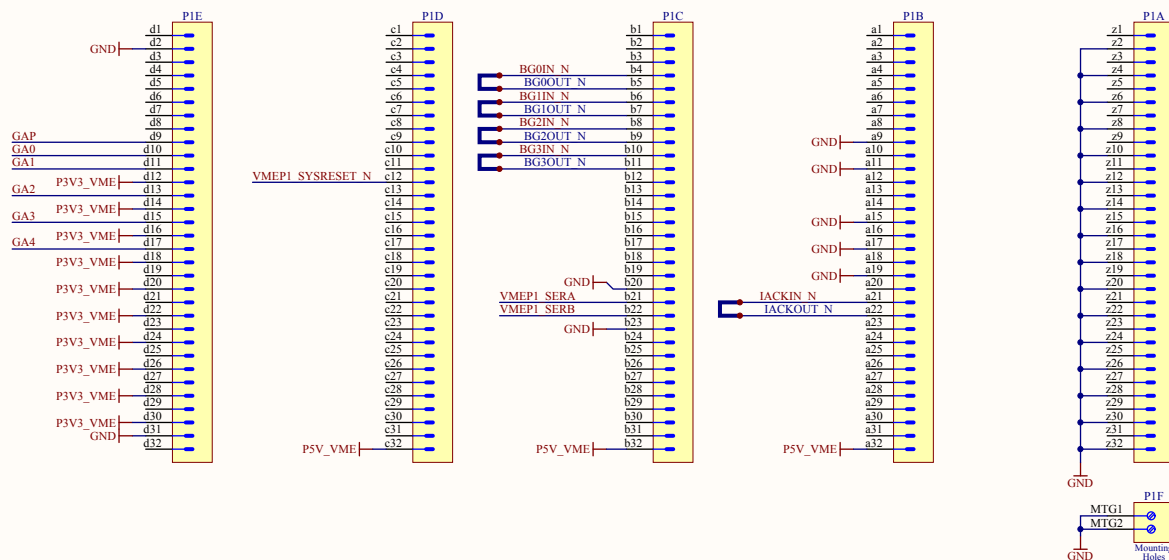
DAC Vih = 2V so it accepts 2.5V CMOS signal
DAC output range: 0V to 2.5V



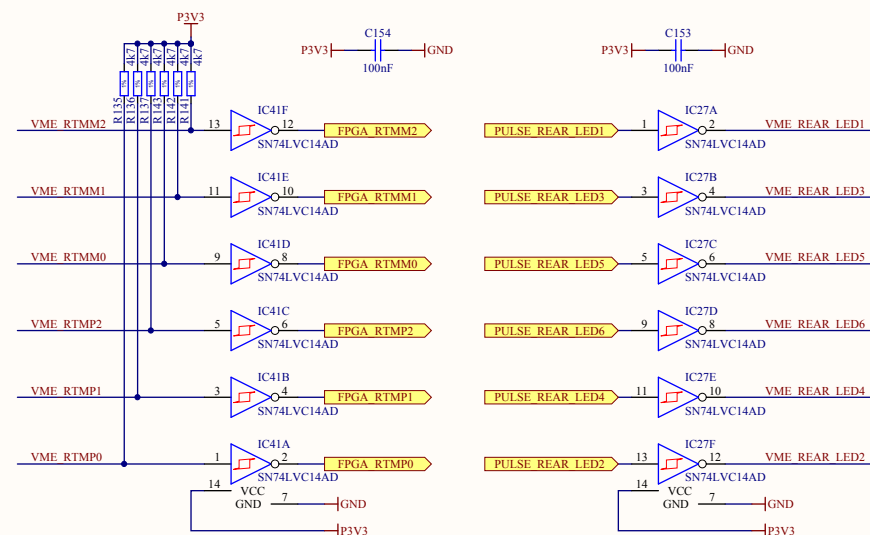
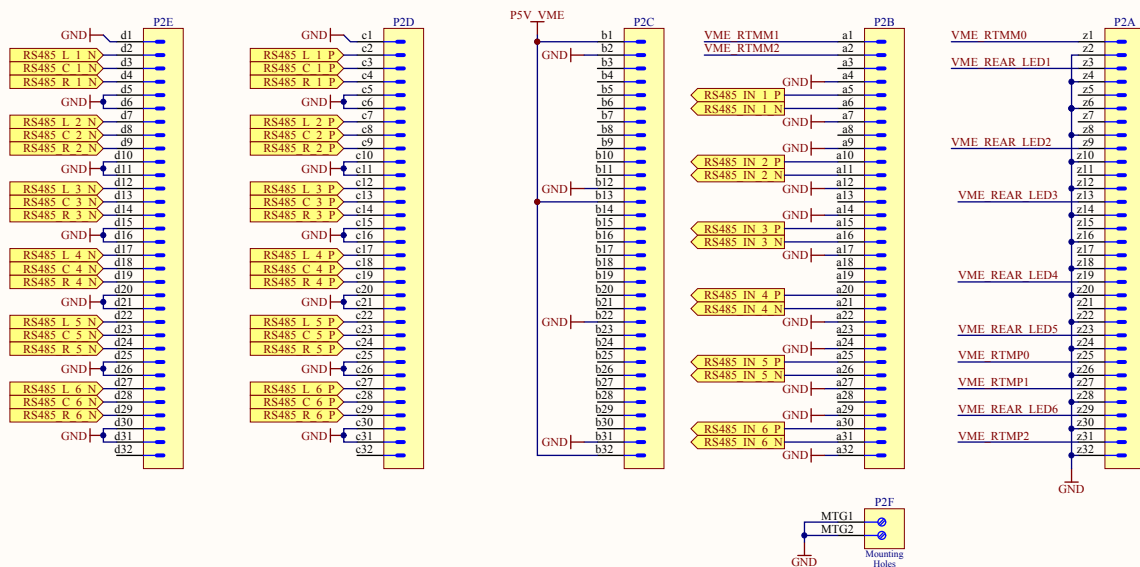
*CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.
Input = 25 MHz
Output = 125 MHz

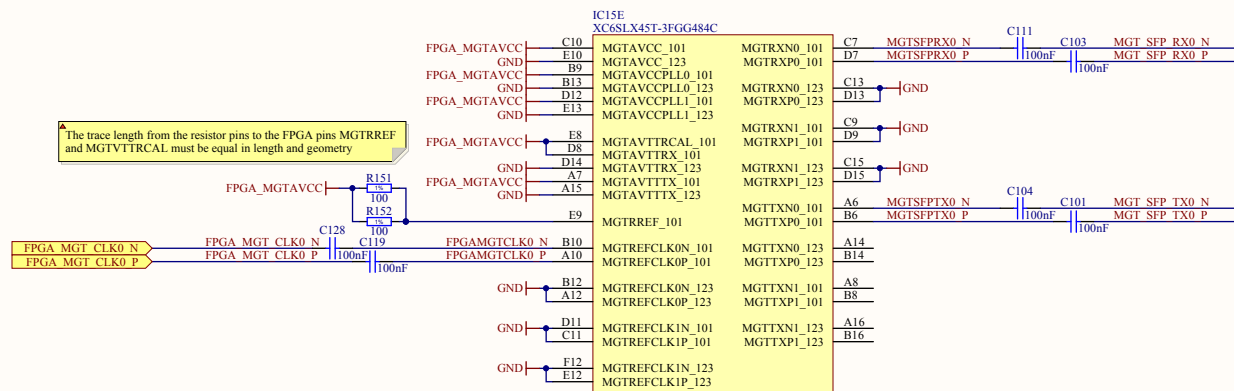
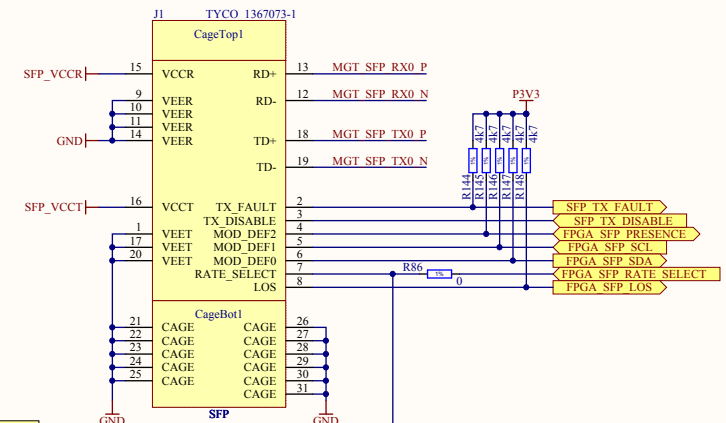
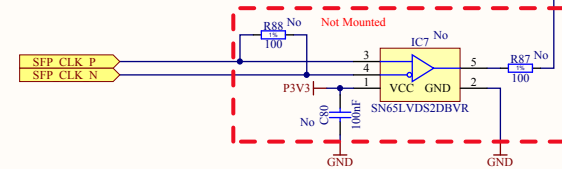
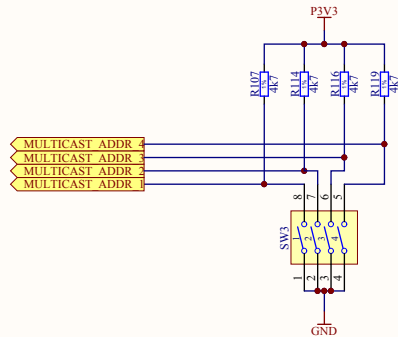
Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).

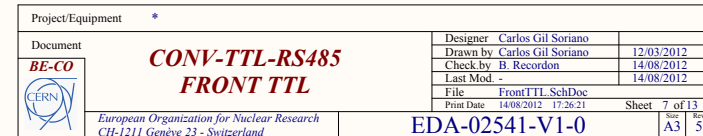




As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used. Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

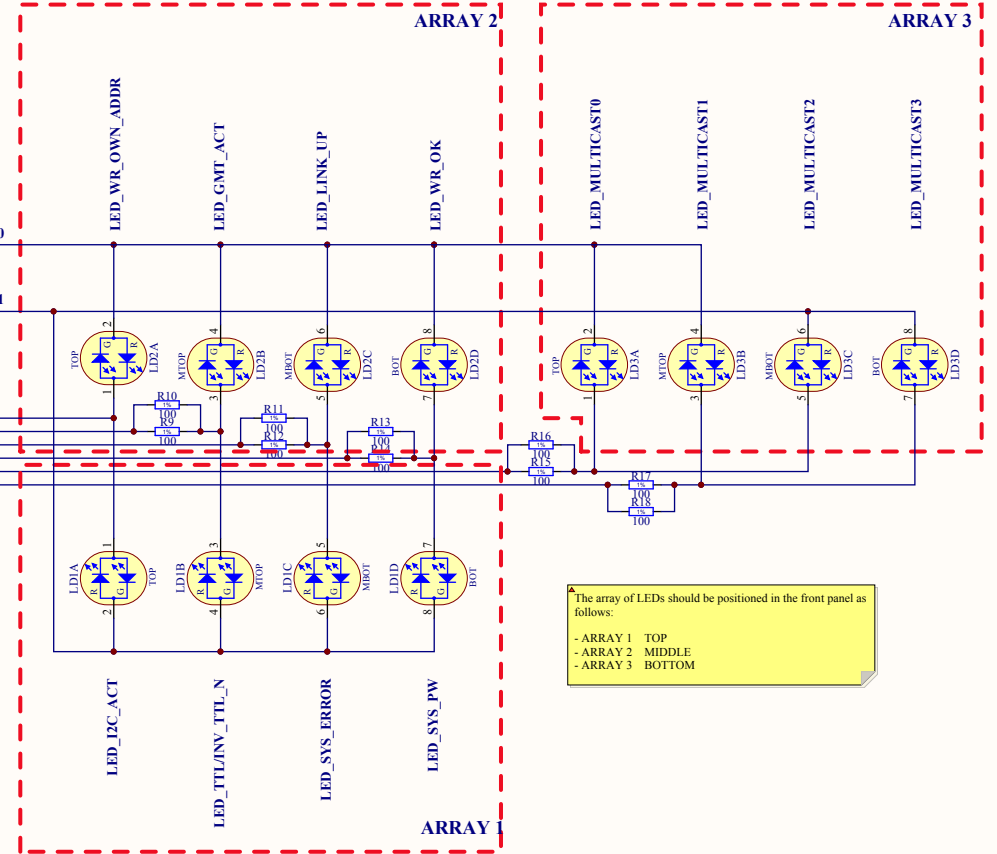
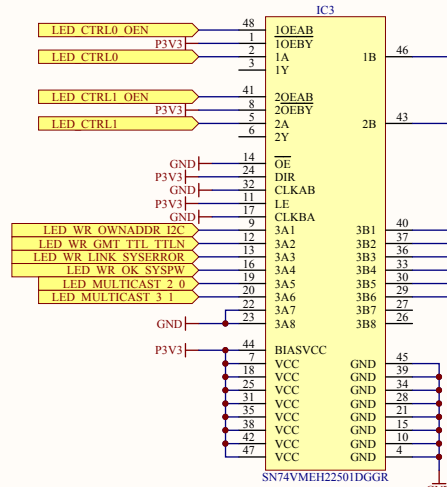
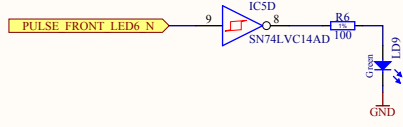
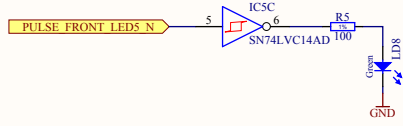
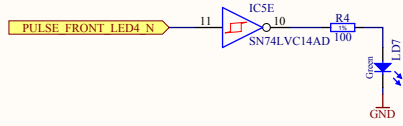
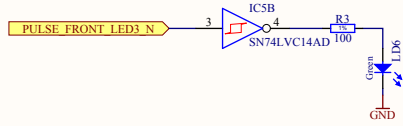
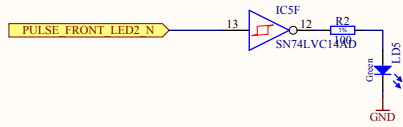
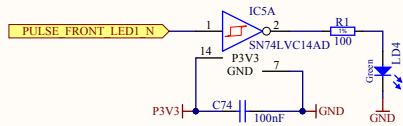






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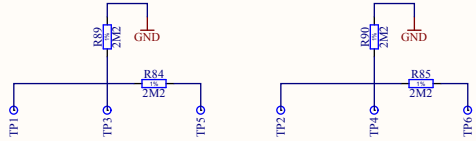
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The array of LEDs should be positioned in the front panel as follows:

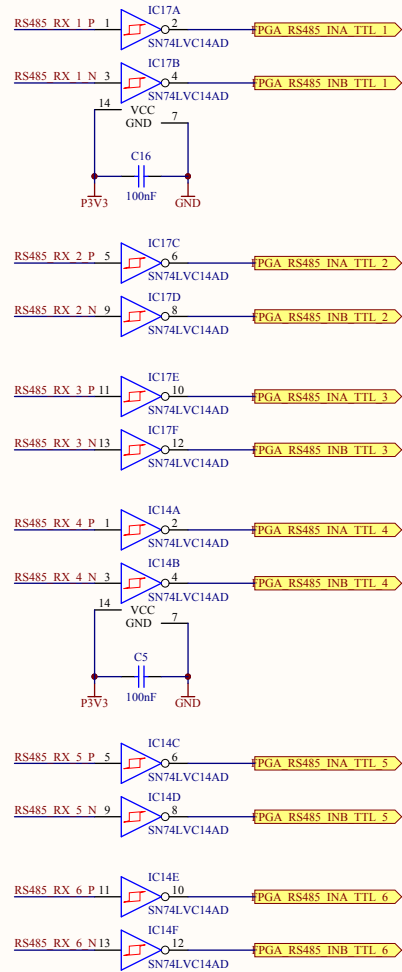
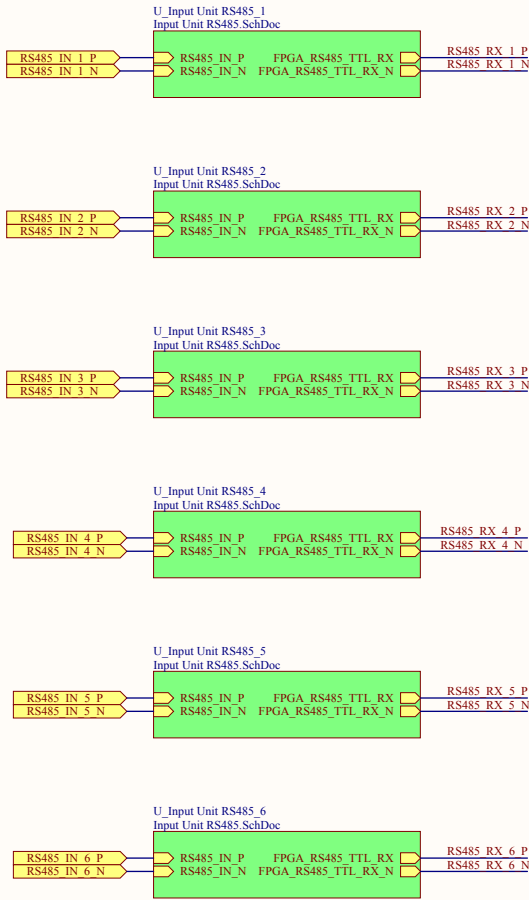
- ARRAY 1 TOP
- ARRAY 2 MIDDLE
- ARRAY 3 BOTTOM

ESD discharge strips (top and bottom of the card)



Project/Equipment *		Document		Design	
BE-CO		CONV-TTL-RS485		Front PANEL	
CERN		European Organization for Nuclear Research		CH-1211 Geneva 23 - Switzerland	
Print Date		14/08/2012 17:28:22		Sheet 8 of 13	
File		FrontPanelLedsSchDoc		Rev A3	
Last Mod.		14/08/2012		Rev 5	
Designer		Carlos Gil Soriano		12/03/2012	
Drawn by		Carlos Gil Soriano		14/08/2012	
Check by		B. Recordon		14/08/2012	

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Document	Designer	Carlos Gil Soriano	CreateDate
	Drawn by	Carlos Gil Soriano	14/08/2012
	Check by	B. Recordon	14/08/2012
	Last Mod.	-	14/08/2012
CERN	File	Input RS485 SchDoe	
	Print Date	14/08/2012	17:26:22
	Sheet	9 of 13	Size A3 Rev 5
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02541-V1-0	

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Extra functionality: DETECTION OF LOW DIFFERENTIAL SIGNAL

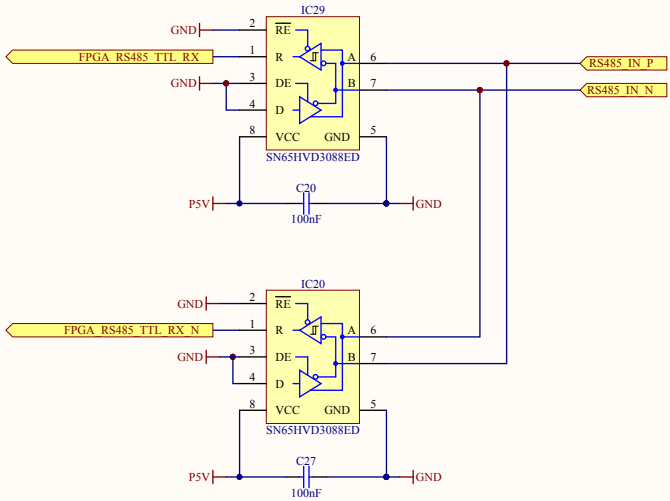
This extra feature can be used to monitor whether the input link is alive. Having not enough differential signal can be interpreted in several ways:


- We are experiencing a lot of attenuation in the link
- Cable is not connected
- DC supression device, such a transformer, has been connected in the link.

HOW TO IMPLEMENT

First, a glance to the SN65HVD3088ED shows that the input differential thresholds V_{+in} and V_{-in} are both negative. By connecting receivers with the differential pins swapped we can define a voltage range between $[-V_{-in}, V_{-in}]$ in which a fault detection can be issued by ANDing the R pins of the two receivers (this will be internally done in the FPGA).

Further information can be found in Texas Instruments technical document slyt257.



Project/Equipment		Projet	
<div>Document</div> <div>BE-CO</div> <div></div>	CONV-TTL-RS485 INPUT UNIT		
	Designer	Carlos Gil Soriano	CreateDate
	Drawn by	Carlos Gil Soriano	14/08/2012
	Check by	B. Recordon	14/08/2012
	Last Mod.	-	14/08/2012
File		Input Unit RS485 SchDoc	
Print Date		14/08/2012 17:28:22	Sheet 10 of 13
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02541-V1-0	Rev 5

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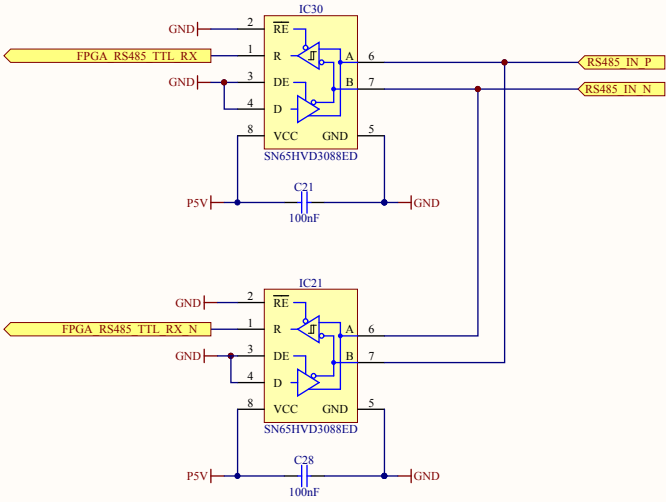
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	Check by	B. Recordon	14/08/2012
	Last Mod.	-	14/08/2012
	File	Input Unit RS485 SchDoc	
Print Date		14/08/2012 17:28:23	Sheet 10 of 13
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02541-V1-0	Rev 5

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Extra functionality: DETECTION OF LOW DIFFERENTIAL SIGNAL

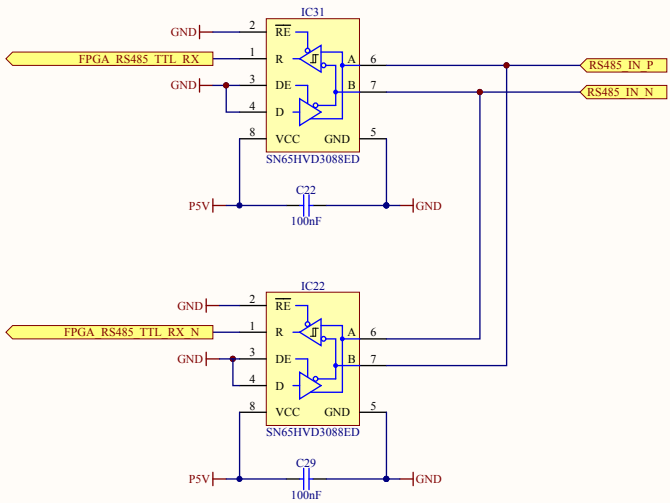
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Document	Designer	Carlos Gil Soriano	CreateDate
	Drawn by	Carlos Gil Soriano	14/08/2012
	Check by	B. Recordon	14/08/2012
	Last Mod.	-	14/08/2012
	File	Input Unit RS485 SchDoc	
Print Date		14/08/2012 17:28:23	Sheet 10 of 13
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02541-V1-0	Rev 5

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Extra functionality: DETECTION OF LOW DIFFERENTIAL SIGNAL

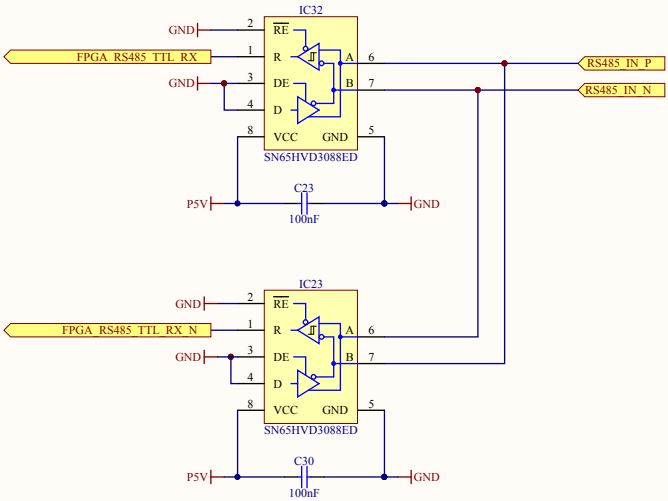
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Document	Designer	Carlos Gil Soriano	CreateDate
	Drawn by	Carlos Gil Soriano	14/08/2012
	Check by	B. Recordon	14/08/2012
	Last Mod.	-	14/08/2012
	File	Input Unit RS485 SchDoc	
Print Date		14/08/2012 17:26:24	Sheet 10 of 13
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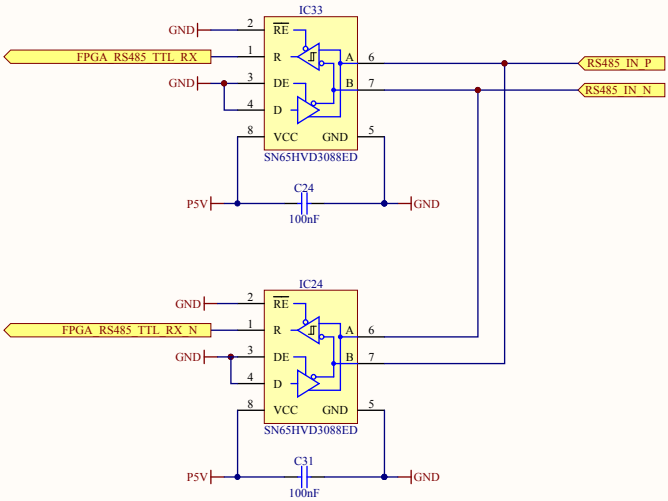
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Project/Equipment		Projet	
<div>Document</div> <div>BE-CO</div> <div></div>	CONV-TTL-RS485		Designer Carlos Gil Soriano
	INPUT UNIT		Drawn by Carlos Gil Soriano CreateDate
			Check by B. Recordon 14/08/2012
			Last Mod. - 14/08/2012
			File Input Unit RS485 SchDoc
		Print Date 14/08/2012 17:26:24	Sheet 10 of 13
		European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	Rev A3 5
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Extra functionality: DETECTION OF LOW DIFFERENTIAL SIGNAL

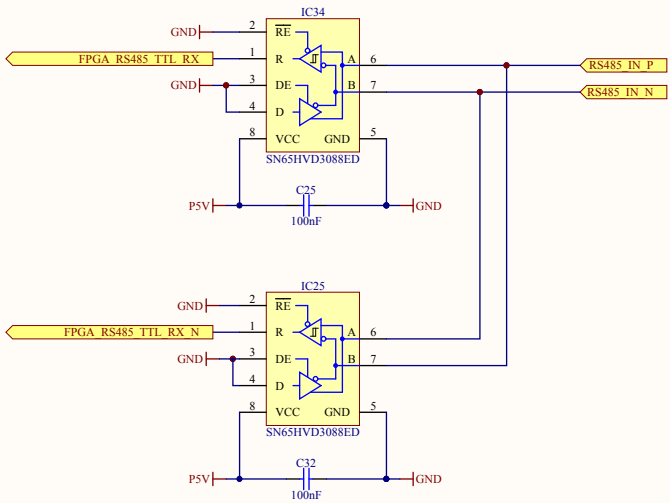
This extra feature can be used to monitor whether the input link is alive. Having not enough differential signal can be interpreted in several ways:


- We are experiencing a lot of attenuation in the link
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HOW TO IMPLEMENT

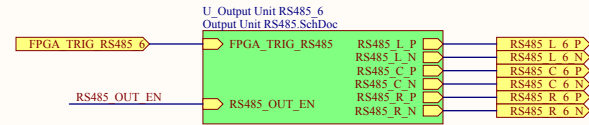
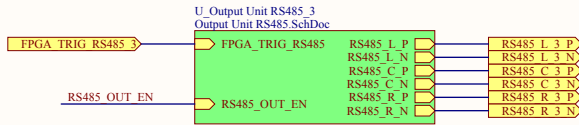
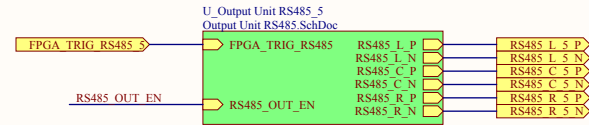
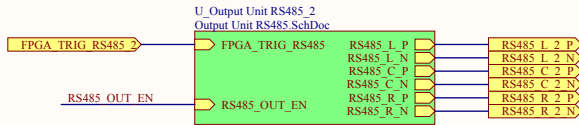
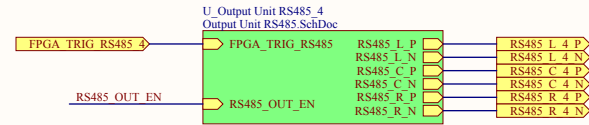
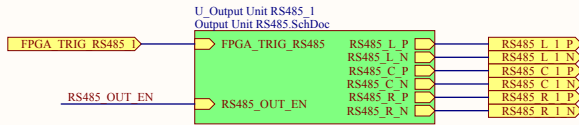
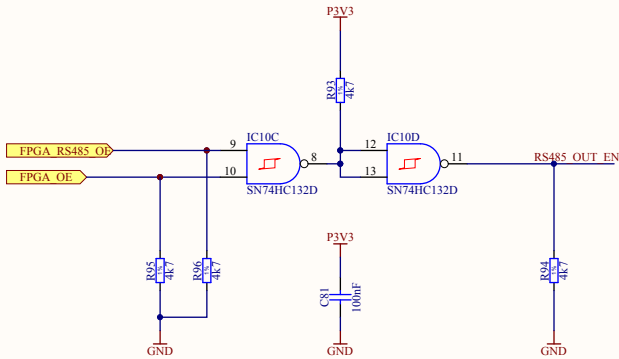
First, a glance to the SN65HVD3088ED shows that the input differential thresholds V_{+in} and V_{-in} are both negative. By connecting receivers with the differential pins swapped we can define a voltage range between $[-V_{-in}, V_{-in}]$ in which a fault detection can be issued by ANDing the R pins of the two receivers (this will be internally done in the FPGA).

Further information can be found in Texas Instruments technical document slyt257.



Project/Equipment		Projet	
<div>Document</div> <div>BE-CO</div> <div></div>	CONV-TTL-RS485		Designer Carlos Gil Soriano
	INPUT UNIT		Drawn by Carlos Gil Soriano
			Check by B. Recordon
			Last Mod. - 14/08/2012
			File Input Unit RS485 SchDoc
		Print Date 14/08/2012 17:28:24	Sheet 10 of 13
		European Organization for Nuclear Research	
		CH-1211 Genève 23 - Switzerland	
		EDA-02541-V1-0	
		Size A3	Rev 5

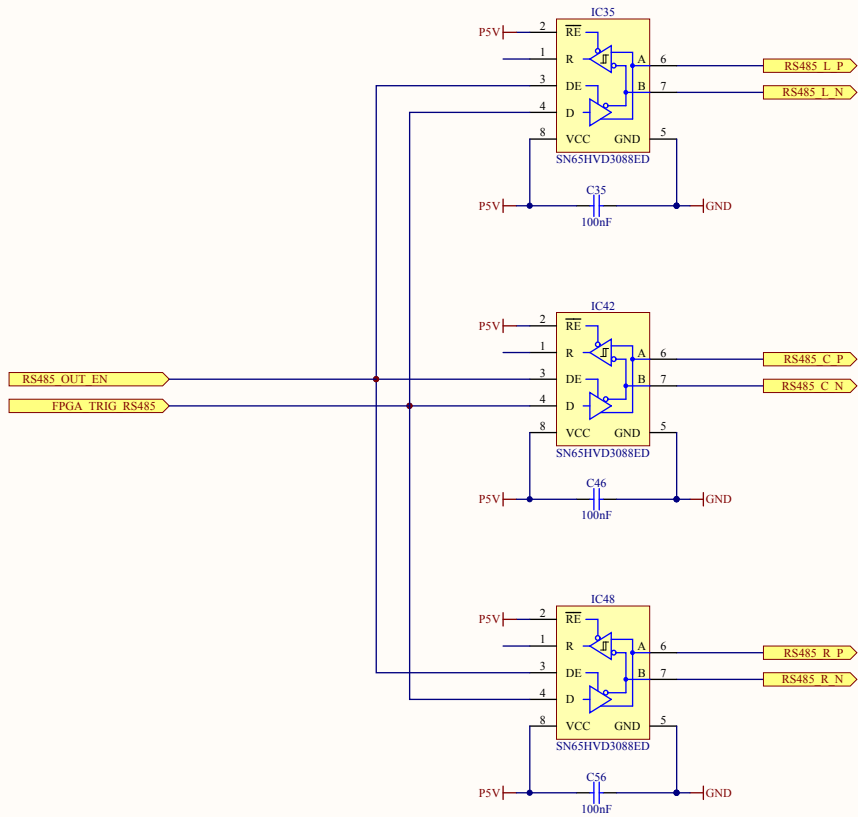
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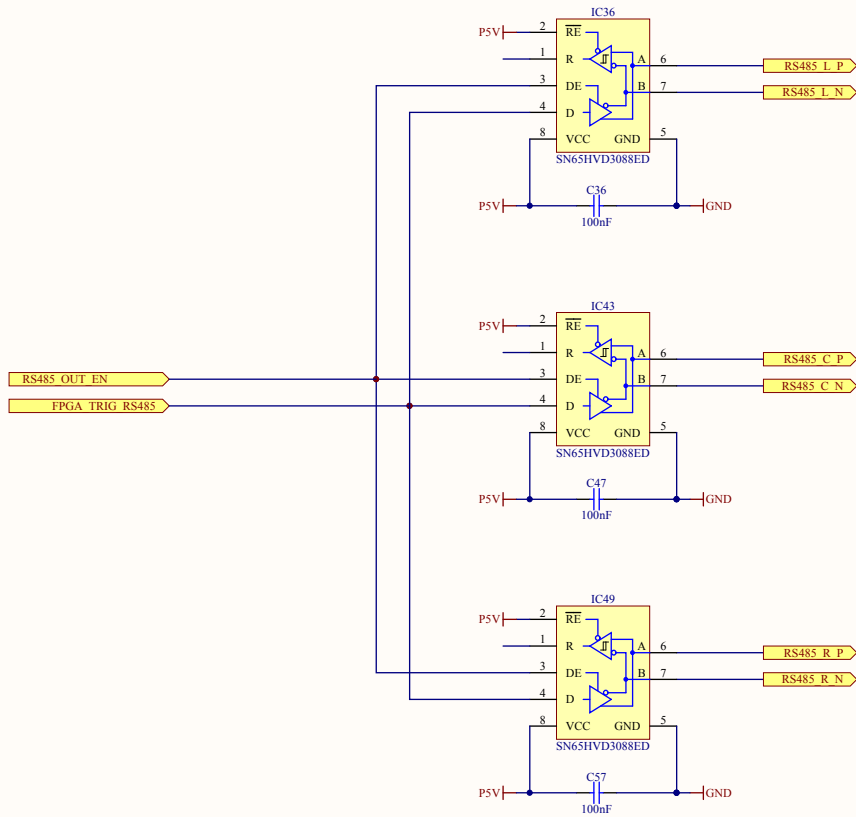
Every SN65HVD3088ED can drive up to 256 nodes




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<div>Document</div> <div>BE-CO</div> <div></div>	Designer Carlos Gil Soriano		
	Drawn by Carlos Gil Soriano		CreateDate
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	Last Mod. -		14/08/2012
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Every SN65HVD3088ED can drive up to 256 nodes

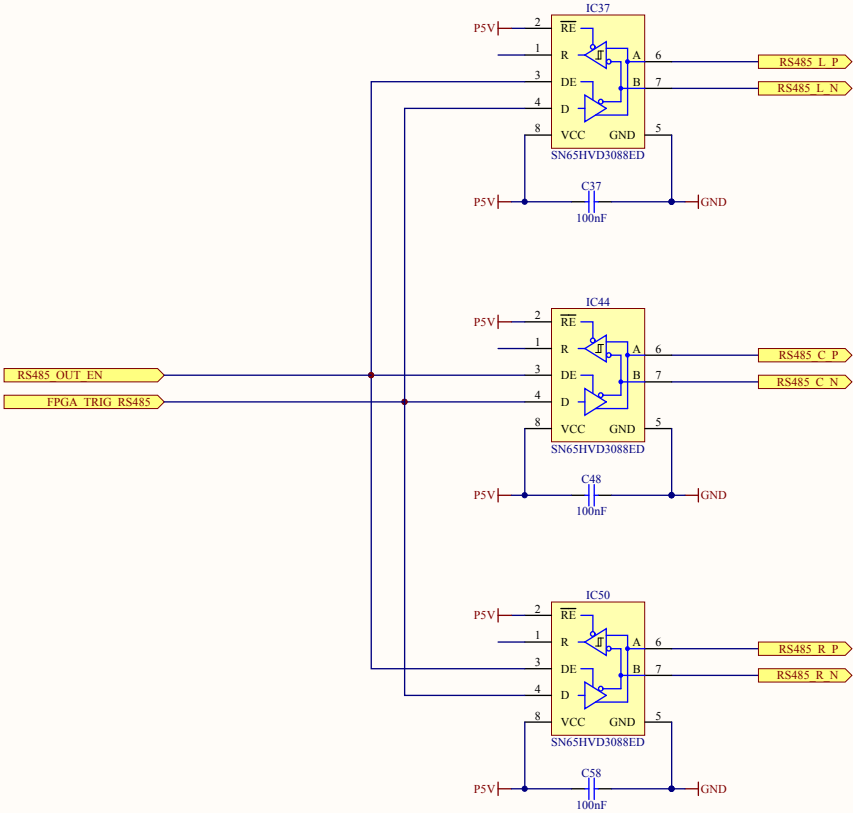



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			Last Mod. -
			File Output Unit RS485.SchDoc
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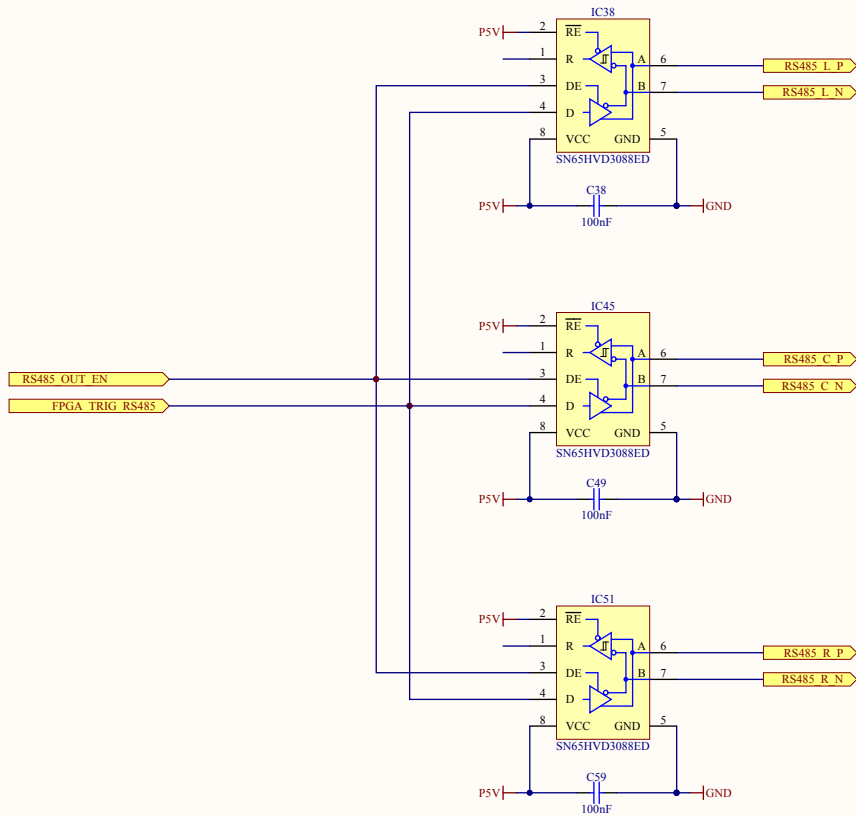
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	Last Mod.		-
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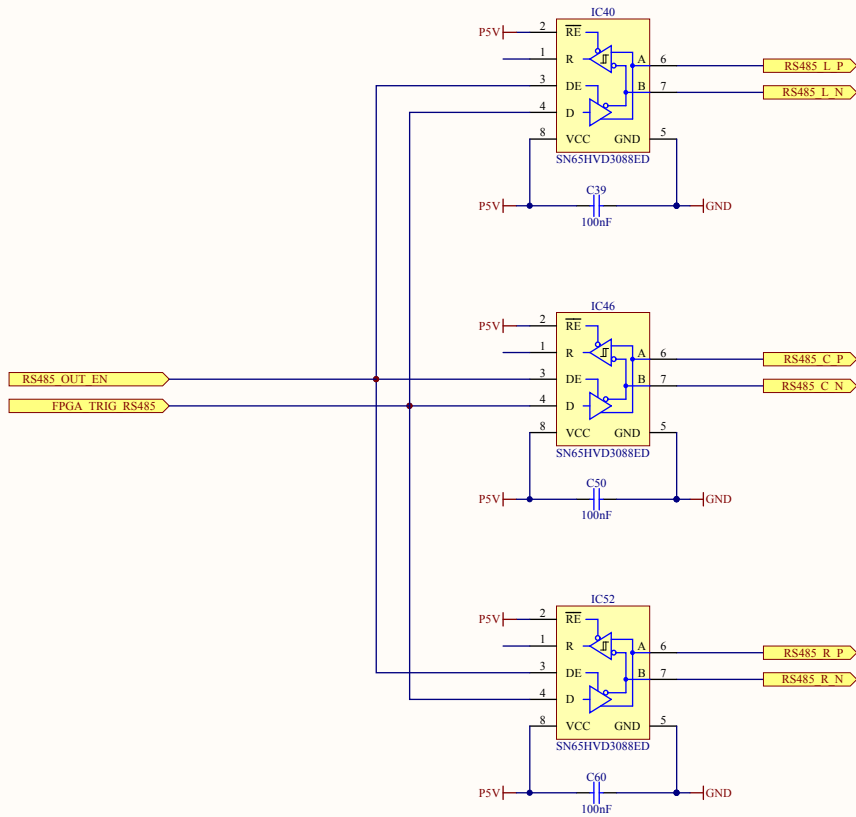
Every SN65HVD3088ED can drive up to 256 nodes




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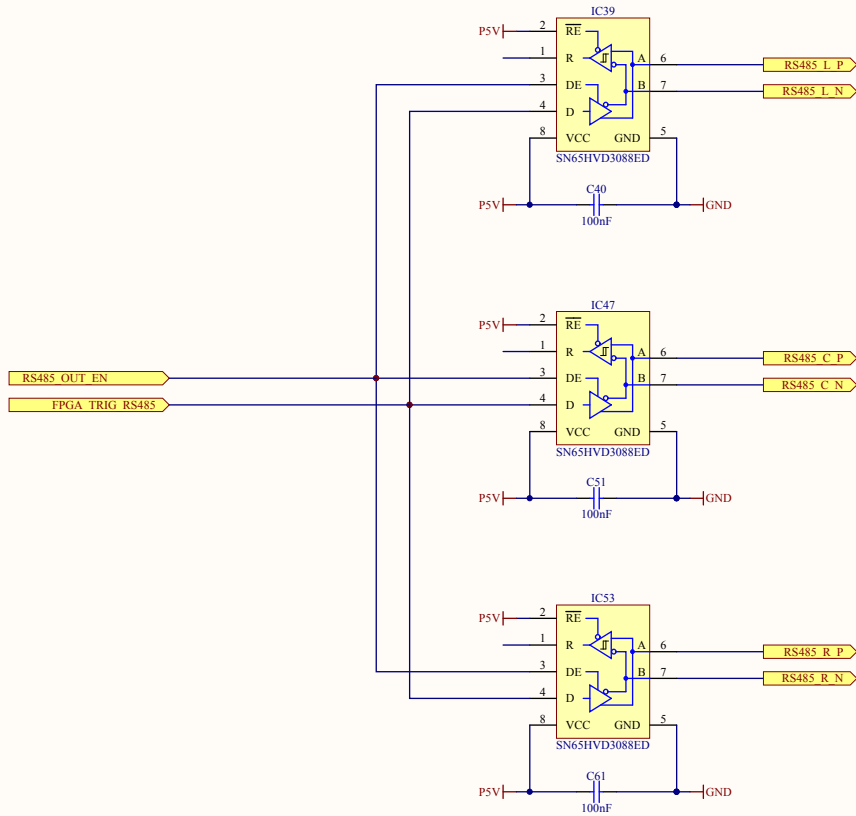
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			File Output Unit RS485.SchDoc
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Every SN65HVD3088ED can drive up to 256 nodes

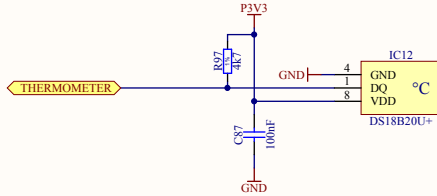


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File	Output Unit RS485 SchDoc		
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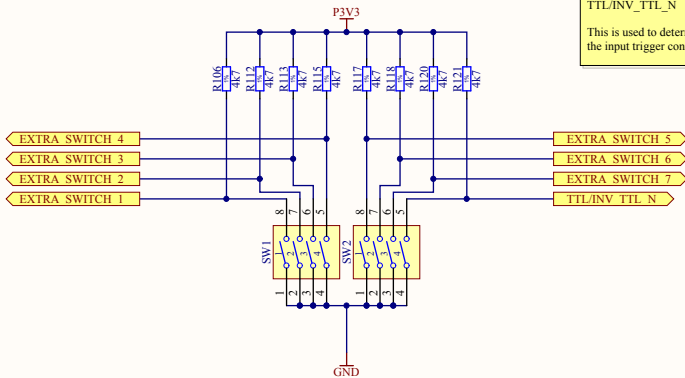
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Thermometer will be used to have a FPGA unique ID

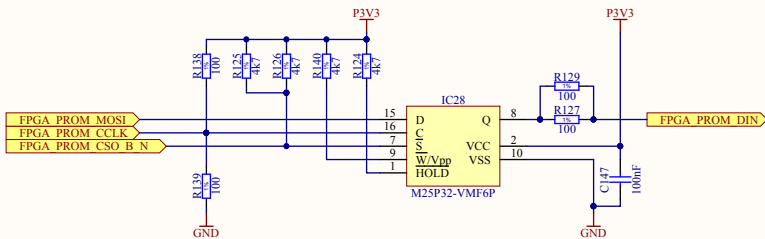


RFU switch

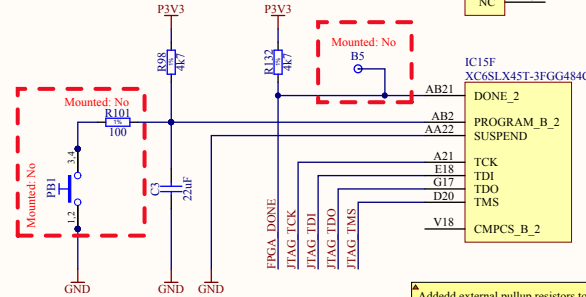


TTL/INV TTL N
This is used to determine the level of
the input trigger connector

PROM MEMORY
W_N is 1 to allow writes in the
memory



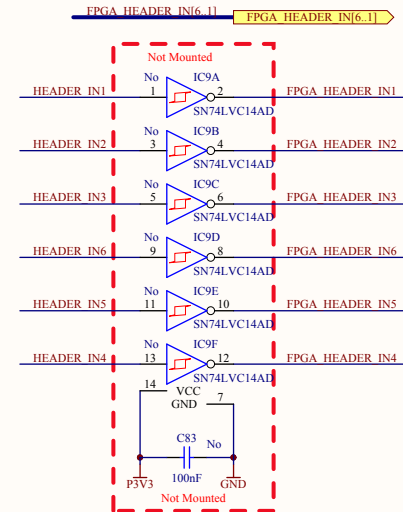
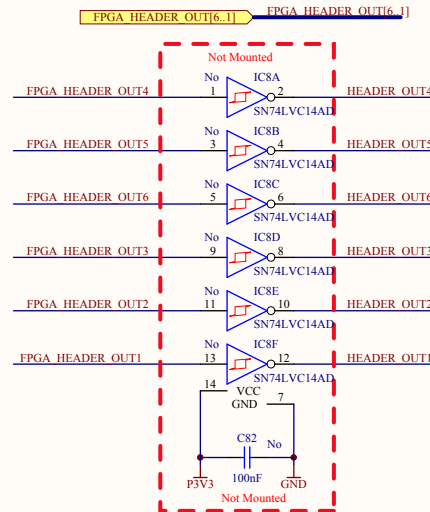
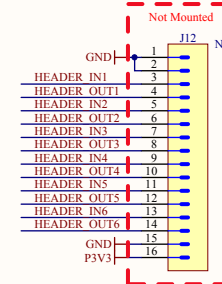
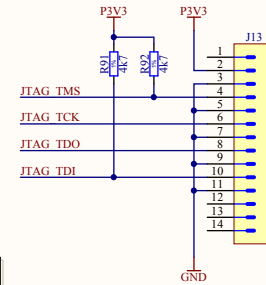
PROGRAM_B must be asserted low
for more than 500ns



Addded external pullup resistors to pins TDI and TMS as
recommended in Xilinx's answer response 11433
However as the JTAG TAP controller fsm is in reset always
that TMS experiences two consecutives ones, we can leave it
pulled up
UG380 pg56: the four JTAG pins are internally pulled up.
Hence, there's no need of external ones.

IC151
XC6SLX45T-3FPG484C
NC
P15
T16
NC

IC15F
XC6SLX45T-3FPG484C
DONE_2
AB21
AA22
PROGRAM_B_2
SUSPEND
TCK
TDI
G17
D20
TMS
V18
CMPCS_B_2



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		Print Date 14/08/2012 17:26:27	
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