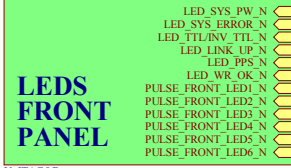
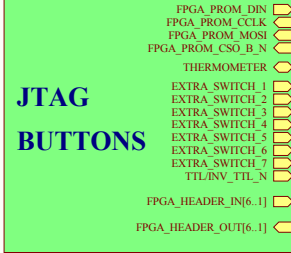


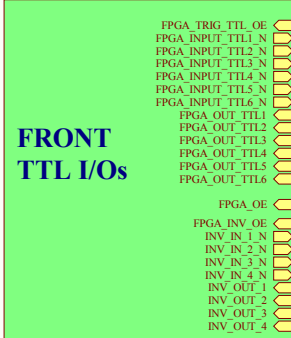
U\_FrontPanelLeds  
FrontPanelLeds.SchDoc



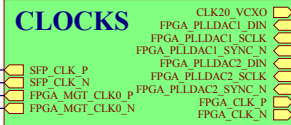
U\_JTAG&Button  
JTAG&Button.SchDoc



U\_FrontTTL  
FrontTTL.SchDoc



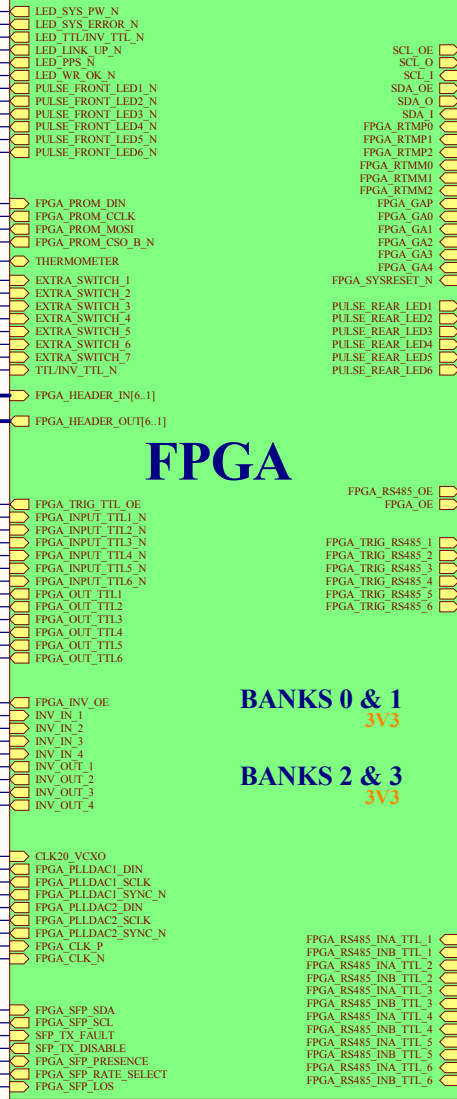
U\_Clocks&Monitor  
Clocks&Monitor.SchDoc



U\_Communication  
Communication.SchDoc



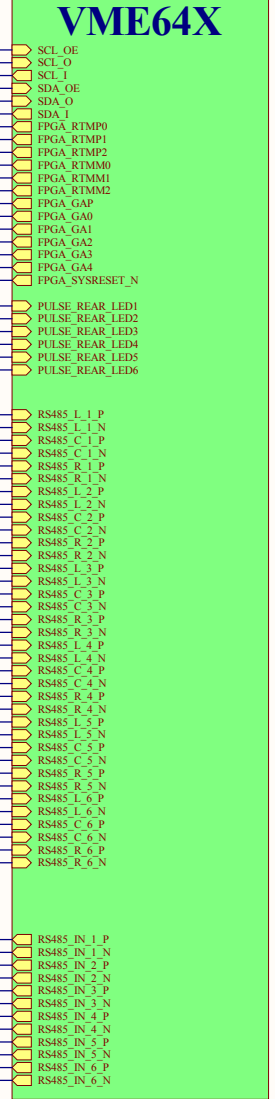
U\_FPGAbank  
FPGAbank.SchDoc



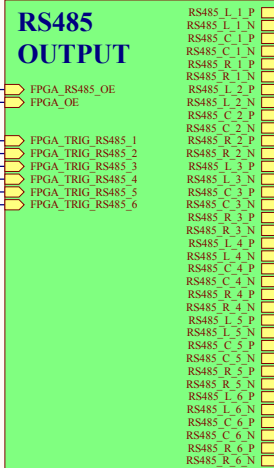
U\_FPGAs  
FPGAs.SchDoc



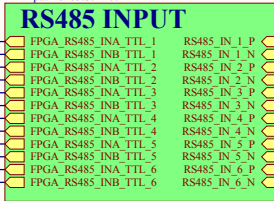
U\_VME64sConn  
VME64sConn.SchDoc

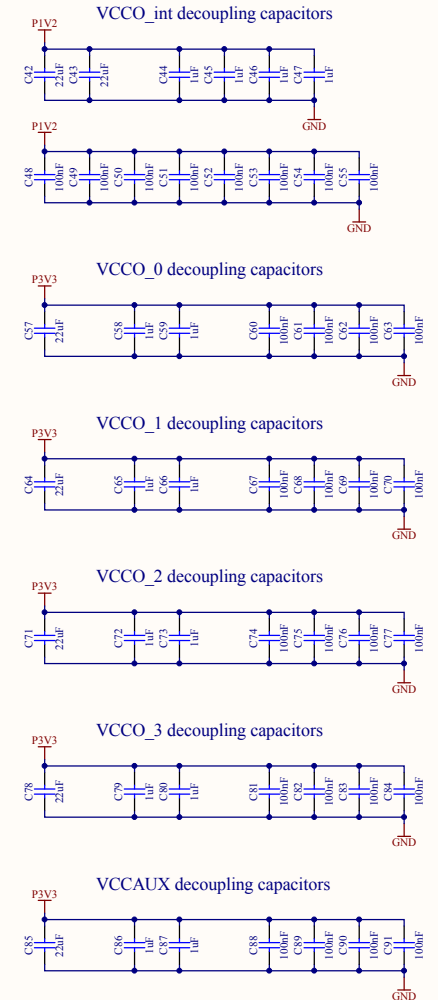
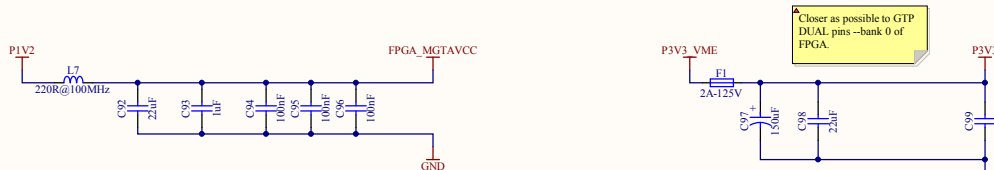
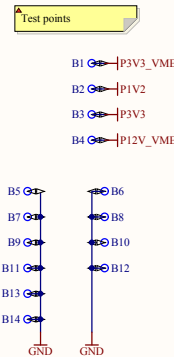
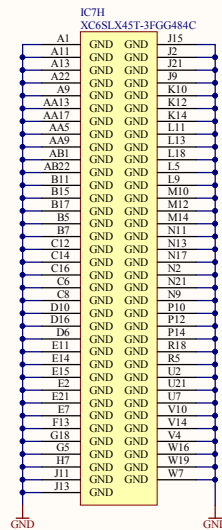
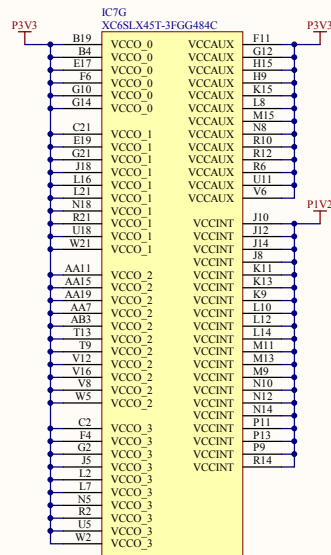
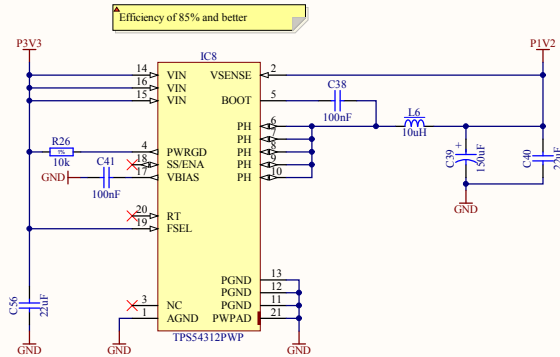


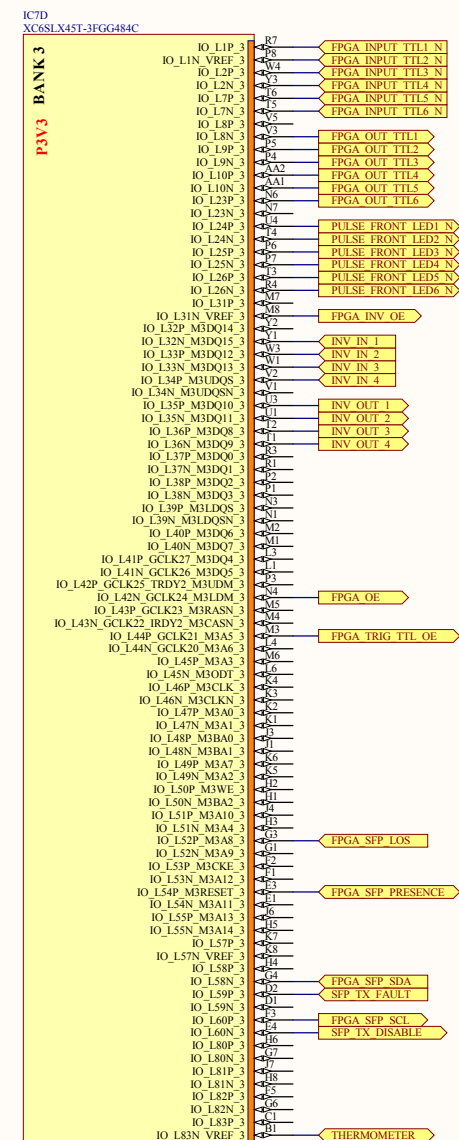
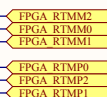
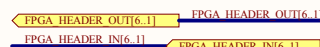
U\_Output RS485  
Output RS485.SchDoc



U\_Input RS485  
Input RS485.SchDoc

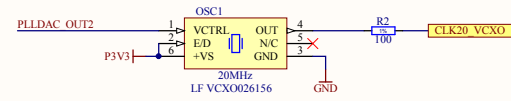
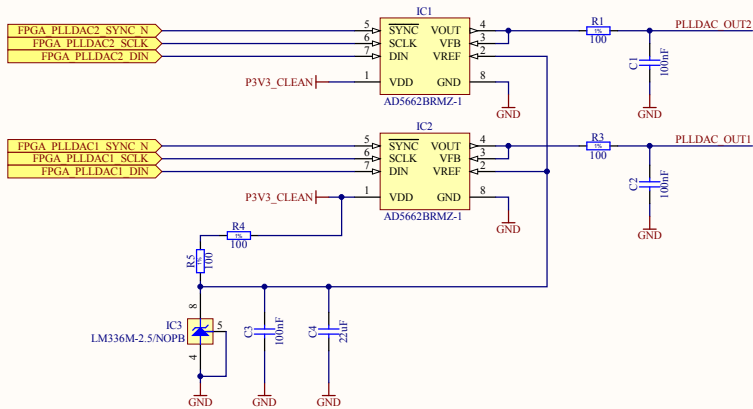






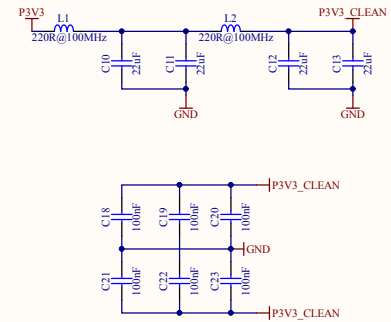
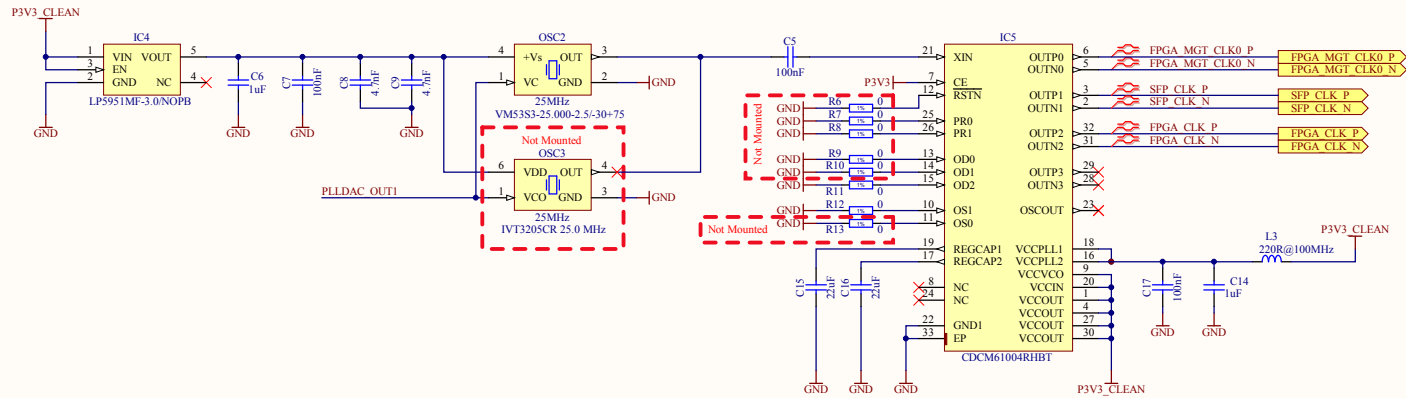
DAC Vih = 2V so it accepts 2.5V CMOS signal  
DAC output range: 0V to 2.5V

DAC Vih = 2V so it accepts 2.5V CMOS signal  
DAC output range: 0V to 2.5V



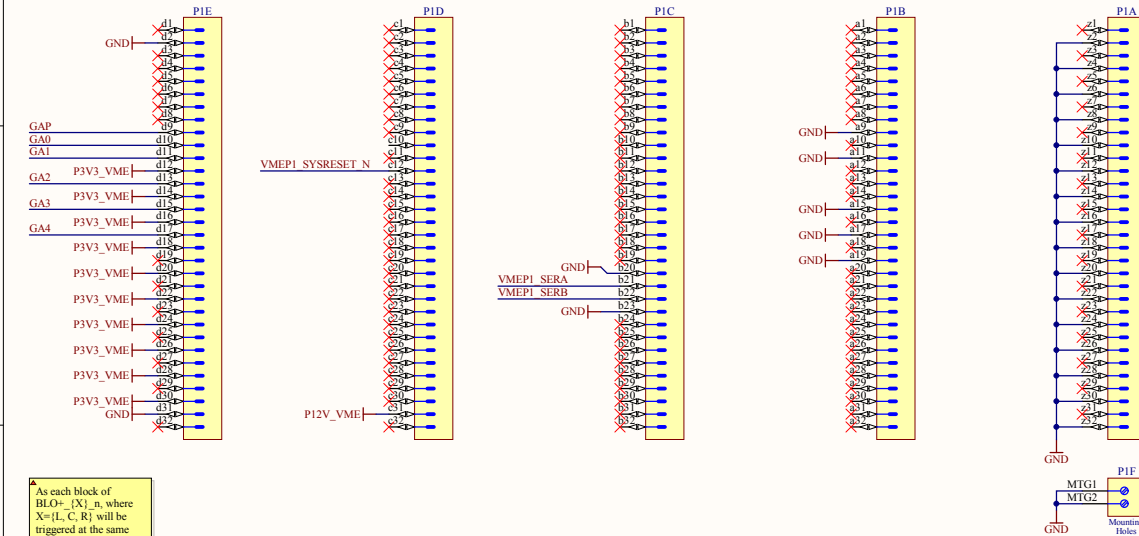
Control voltage is +1.5V±1V.  
Min. pull range is ±10 ppm for ±1V.  
Positive slope (Positive voltage for positive frequency shift).

CDCM61004 configuration:  
LVDS outputs  
PRESC DIV = 4  
FB DIV = 20  
OUT DIV = 4  
All config inputs have internal pull-ups.  
Input = 25 MHz  
Output=125 MHz



Utility Bus Signal: see page 199  
ANSI/VITA 1-1994

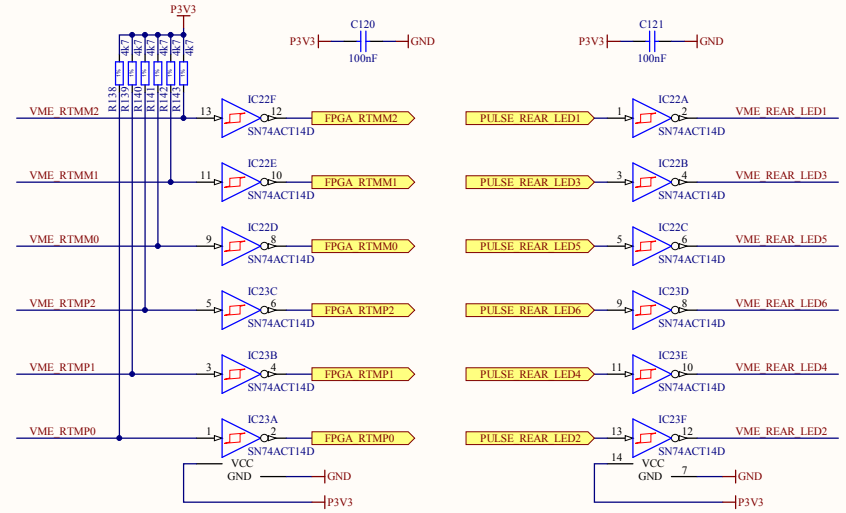
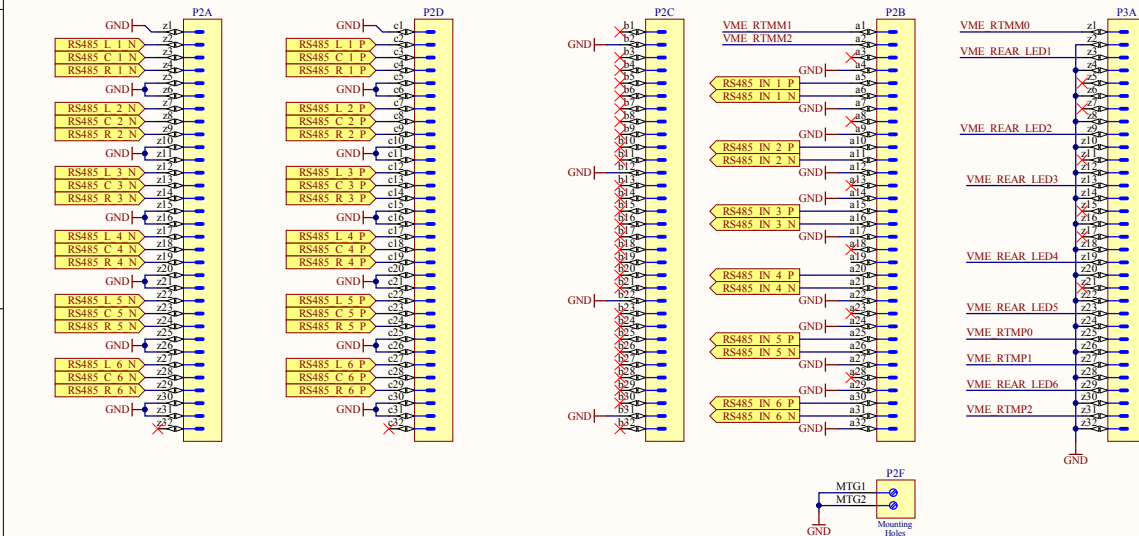
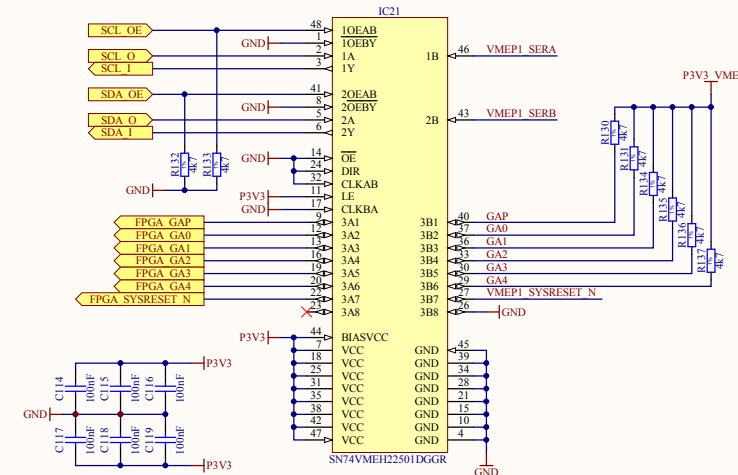
Output configurations in page 230  
ACFAIL\_N Open collector  
SYSFAIL\_N Open collector  
SYSRESET\_N Open collector  
SYSCLK Totem-pole



As each block of  $BLO+ \{X\}_n$ , where  $X=\{L, C, R\}$  will be triggered at the same time, cross talk should not be so critical. However, it would be better group the signals as it is shown and leave group between sets of signals triggered by different sources.

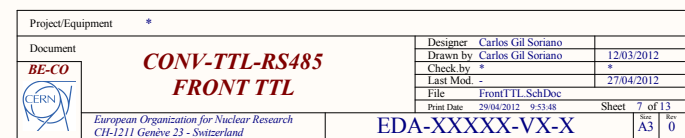
As input signals come from far away, the spectrum of this signal will have less high frequency components than the spectrum of the generated Standard Blocking in conv-ttl-blo. Signals with more spectral power in higher frequencies should be routed more carefully, so it is better to leave the easiest paths to them. In this case, outer pins should be available for output signals and inner pins to input ones.

As can be seen in ANSI/VITA 1-1994 page 247, the row b is used in VME64. Hence, none of its pins can be used. Rows z,a,c,d have available pins as documented in the VME64 and VME64x specifications.

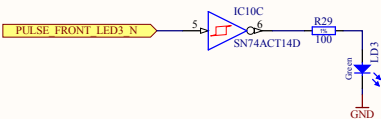
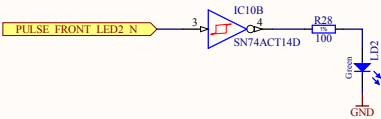
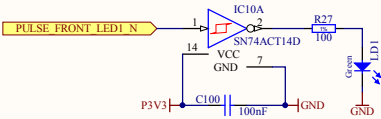


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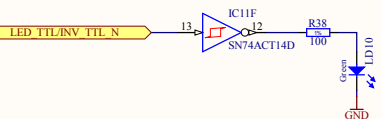
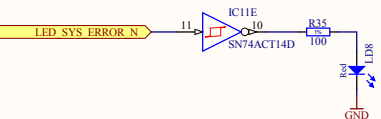
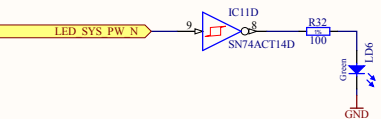
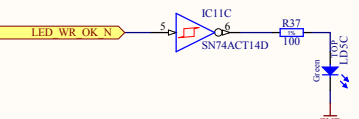
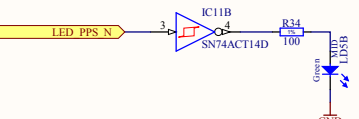
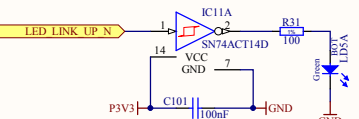
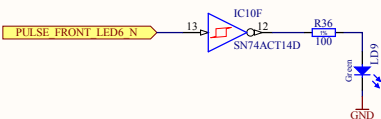
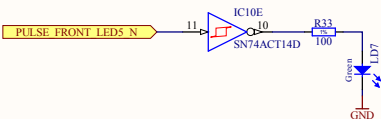
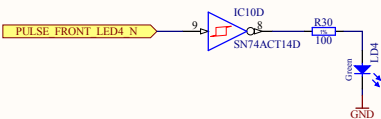




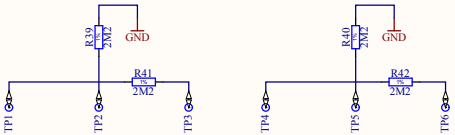




Dialight model		
Green	551-1307F	2.5V@ 4.7mA
Red	551-1107F	1.9V@ 6mA



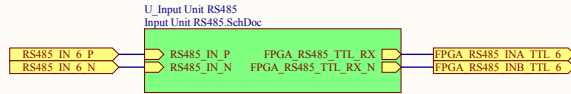
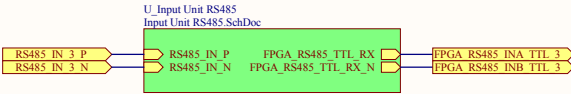
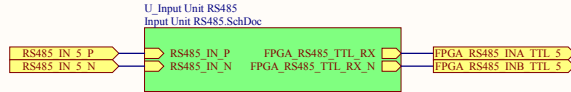
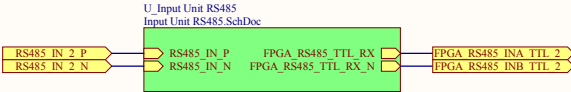
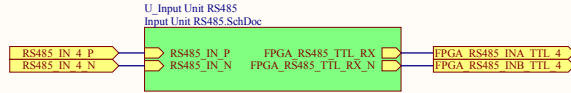
ESD discharge strips (top and bottom of the card)



- FTG1
- FTG2
- FTG3
- FTG4
- FTG5
- FTG6

Project/Equipment		*	
Document		Designer Carlos Gil Soriano	
BE-CO		Drawn by Carlos Gil Soriano	
CERN		Check by *	
European Organization for Nuclear Research		Last Mod. -	
CH-1211 Genève 23 - Switzerland		File FrontPanelLeds.SchDoc	
EDA-XXXXX-VX-X		Print Date 29/04/2012 9:53:49	
		Sheet 8 of 13	
		A3	





Extra functionality: DETECTION OF LOW DIFFERENTIAL SIGNAL.

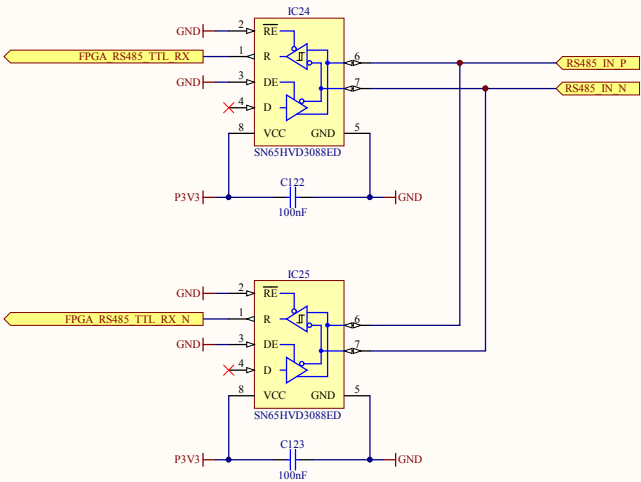
This extra feature can be used to monitor whether the input link is alive. Having not enough differential signal can be interpreted in several ways:

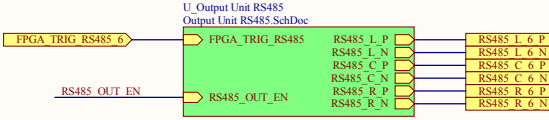
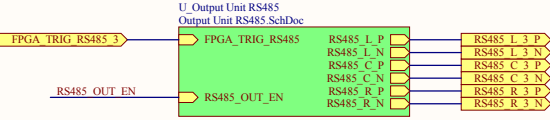
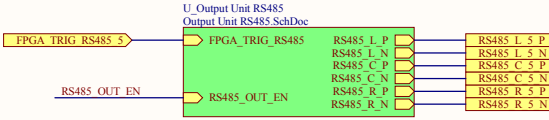
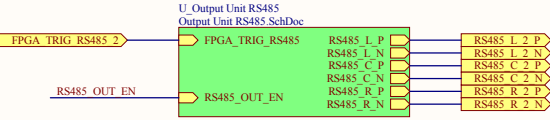
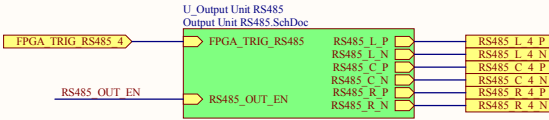
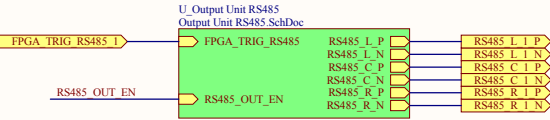
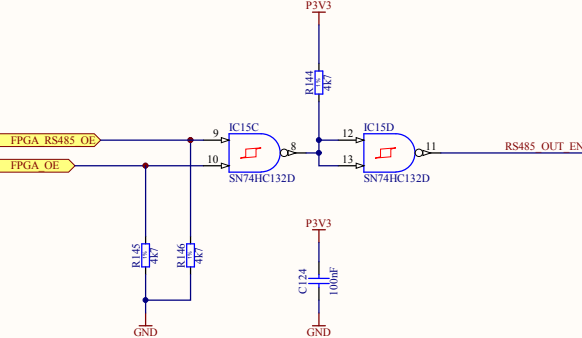
- We are experiencing a lot of attenuation in the link
- Cable is not connected
- DC supression device, such a transformer, has been connected in the link.

HOW TO IMPLEMENT

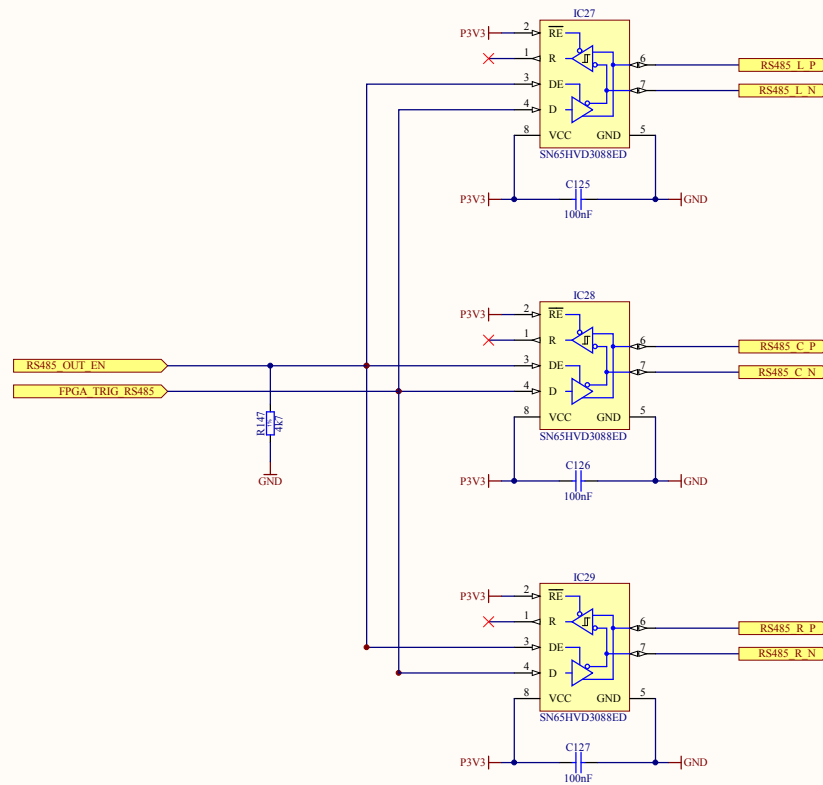
First, a glance to the SN65HVD3088ED shows that the input differential thresholds  $V_{+in}$  and  $V_{-in}$  are both negative. By connecting receivers with the differential pins swapped we can define a voltage range between  $[-V_{-in}, V_{-in}]$  in which a fault detection can be issued by **ANDing** the R pins of the two receivers (this will be internally done in the FPGA).

Further information can be found in Texas Instruments technical document sly257.

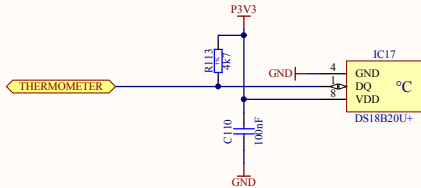




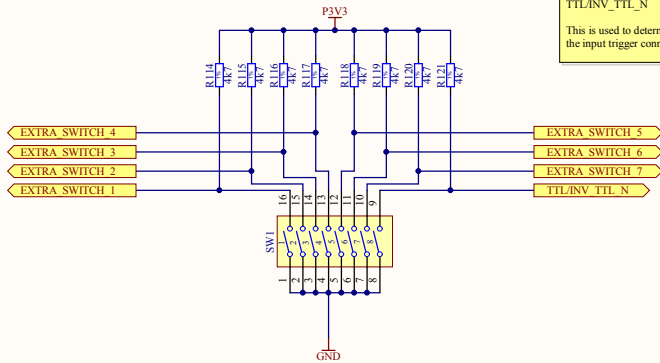
Every SN65HVD3088ED can drive up to 256 nodes



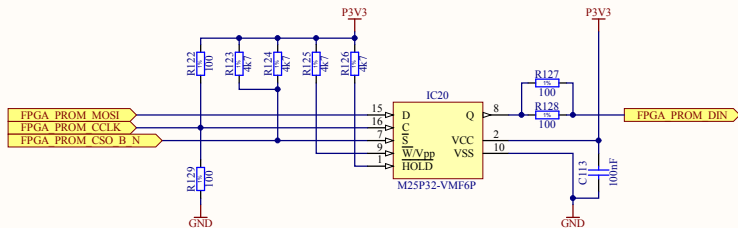
Thermometer will be used to have a FPGA unique ID



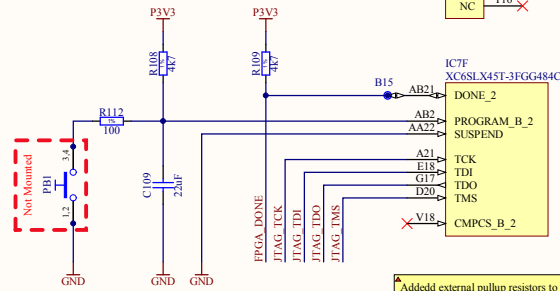
RFU switch



PROM MEMORY  
W\_N is 1 to allow writes in the memory

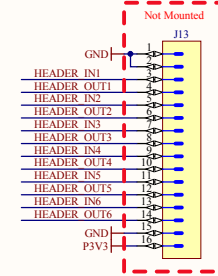
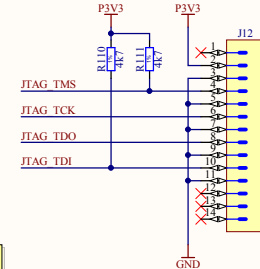


PROGRAM\_B must be asserted low for more than 500ns

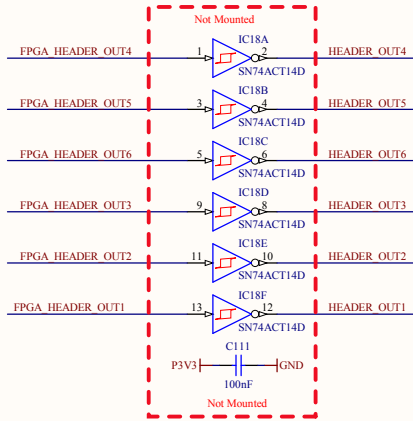


IC7I  
XC6SLX45T-3FGG484C  
NC  
U17  
P15  
T16

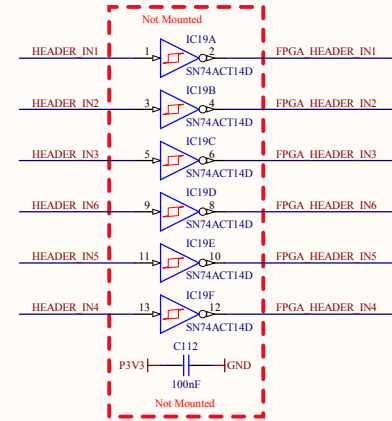
Add external pullup resistors to pins TDI and TMS as recommended in Xilinx's answer response 11433. However as the JTAG TAP controller fsm is in reset always that TMS experiences two consecutive ones, we can leave it pulled up.  
UG380 pg56: the four JTAG pins are internally pulled up. Hence, there's no need of external ones.



FPGA HEADER OUT[6..1]



FPGA HEADER IN[6..1]



[illegible]