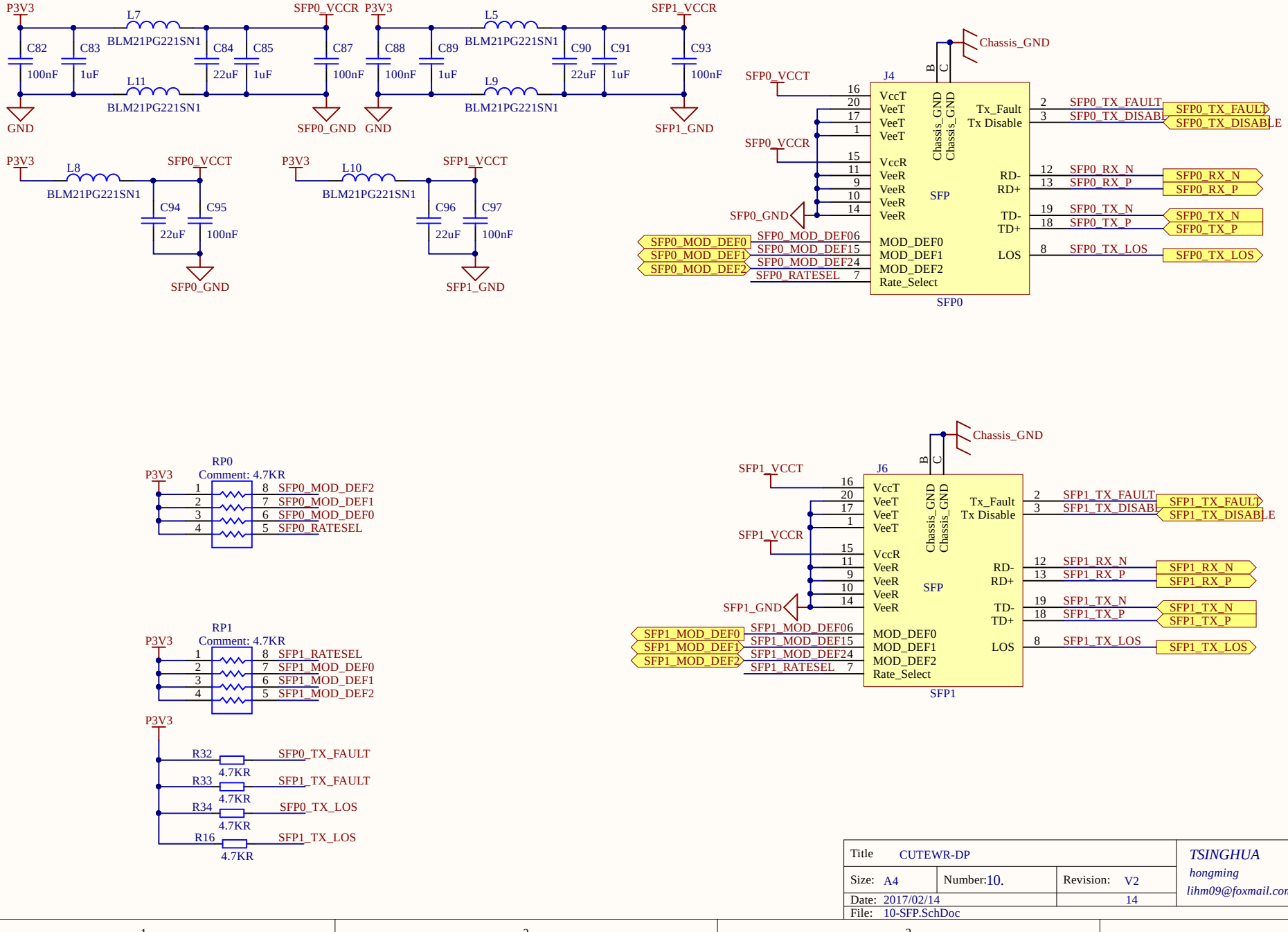
P3V3
L7
BLM21PG221SN1
C82
100nF
C83
1uF
C84
22uF
C85
1uF
C87
100nF
L11
BLM21PG221SN1
GND
SFP0_VCCR
SFP0_GND
P3V3
L5
BLM21PG221SN1
C88
100nF
C89
1uF
C90
22uF
C91
1uF
C93
100nF
L9
BLM21PG221SN1
GND
SFP1_VCCR
SFP1_GND
P3V3
L8
BLM21PG221SN1
C94
22uF
C95
100nF
SFP0_VCCT
SFP0_GND
P3V3
L10
BLM21PG221SN1
C96
22uF
C97
100nF
SFP1_VCCT
SFP1_GND
Chassis_GND
J4
SFP0_VCCT
SFP0_VCCR
SFP0_GND
SFP0_MOD_DEF0
SFP0_MOD_DEF1
SFP0_MOD_DEF2
VccT
VeeT
VeeT
VeeT
VccR
VeeR
VeeR
VeeR
VeeR
MOD_DEF0
MOD_DEF1
MOD_DEF2
Rate_Select
SFP
Chassis_GND
Chassis_GND
Tx_Fault
Tx Disable
RD-
RD+
TD-
TD+
LOS
SFP0_MOD_DEF06
SFP0_MOD_DEF15
SFP0_MOD_DEF24
SFP0_RATESEL
SFP0_TX_FAULT
SFP0_TX_DISABLE
SFP0_RX_N
SFP0_RX_P
SFP0_TX_N
SFP0_TX_P
SFP0_TX_LOS
SFP0
RP0
Comment: 4.7KR
P3V3
SFP0_MOD_DEF2
SFP0_MOD_DEF1
SFP0_MOD_DEF0
SFP0_RATESEL
RP1
Comment: 4.7KR
P3V3
SFP1_RATESEL
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
P3V3
R32
4.7KR
SFP0_TX_FAULT
R33
4.7KR
SFP1_TX_FAULT
R34
4.7KR
SFP0_TX_LOS
R16
4.7KR
SFP1_TX_LOS
Chassis_GND
J6
SFP1_VCCT
SFP1_VCCR
SFP1_GND
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
VccT
VeeT
VeeT
VeeT
VccR
VeeR
VeeR
VeeR
VeeR
MOD_DEF0
MOD_DEF1
MOD_DEF2
Rate_Select
SFP
Chassis_GND
Chassis_GND
Tx_Fault
Tx Disable
RD-
RD+
TD-
TD+
LOS
SFP1_MOD_DEF06
SFP1_MOD_DEF15
SFP1_MOD_DEF24
SFP1_RATESEL
SFP1_TX_FAULT
SFP1_TX_DISABLE
SFP1_RX_N
SFP1_RX_P
SFP1_TX_N
SFP1_TX_P
SFP1_TX_LOS
SFP1
Title CUTEWR-DP
Size: A4
Number:10.
Revision: V2
Date: 2017/02/14
14
File: 10-SFP.SchDoc
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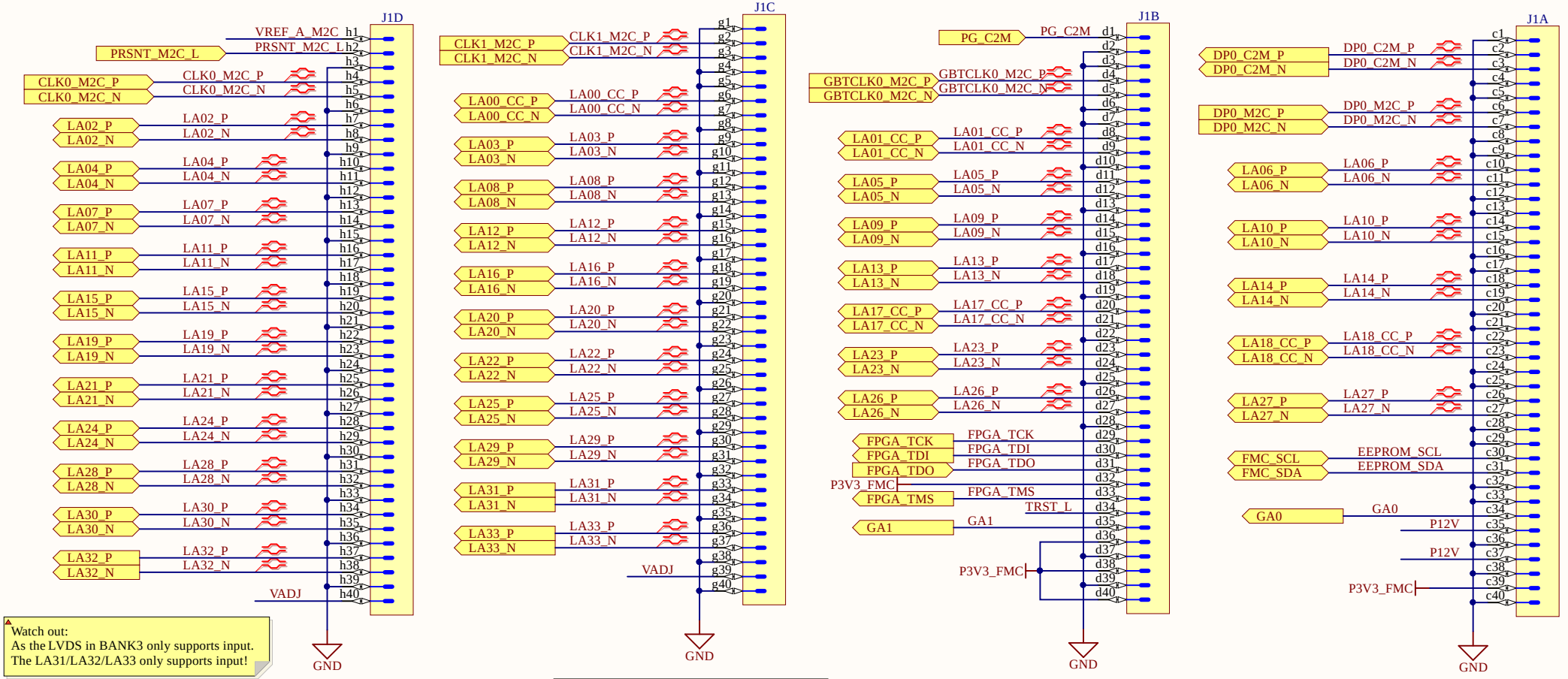

Watch out:
As the LVDS in BANK3 only supports input.
The LA31/LA32/LA33 only supports input!

NB: the LVDS pairs must have a differential impedance of 100 ohm (+/-10%) and be routed with no skew between the P and the N lines. The skew between the various LA pairs should be kept as low as possible (<200ps).

Title	CUTEWR-DP		
Size: A4	Number:11.	Revision: V2	
Date: 2017/02/14		14	
File: 11-FMC_Connector.SchDoc			

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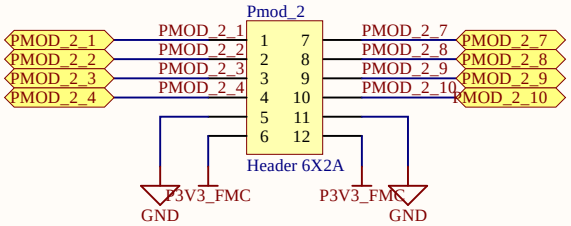

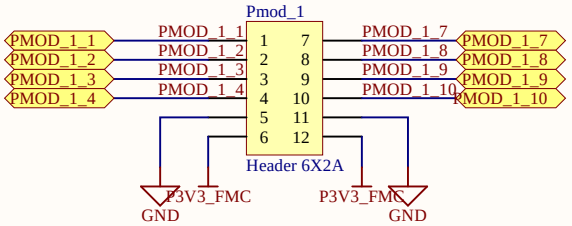

Title	CUTEWR-DP		
Size: A4	Number:12.	Revision: V2	
Date: 2017/02/14		14	
File: 12-Pmod_Connector.SchDoc			

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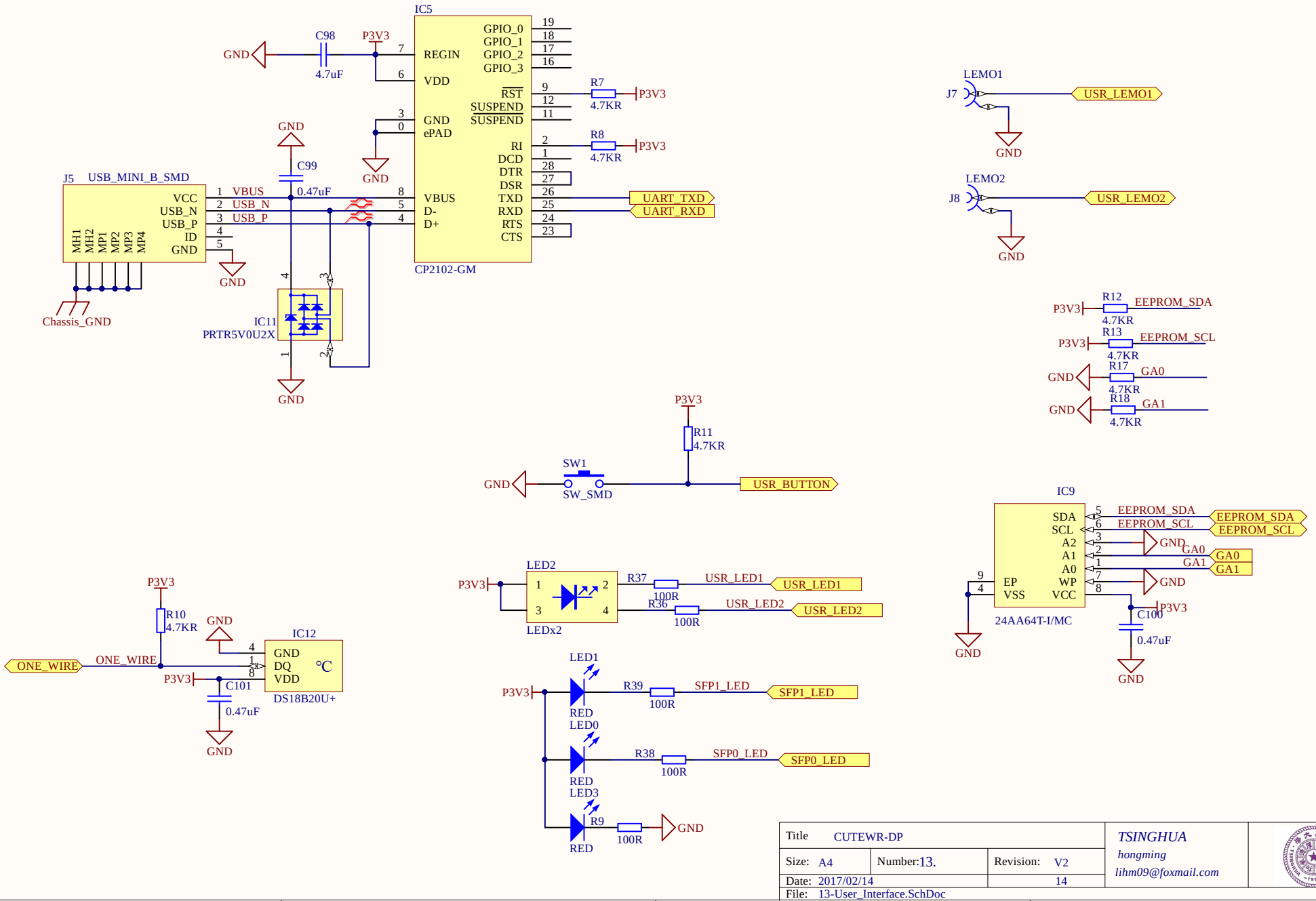
IC5
GPIO_0
GPIO_1
GPIO_2
GPIO_3
REGIN
VDD
RST
SUSPEND
SUSPEND
GND
ePAD
RI
DCD
DTR
DSR
TXD
RXD
RTS
CTS
VBUS
D-
D+
CP2102-GM
C98
4.7uF
C99
0.47uF
R7
R8
4.7KR
P3V3
GND
UART_TXD
UART_RXD
J5
USB_MINI_B_SMD
VCC
USB_N
USB_P
ID
GND
VBUS
USB_N
USB_P
MH1
MH2
MP1
MP2
MP3
MP4
Chassis_GND
IC11
PRTR5V0U2X
LEMO1
J7
USR_LEMO1
LEMO2
J8
USR_LEMO2
R12
R13
R17
R18
EEPROM_SDA
EEPROM_SCL
GA0
GA1
SW1
SW_SMD
R11
USR_BUTTON
IC9
SDA
SCL
A2
A1
A0
WP
VCC
EP
VSS
24AA64T-I/MC
C100
LED2
LEDx2
R37
R36
100R
USR_LED1
USR_LED2
LED1
LED0
LED3
RED
R39
R38
R9
SFP1_LED
SFP0_LED
IC12
DS18B20U+
R10
C101
ONE_WIRE
DQ
VDD
Title CUTEWR-DP
Size: A4
Number:13.
Revision: V2
Date: 2017/02/14
14
File: 13-User_Interface.SchDoc
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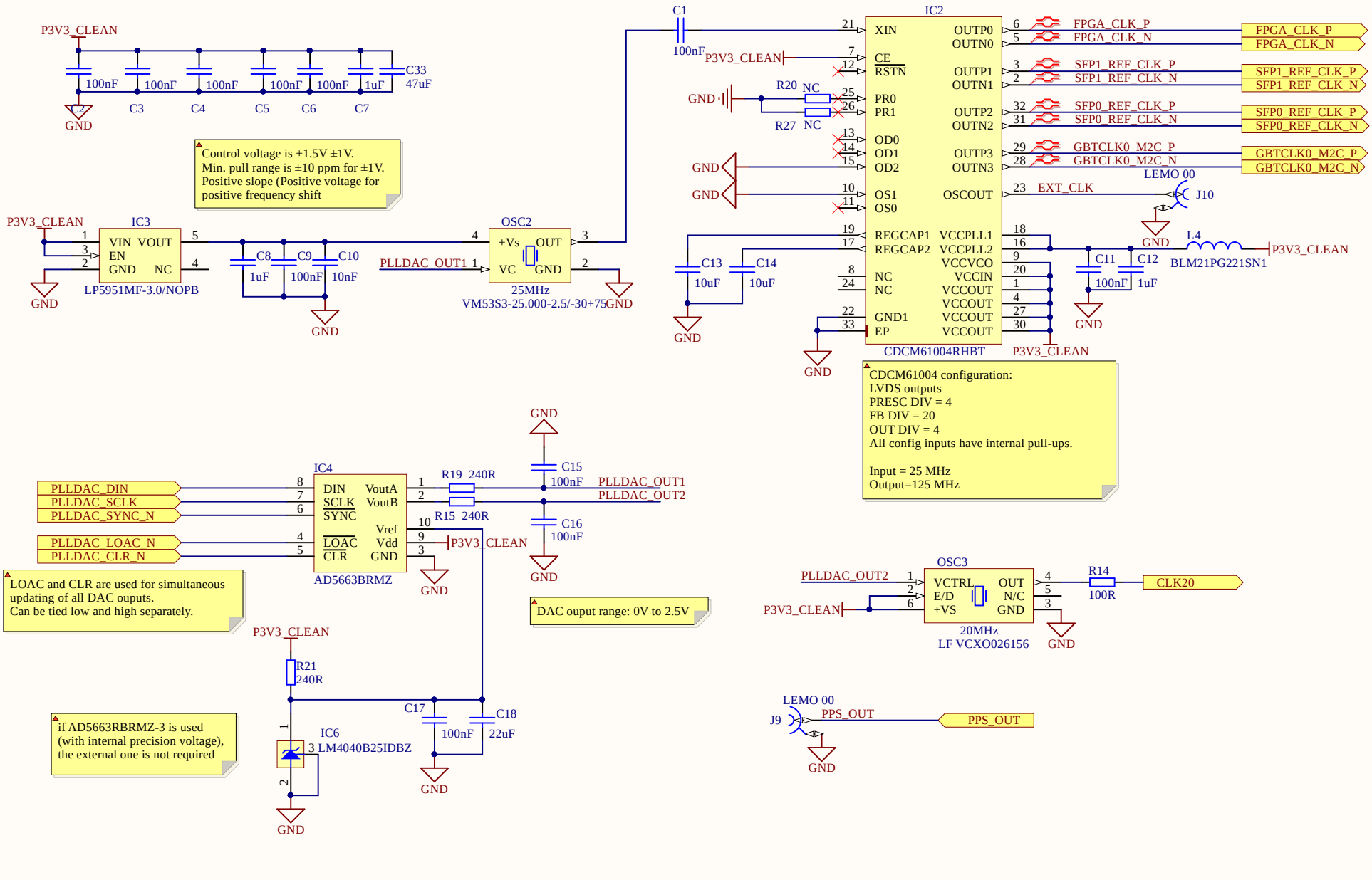

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Size: A4	Number:1.	Revision: V2	
Date: 2017/02/14		14	
File: 1-Clocks.SchDoc			

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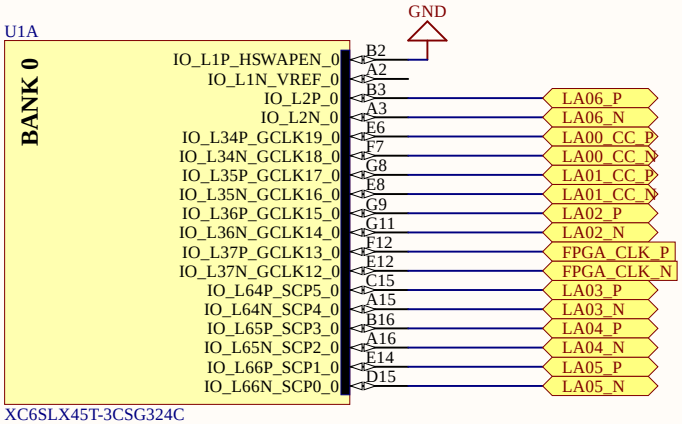
Bank 0 Supports differential output



Title	CUTEWR-DP		
Size: A4	Number:2.	Revision: V2	
Date: 2017/02/14		14	
File: 2-FPGA_bank0.SchDoc			

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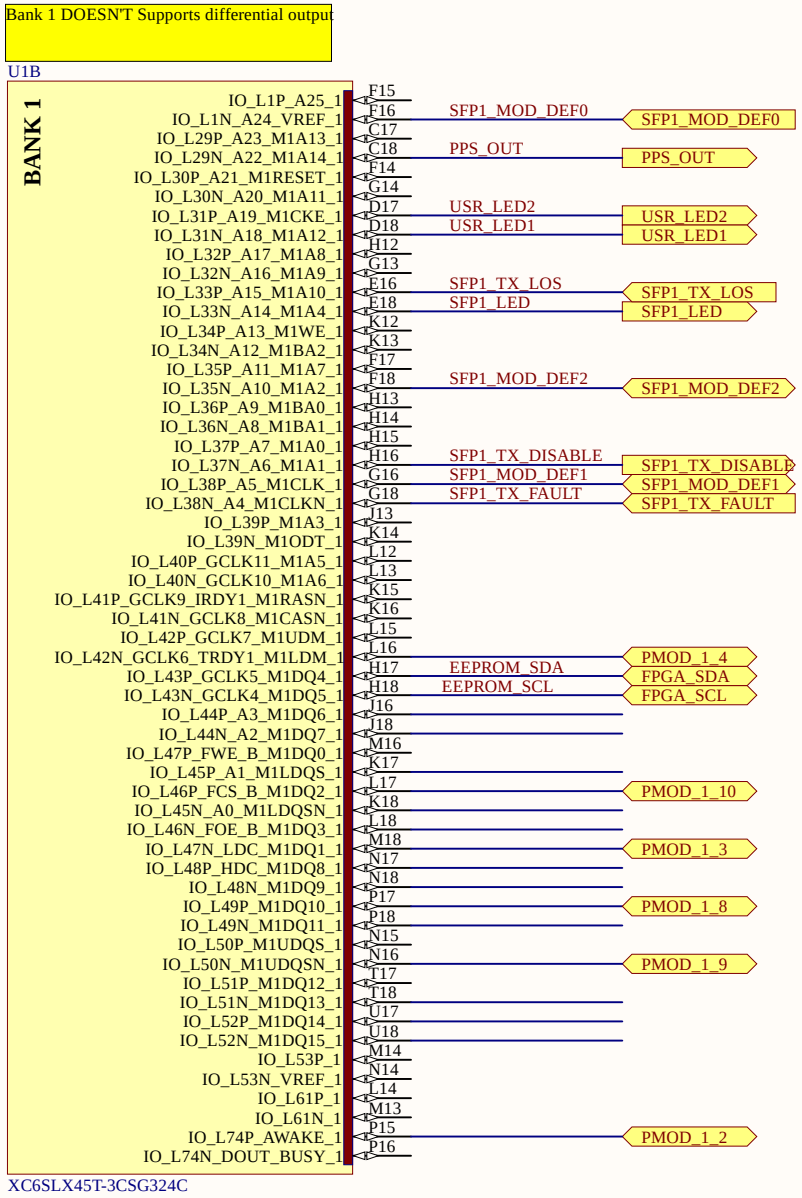

Title	CUTEWR-DP		
Size: A4	Number:3.	Revision: V2	
Date: 2017/02/14		14	
File: 3-FPGA_bank1.SchDoc			

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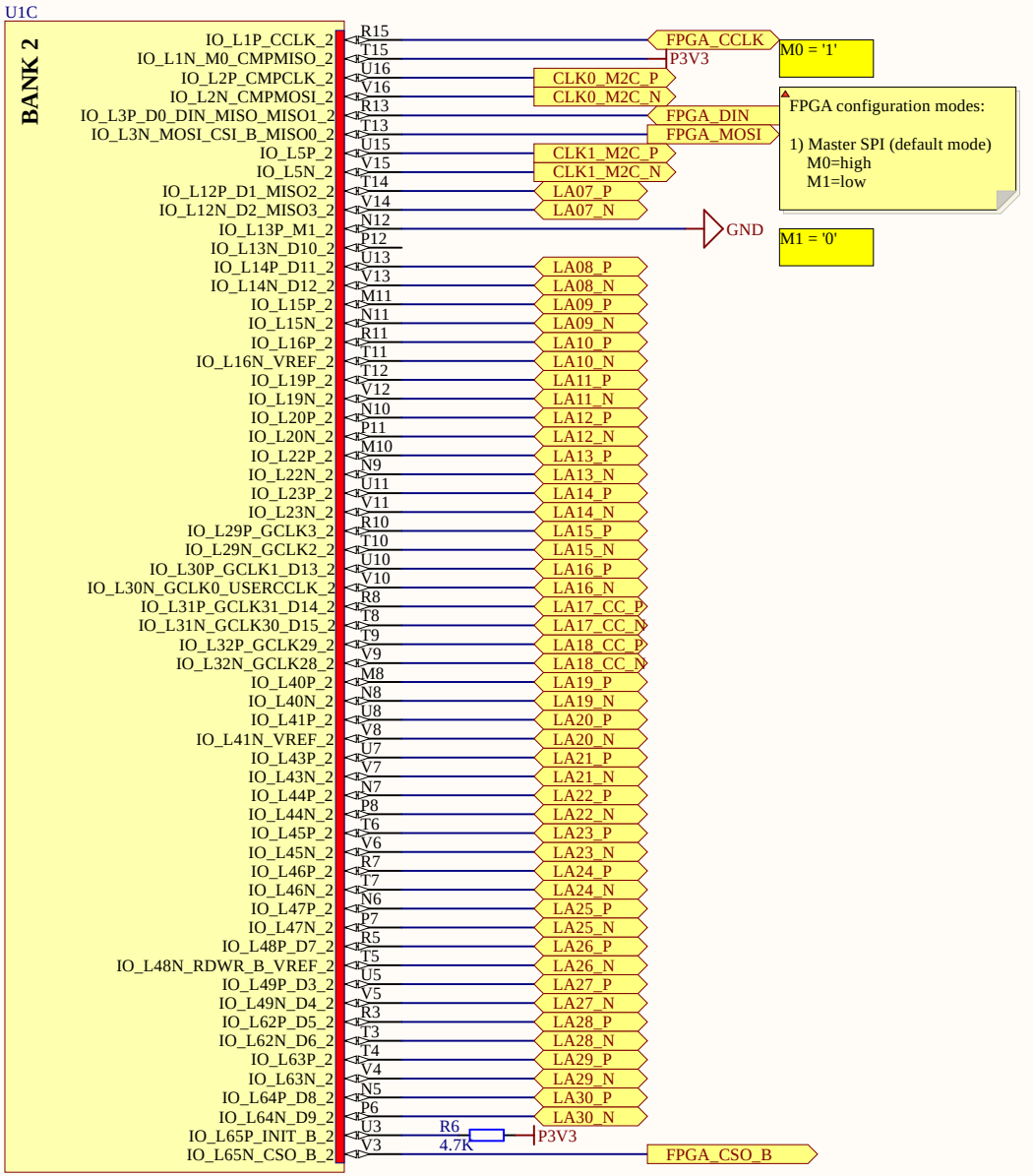

Title	CUTEWR-DP		
Size: A4	Number:4.	Revision: V2	
Date: 2017/02/14		14	
File: 4-FPGA_bank2.SchDoc			

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Bank 3 DOESNT Supports differential output

U1D

BANK 3

IO_L1P_3	N4	
IO_L1N_VREF_3	N3	
IO_L2P_3	P4	
IO_L2N_3	P3	PMOD_1_7
IO_L31P_3	L6	
IO_L31N_VREF_3	M5	
IO_L32P_M3DQ14_3	U2	FMC_PRT / PRSNT_M2C_L
IO_L32N_M3DQ15_3	U1	
IO_L33P_M3DQ12_3	T2	PG_C2M / PG_C2M
IO_L33N_M3DQ13_3	T1	PMOD_1_1
IO_L34P_M3UDQS_3	P2	PMOD_2_3
IO_L34N_M3UDQSN_3	P1	PMOD_2_10
IO_L35P_M3DQ10_3	N2	PMOD_2_4
IO_L35N_M3DQ11_3	N1	PMOD_2_2
IO_L36P_M3DQ8_3	M3	
IO_L36N_M3DQ9_3	M1	PMOD_2_8
IO_L37P_M3DQ0_3	L2	PMOD_2_9
IO_L37N_M3DQ1_3	L1	PMOD_2_7
IO_L38P_M3DQ2_3	K2	PMOD_2_1
IO_L38N_M3DQ3_3	K1	USR_LEMO1 / USR_LEMO1
IO_L39P_M3LDQS_3	L4	
IO_L39N_M3LDQSN_3	L3	
IO_L40P_M3DQ6_3	J3	USR_LEMO2 / USR_LEMO2
IO_L40N_M3DQ7_3	J1	ONE_WIRE / ONE_WIRE
IO_L41P_GCLK27_M3DQ4_3	H2	UART_RX / UART_RX
IO_L41N_GCLK26_M3DQ5_3	H1	CLK20 / CLK20
IO_L42P_GCLK25_TRDY2_M3UDM_3	K4	LA31_P / LA31_P
IO_L42N_GCLK24_M3LDM_3	K3	LA31_N / LA31_N
IO_L43P_GCLK23_M3RASN_3	L5	LA32_P / LA32_P
IO_L43N_GCLK22_IRDY2_M3CASN_3	K5	LA32_N / LA32_N
IO_L44P_GCLK21_M3A5_3	H4	
IO_L44N_GCLK20_M3A6_3	H3	UART_TX / UART_TX
IO_L45P_M3A3_3	L7	
IO_L45N_M3ODT_3	K6	
IO_L46P_M3CLK_3	G3	USR_BUTTON / USR_BUTTON
IO_L46N_M3CLKN_3	G1	CLR_N / PLLDAC_CLR_N
IO_L47P_M3A0_3	J7	
IO_L47N_M3A1_3	J6	
IO_L48P_M3BA0_3	F2	SFP0_TX_DISABLE / SFP0_TX_DISABLE
IO_L48N_M3BA1_3	F1	LOAC_N / PLLDAC_LOAC_N
IO_L49P_M3A7_3	H6	
IO_L49N_M3A2_3	H5	
IO_L50P_M3WE_3	E3	SFP0_MOD_DEF1 / SFP0_MOD_DEF1
IO_L50N_M3BA2_3	E1	PLLDAC_SYNC_N / PLLDAC_SYNC_N
IO_L51P_M3A10_3	F4	
IO_L51N_M3A4_3	F3	SFP0_TX_FAULT / SFP0_TX_FAULT
IO_L52P_M3A8_3	D2	SFP0_MOD_DEF0 / SFP0_MOD_DEF0
IO_L52N_M3A9_3	D1	PLLDAC_SCLK / PLLDAC_SCLK
IO_L53P_M3CKE_3	H7	LA33_P / LA33_P
IO_L53N_M3A12_3	G6	LA33_N / LA33_N
IO_L54P_M3RESET_3	E4	SFP0_MOD_DEF2 / SFP0_MOD_DEF2
IO_L54N_M3A11_3	D3	SFP0_TX_LOS / SFP0_TX_LOS
IO_L55P_M3A13_3	F6	
IO_L55N_M3A14_3	F5	
IO_L83P_3	C2	SFP0_LED / SFP0_LED
IO_L83N_VREF_3	C1	DIN / PLLDAC_DIN

XC6SLX45T-3CSG324C

Title	CUTEWR-DP		
Size: A4	Number:5.	Revision: V2	
Date: 2017/02/14		14	
File: 5-FPGA_bank3.SchDoc			

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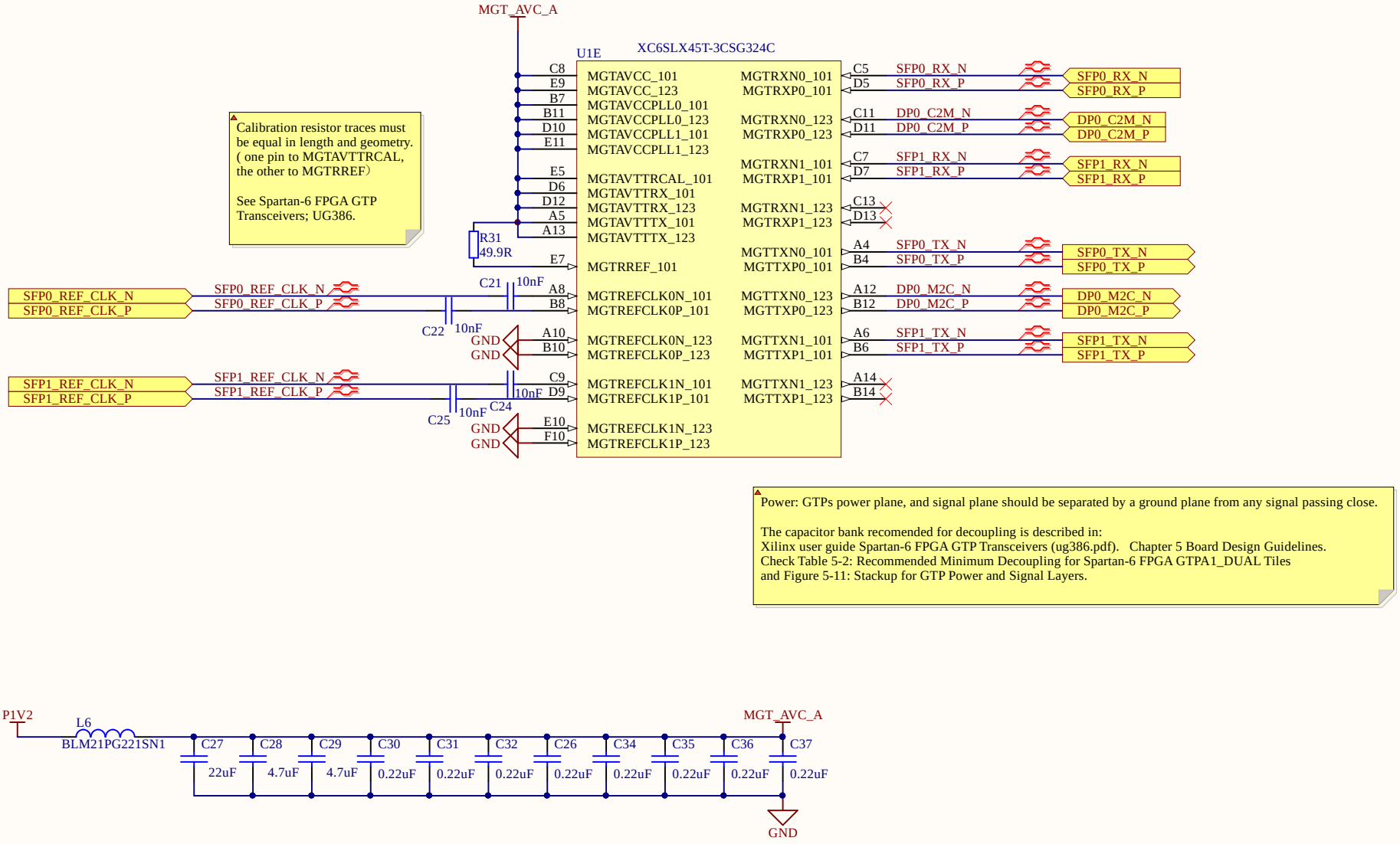
MGT_AVC_A
U1E
XC6SLX45T-3CSG324C
Calibration resistor traces must be equal in length and geometry. (one pin to MGTAVTTRCAL, the other to MGTRREF）
See Spartan-6 FPGA GTP Transceivers; UG386.
R31
49.9R
SFP0_REF_CLK_N
SFP0_REF_CLK_P
SFP1_REF_CLK_N
SFP1_REF_CLK_P
C21 10nF
C22 10nF
C24 10nF
C25 10nF
GND
MGTAVCC_101
MGTAVCC_123
MGTAVCCPLL0_101
MGTAVCCPLL0_123
MGTAVCCPLL1_101
MGTAVCCPLL1_123
MGTAVTTRCAL_101
MGTAVTTRX_101
MGTAVTTRX_123
MGTAVTTTX_101
MGTAVTTTX_123
MGTTREF_101
MGTREFCLK0N_101
MGTREFCLK0P_101
MGTREFCLK0N_123
MGTREFCLK0P_123
MGTREFCLK1N_101
MGTREFCLK1P_101
MGTREFCLK1N_123
MGTREFCLK1P_123
MGTRXN0_101
MGTRXP0_101
MGTRXN0_123
MGTRXP0_123
MGTRXN1_101
MGTRXP1_101
MGTRXN1_123
MGTRXP1_123
MGTTXN0_101
MGTTXP0_101
MGTTXN0_123
MGTTXP0_123
MGTTXN1_101
MGTTXP1_101
MGTTXN1_123
MGTTXP1_123
SFP0_RX_N
SFP0_RX_P
DP0_C2M_N
DP0_C2M_P
SFP1_RX_N
SFP1_RX_P
SFP0_TX_N
SFP0_TX_P
DP0_M2C_N
DP0_M2C_P
SFP1_TX_N
SFP1_TX_P
Power: GTPs power plane, and signal plane should be separated by a ground plane from any signal passing close.
The capacitor bank recomended for decoupling is described in:
Xilinx user guide Spartan-6 FPGA GTP Transceivers (ug386.pdf). Chapter 5 Board Design Guidelines.
Check Table 5-2: Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles
and Figure 5-11: Stackup for GTP Power and Signal Layers.
P1V2
L6
BLM21PG221SN1
C27 22uF
C28 4.7uF
C29 4.7uF
C30 0.22uF
C31 0.22uF
C32 0.22uF
C26 0.22uF
C34 0.22uF
C35 0.22uF
C36 0.22uF
C37 0.22uF
GND
Title CUTEWR-DP
Size: A4
Number:6.
Revision: V2
Date: 2017/02/14
14
File: 6-FPGA_GTP.SchDoc
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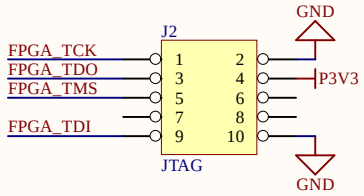
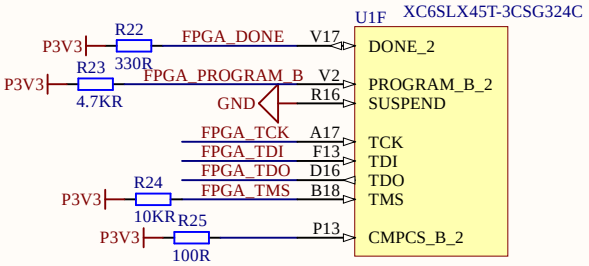
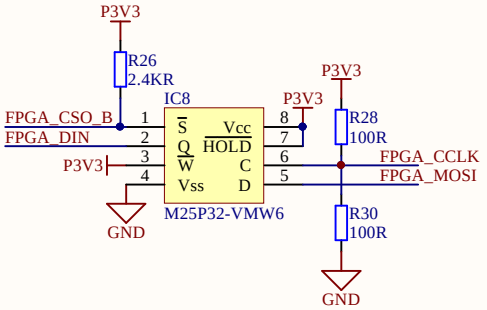
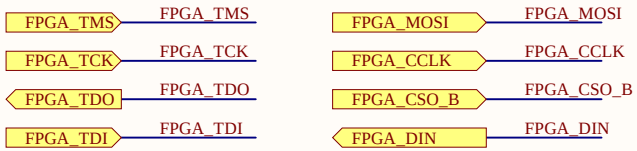


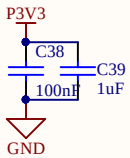




When CS_n is high, Q will stay high impedence



CCLK Termination. See Spartan6 FPGA Configuration User Guide P52



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Size: A4	Number:7.	Revision: V2	
Date: 2017/02/14		14	
File: 7-FPGA_Config.SchDoc			

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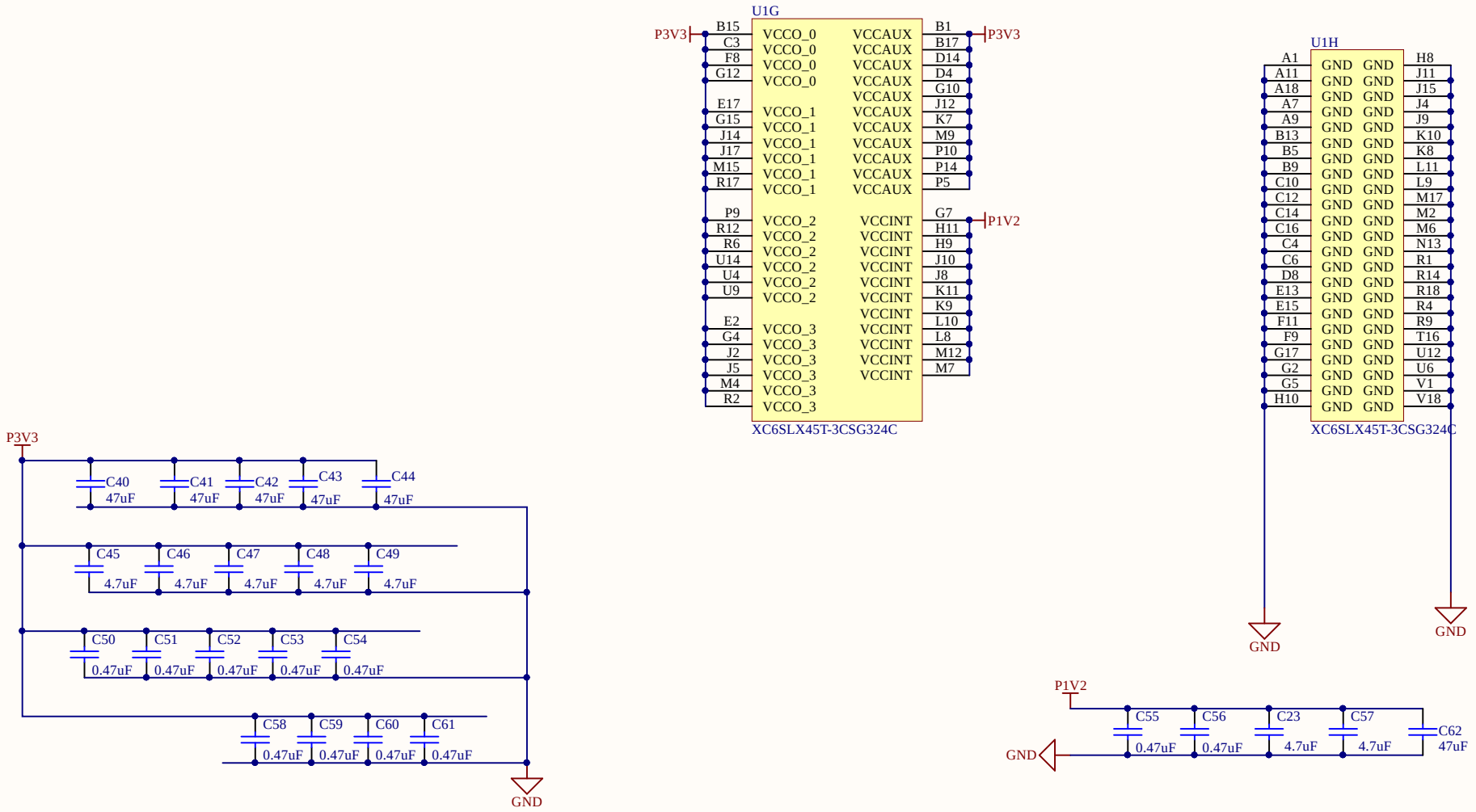

Title	CUTEWR-DP		
Size: A4	Number:8.	Revision: V3	
Date: 2017/02/14		14	
File: 8-FPGA_Power.SchDoc			

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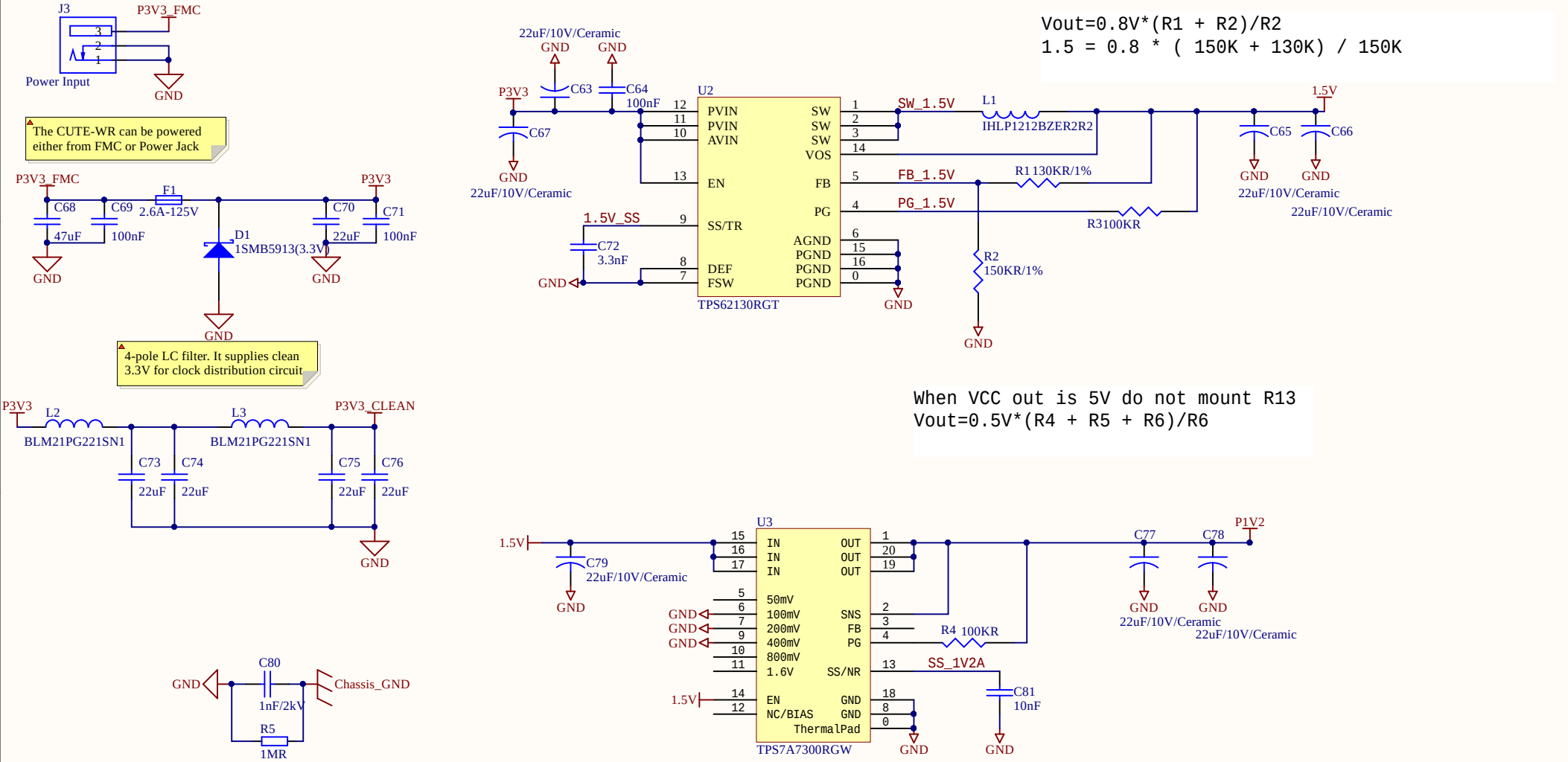

Title	CUTEWR-DP		
Size: A4	Number:9.	Revision: V2	
Date: 2017/02/14		14	
File: 9-Power.SchDoc			

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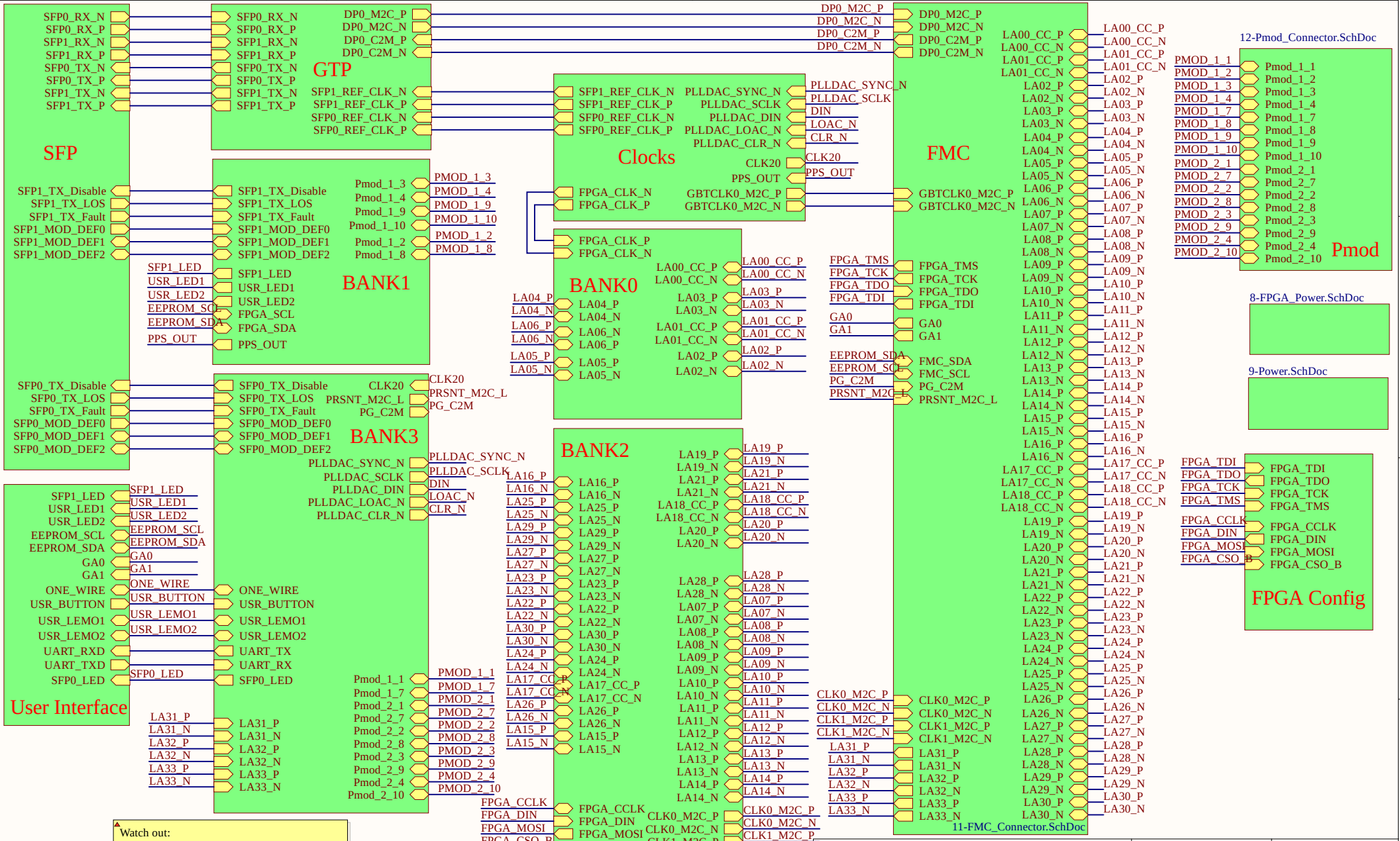
SFP
SFP0_RX_N
SFP0_RX_P
SFP1_RX_N
SFP1_RX_P
SFP0_TX_N
SFP0_TX_P
SFP1_TX_N
SFP1_TX_P
GTP
SFP1_REF_CLK_N
SFP1_REF_CLK_P
SFP0_REF_CLK_N
SFP0_REF_CLK_P
DP0_M2C_P
DP0_M2C_N
DP0_C2M_P
DP0_C2M_N
Clocks
PLLDAC_SYNC_N
PLLDAC_SCLK
PLLDAC_DIN
PLLDAC_LOAC_N
PLLDAC_CLR_N
DIN
LOAC_N
CLR_N
CLK20
PPS_OUT
FPGA_CLK_N
FPGA_CLK_P
GBTCLK0_M2C_P
GBTCLK0_M2C_N
FMC
BANK1
SFP1_TX_Disable
SFP1_TX_LOS
SFP1_TX_Fault
SFP1_MOD_DEF0
SFP1_MOD_DEF1
SFP1_MOD_DEF2
SFP1_LED
USR_LED1
USR_LED2
EEPROM_SCL
EEPROM_SDA
FPGA_SCL
FPGA_SDA
PPS_OUT
Pmod_1_3
Pmod_1_4
Pmod_1_9
Pmod_1_10
Pmod_1_2
Pmod_1_8
PMOD_1_3
PMOD_1_4
PMOD_1_9
PMOD_1_10
PMOD_1_2
PMOD_1_8
BANK0
LA00_CC_P
LA00_CC_N
LA03_P
LA03_N
LA01_CC_P
LA01_CC_N
LA02_P
LA02_N
LA04_P
LA04_N
LA06_P
LA06_N
LA05_P
LA05_N
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
GA0
GA1
EEPROM_SDA
EEPROM_SCL
PG_C2M
PRSNT_M2C_L
FMC_SDA
FMC_SCL
BANK3
SFP0_TX_Disable
SFP0_TX_LOS
SFP0_TX_Fault
SFP0_MOD_DEF0
SFP0_MOD_DEF1
SFP0_MOD_DEF2
CLK20
PRSNT_M2C_L
PG_C2M
PLLDAC_SYNC_N
PLLDAC_SCLK
PLLDAC_DIN
PLLDAC_LOAC_N
PLLDAC_CLR_N
BANK2
LA19_P
LA19_N
LA21_P
LA21_N
LA18_CC_P
LA18_CC_N
LA20_P
LA20_N
LA16_P
LA16_N
LA25_P
LA25_N
LA29_P
LA29_N
LA27_P
LA27_N
LA23_P
LA23_N
LA22_P
LA22_N
LA30_P
LA30_N
LA24_P
LA24_N
LA17_CC_P
LA17_CC_N
LA26_P
LA26_N
LA15_P
LA15_N
LA28_P
LA28_N
LA07_P
LA07_N
LA08_P
LA08_N
LA09_P
LA09_N
LA10_P
LA10_N
LA11_P
LA11_N
LA12_P
LA12_N
LA13_P
LA13_N
LA14_P
LA14_N
CLK0_M2C_P
CLK0_M2C_N
CLK1_M2C_P
CLK1_M2C_N
FPGA_CCLK
FPGA_DIN
FPGA_MOSI
FPGA_CSO_B
User Interface
SFP1_LED
USR_LED1
USR_LED2
EEPROM_SCL
EEPROM_SDA
GA0
GA1
ONE_WIRE
USR_BUTTON
USR_LEMO1
USR_LEMO2
UART_RXD
UART_TXD
SFP0_LED
ONE_WIRE
USR_BUTTON
USR_LEMO1
USR_LEMO2
UART_TX
UART_RX
SFP0_LED
LA31_P
LA31_N
LA32_P
LA32_N
LA33_P
LA33_N
Watch out:
As the LVDS in BANK3 only supports input.
The LA31/LA32/LA33 only supports input!
12-Pmod_Connector.SchDoc
Pmod
Pmod_1_1
Pmod_1_2
Pmod_1_3
Pmod_1_4
Pmod_1_7
Pmod_1_8
Pmod_1_9
Pmod_1_10
Pmod_2_1
Pmod_2_7
Pmod_2_2
Pmod_2_8
Pmod_2_3
Pmod_2_9
Pmod_2_4
Pmod_2_10
8-FPGA_Power.SchDoc
9-Power.SchDoc
FPGA Config
FPGA_TDI
FPGA_TDO
FPGA_TCK
FPGA_TMS
FPGA_CCLK
FPGA_DIN
FPGA_MOSI
FPGA_CSO_B
11-FMC_Connector.SchDoc
Title CUTEWR-DP
Size: A4
Number:0.
Revision: V2
Date: 2017/02/14
File: cutewr_dp.SchDoc
14
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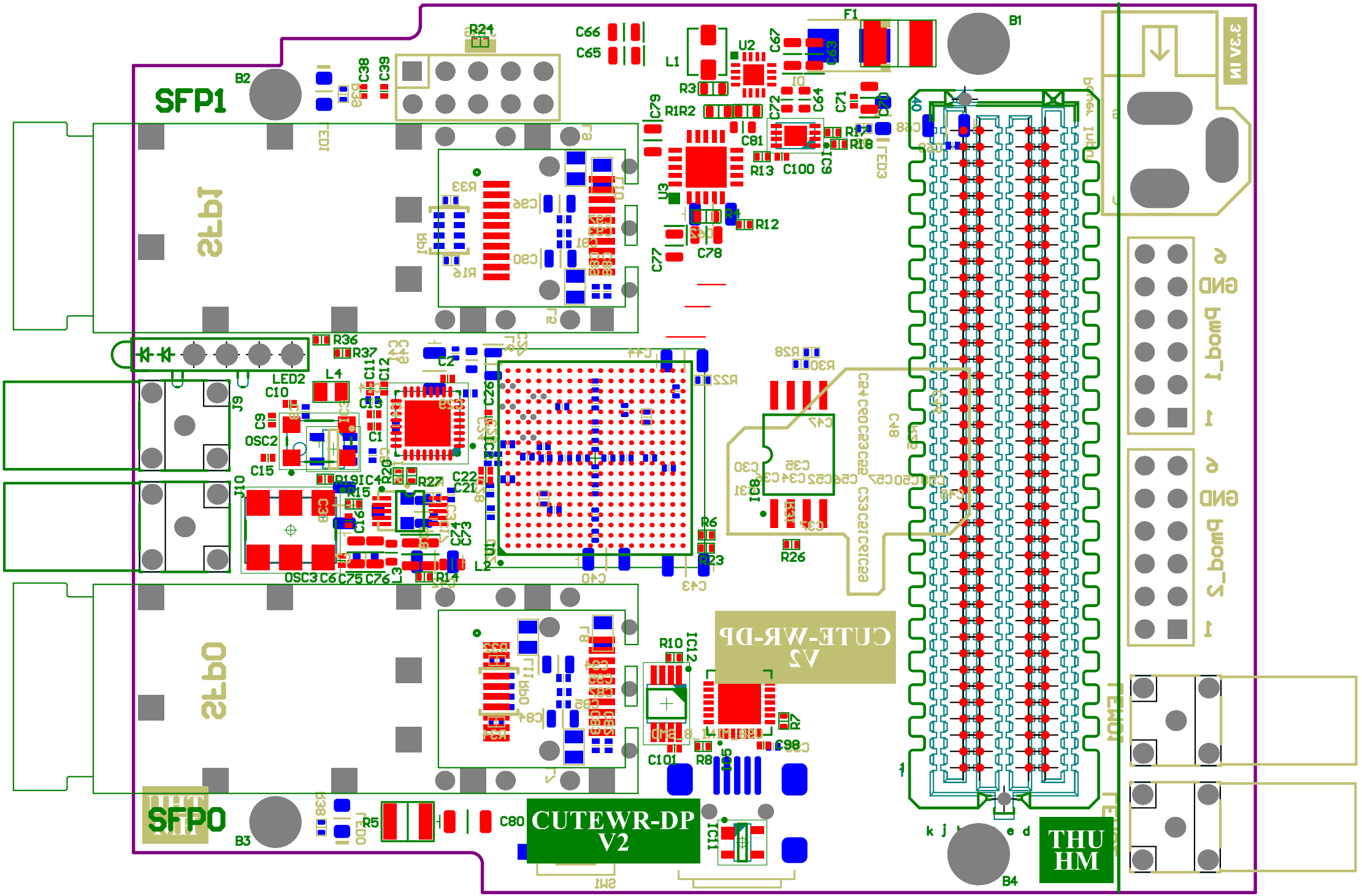
SFP1
SFP0
CUTEWR-DP
V2
THU
HM