

A

A

B

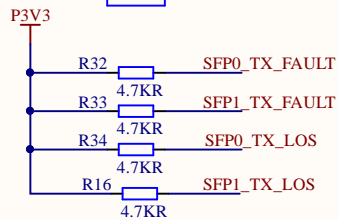
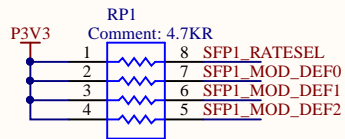
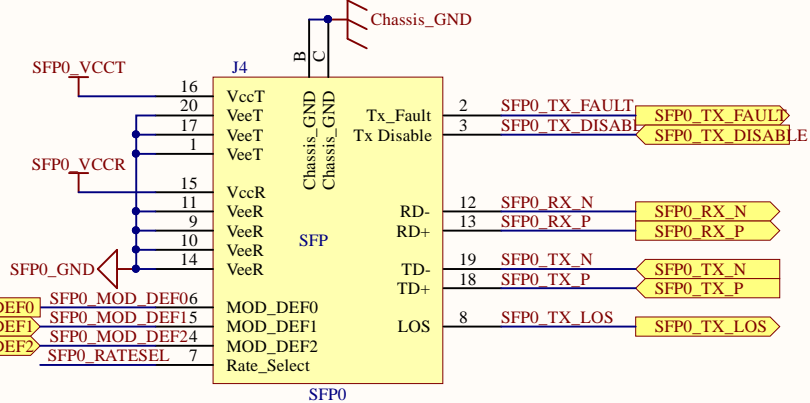
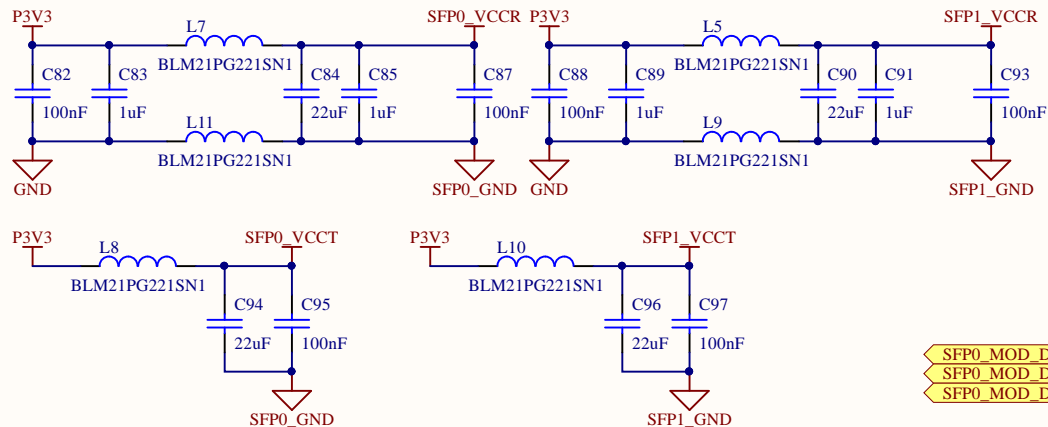
B

C

C

D

D



Title Compact Universal Timing Endpoint

TSINGHUA

Size: A4

Number: *

Revision: V3

hongming

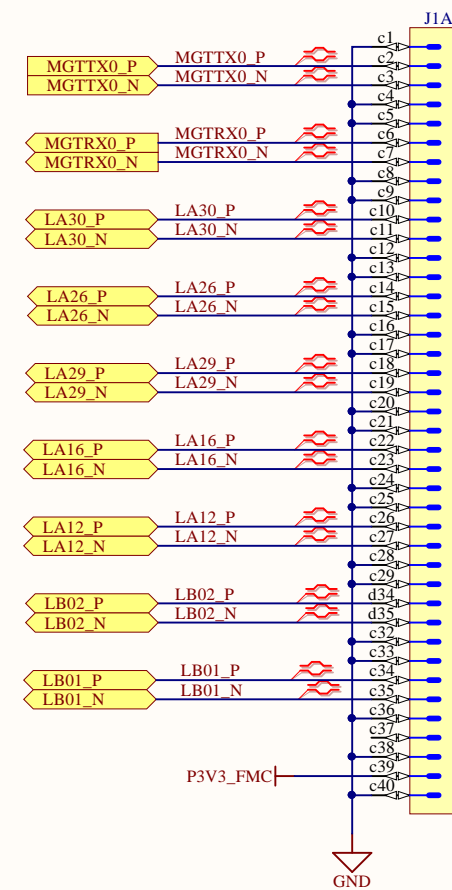
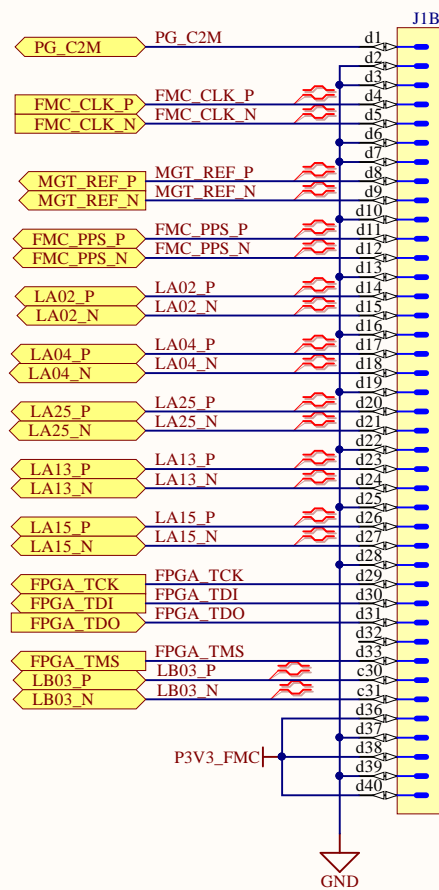
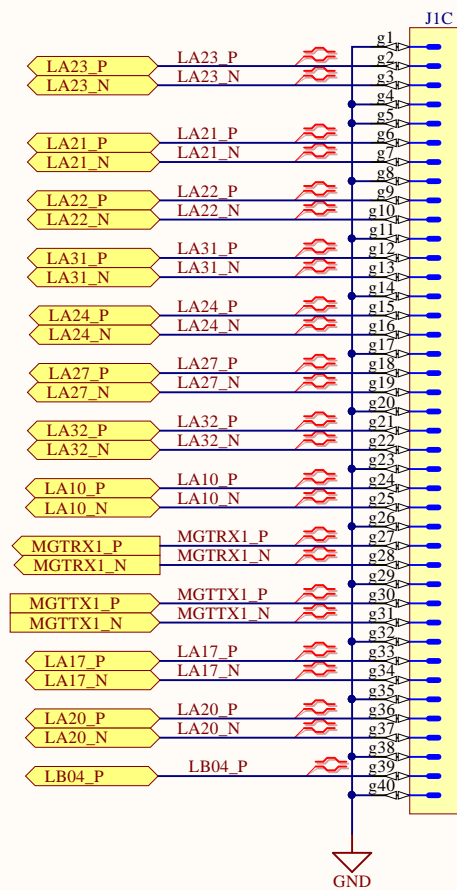
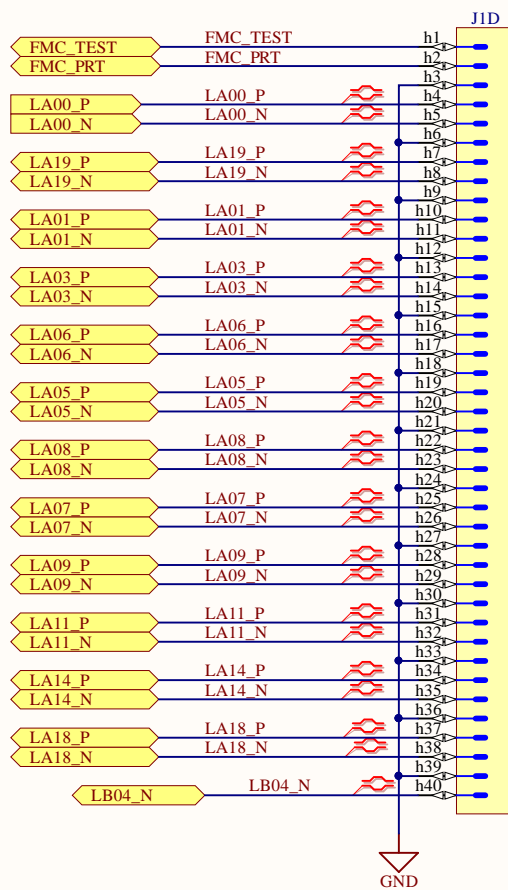
Date: 2015/11/16

14

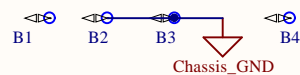
lihm09@foxmail.com

File: 10-SFP.SchDoc





Routing Differences among all FMC Differential Pairs are within 150 mil



Title Compact Universal Timing Endpoint

Size: A4

Number: *

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Date: 2015/11/16

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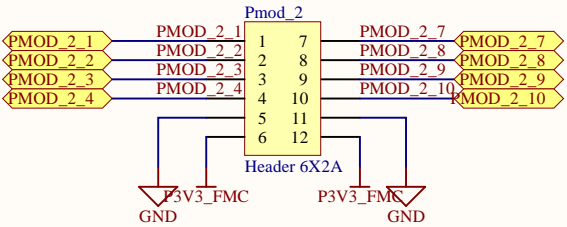
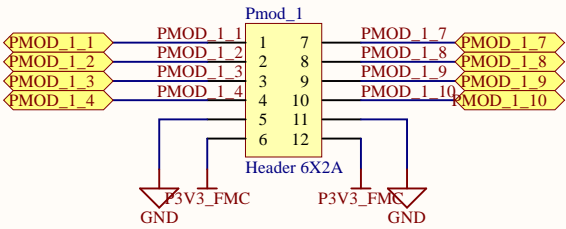
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TSINGHUA

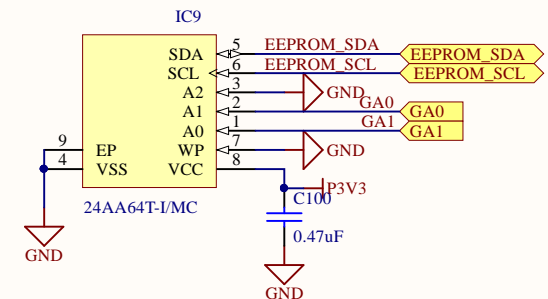
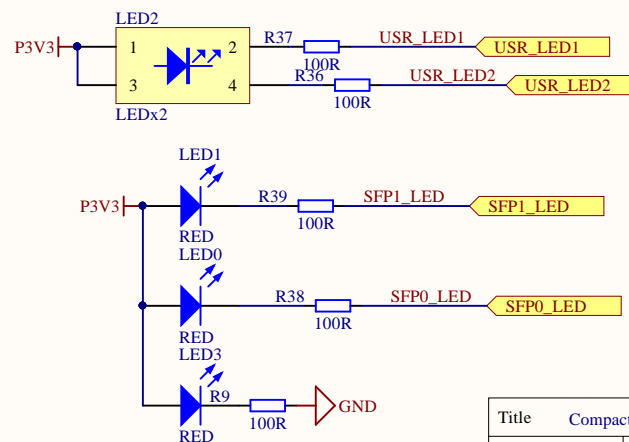
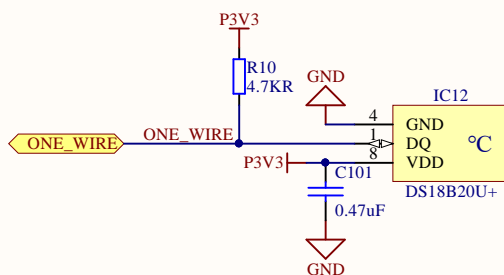
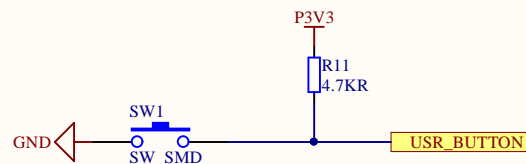
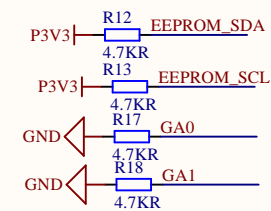
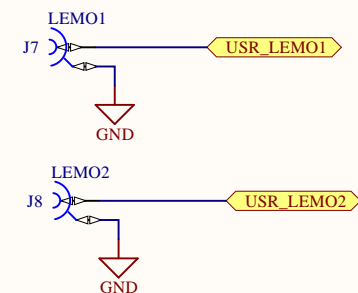
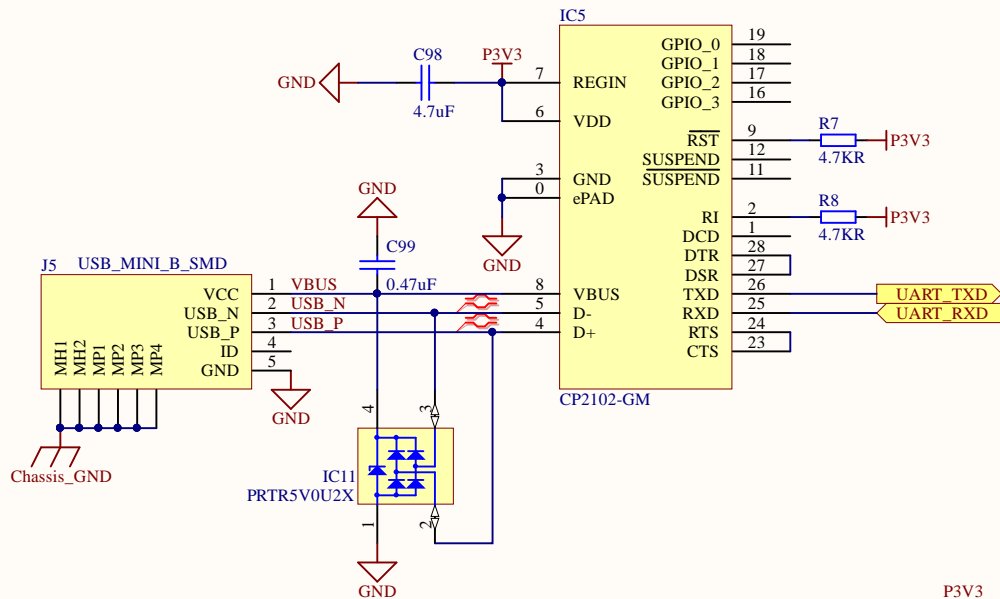
hongming


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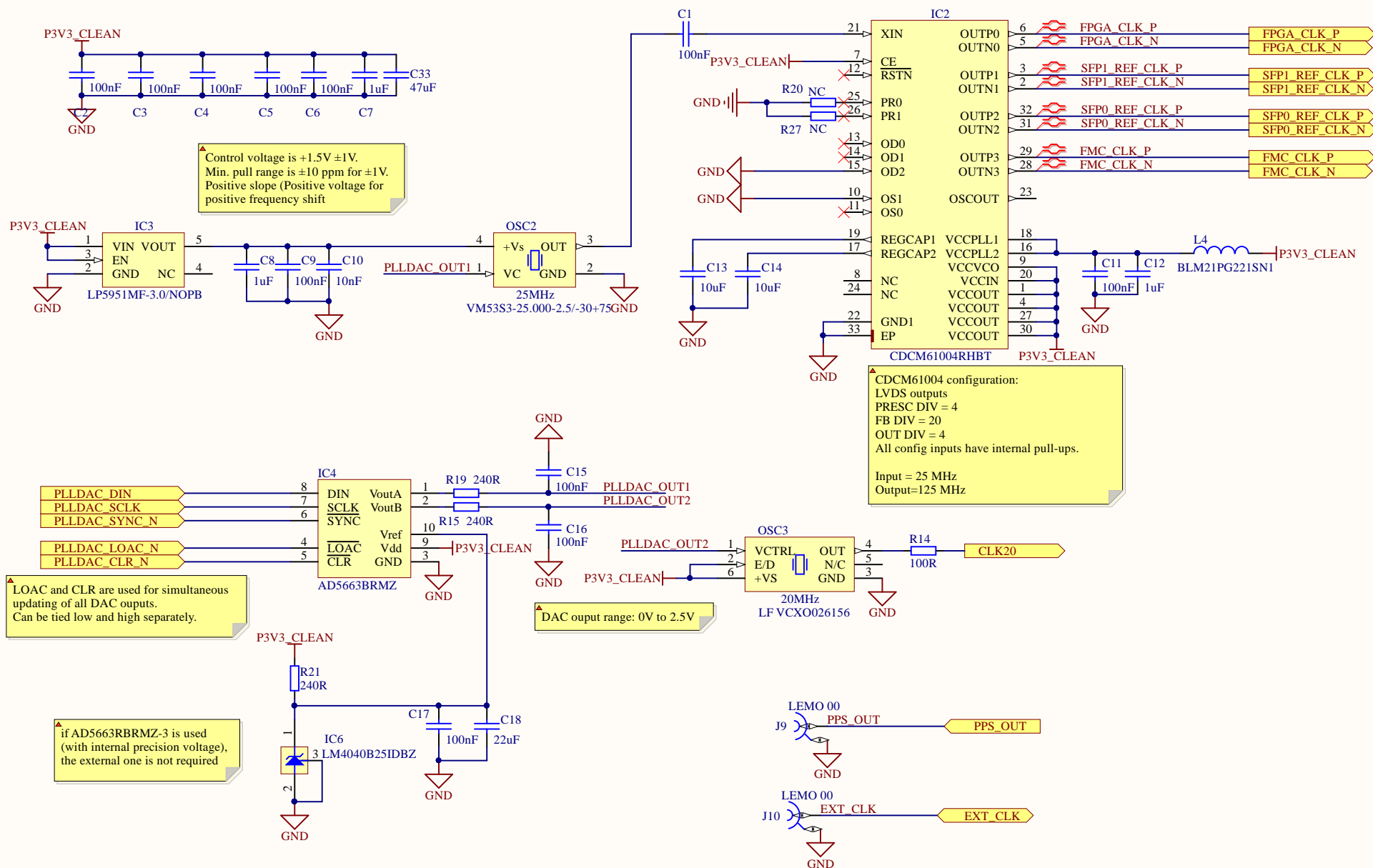





Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 12-Pmod_Connector.SchDoc				

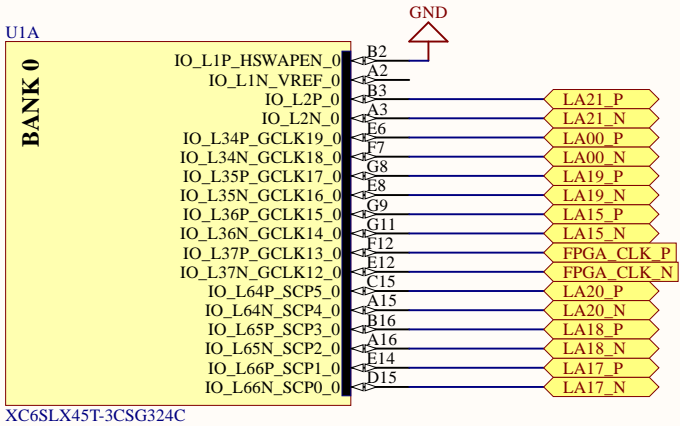



Title Compact Universal Timing Endpoint			TSINGHUA hongming lihnm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 13-User_Interface.SchDoc				



Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 1-Clocks.SchDoc				

Bank 0 Supports differential output

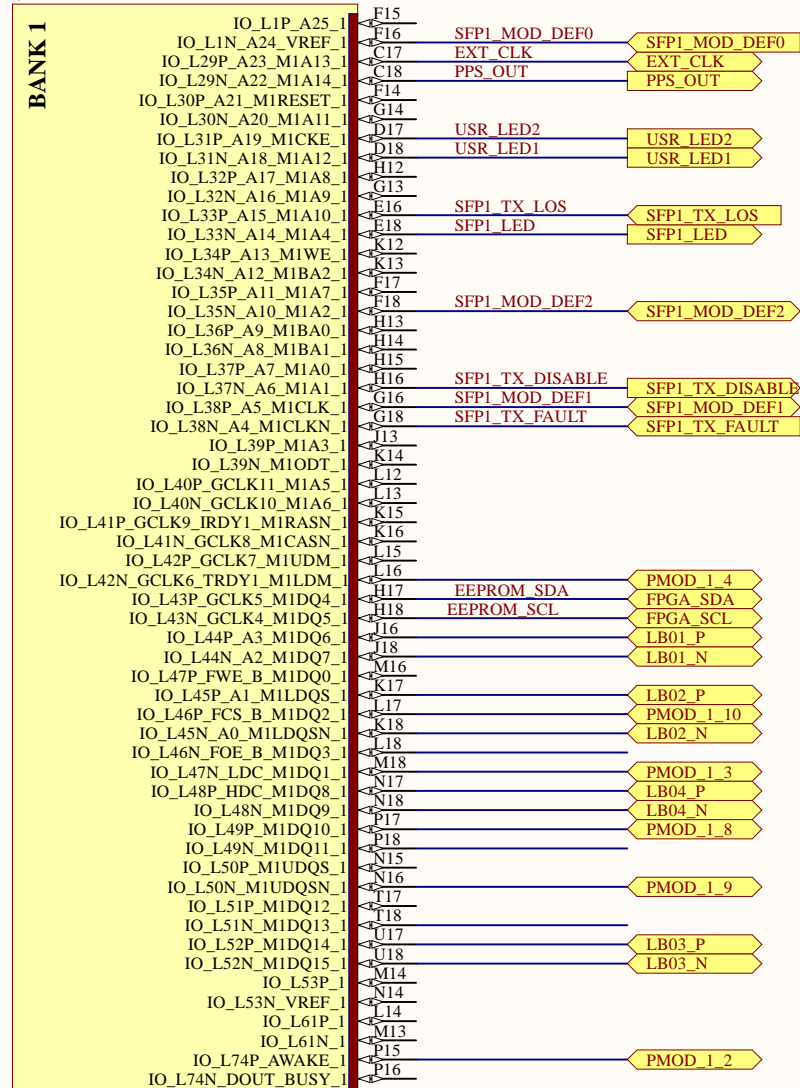


Title Compact Universal Timing Endpoint			<i>TSINGHUA</i> <i>hongming</i> <i>lihm09@foxmail.com</i>	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 2-FPGA_bank0.SchDoc				


Bank 1 DOESN'T Supports differential output

U1B

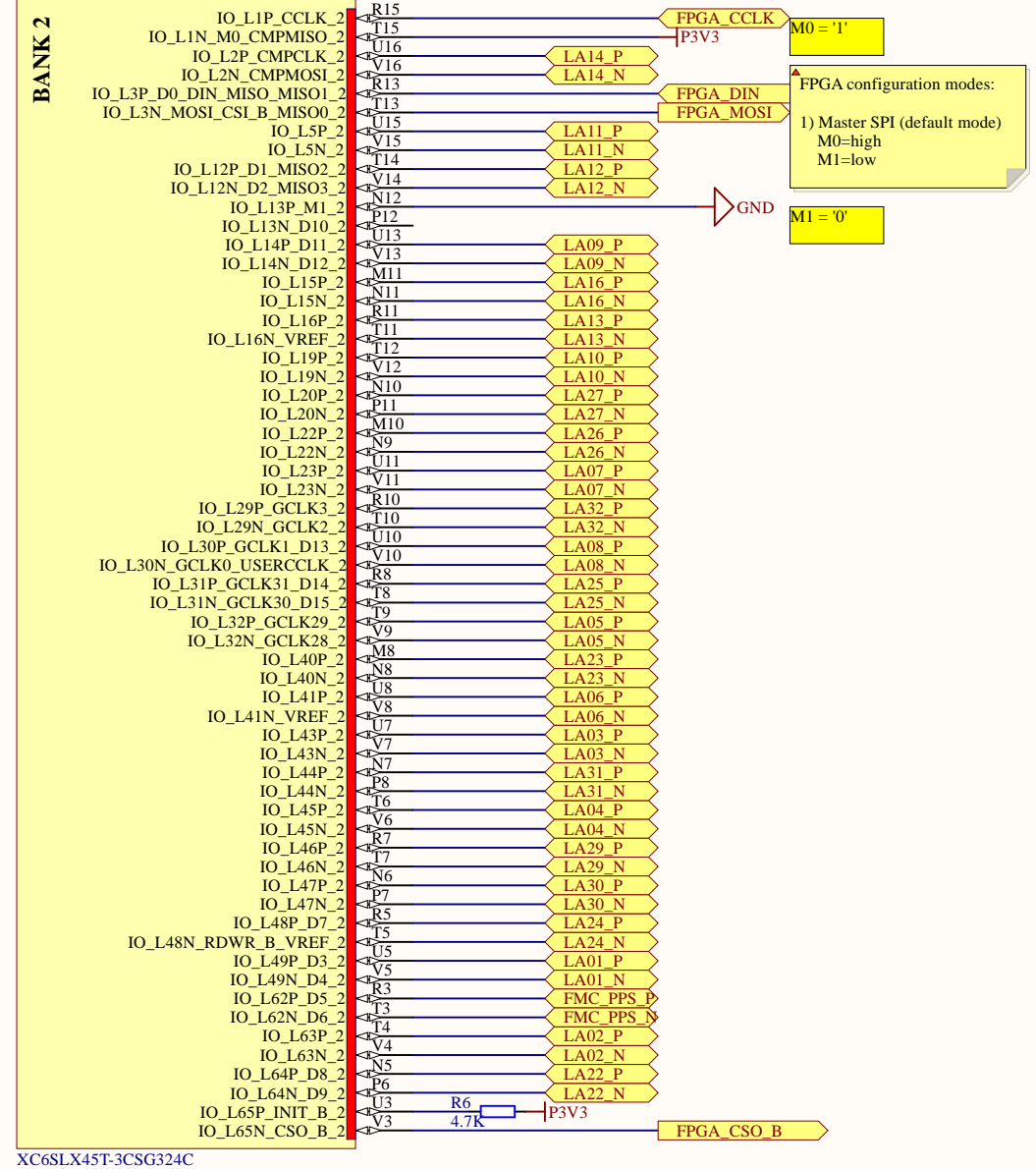
BANK 1




XC6SLX45T-3CSG324C

Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 3-FPGA_bank1.SchDoc				

UIC

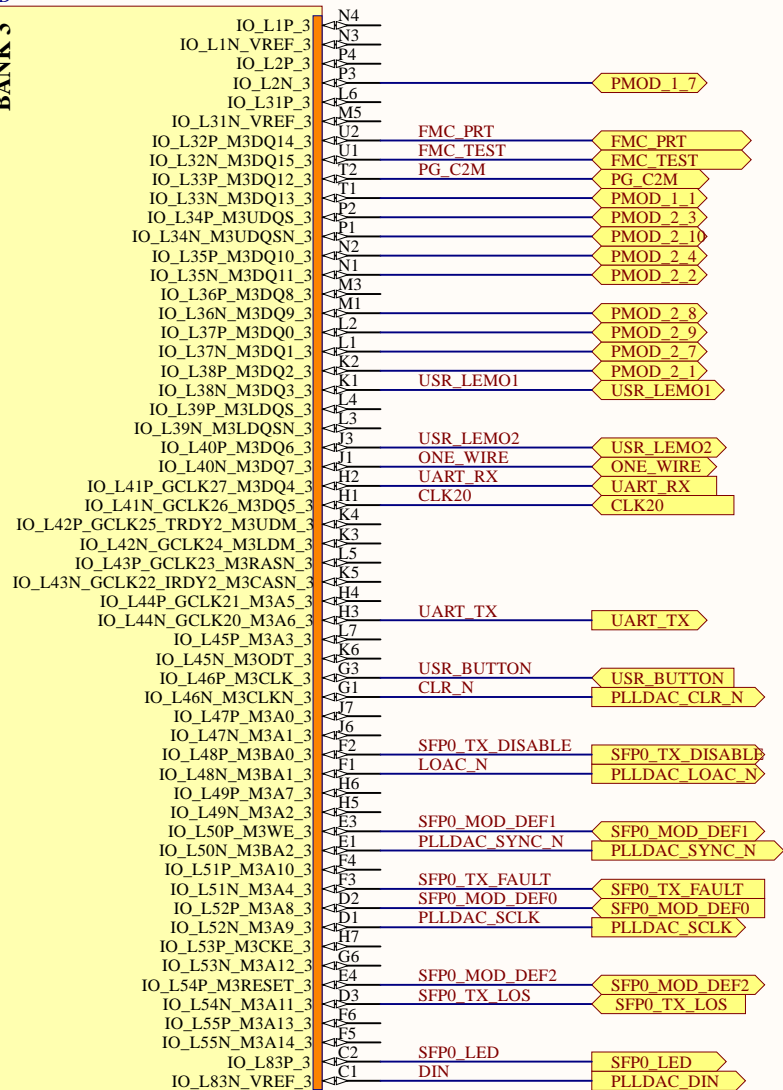


Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 4-FPGA_bank2.SchDoc				


Bank 3 DOESN'T Supports differential output

UID

BANK 3



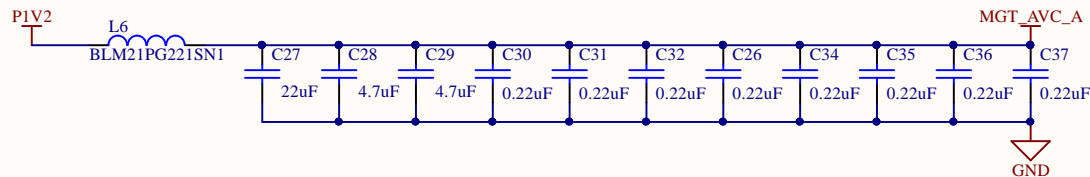
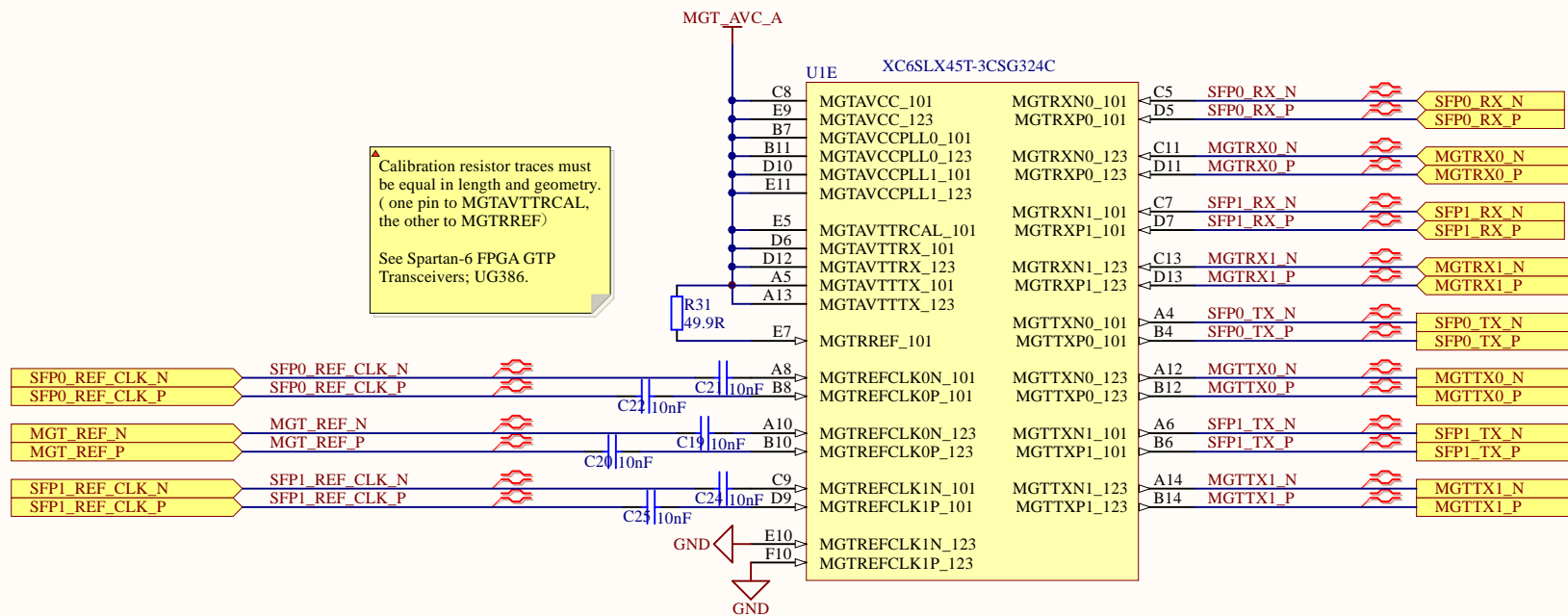
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Title Compact Universal Timing Endpoint			<div>TSINGHUA</div> <div>hongming</div> <div>lihm09@foxmail.com</div>	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 5-FPGA_bank3.SchDoc				

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hongming

lihm09@foxmail.com



Title Compact Universal Timing Endpoint

Size: A4

Number: *

Revision: V3

Date: 2015/11/16

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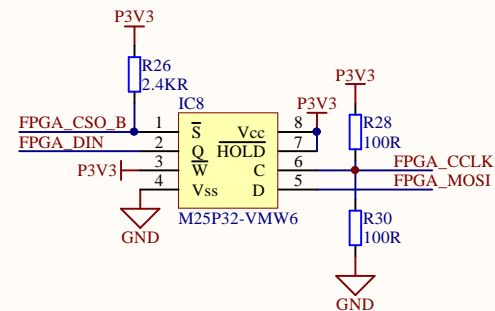
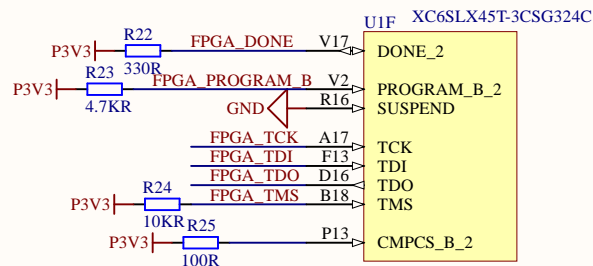
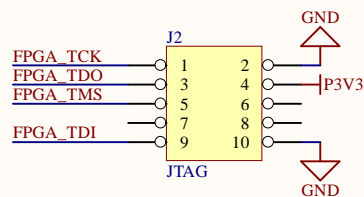
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TSINGHUA

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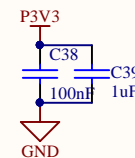
lihm09@foxmail.com




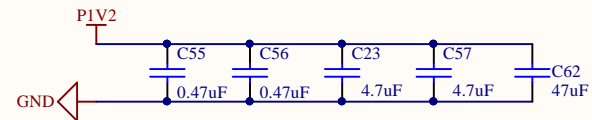
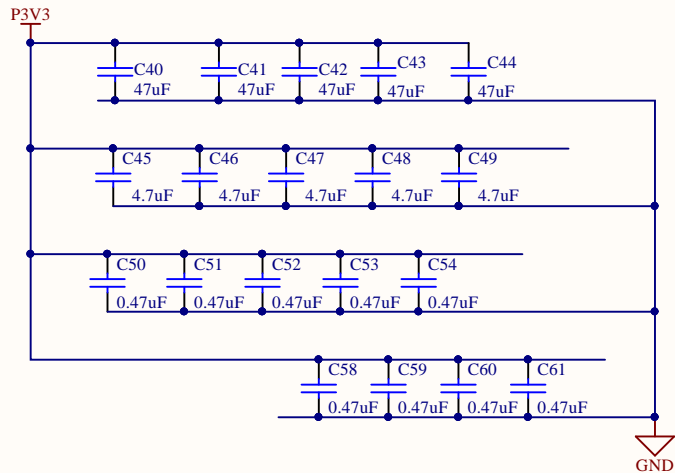
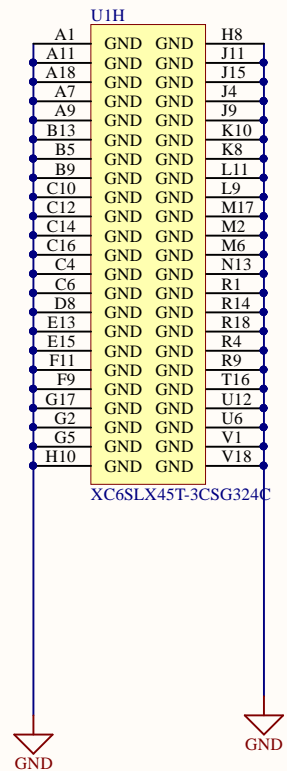
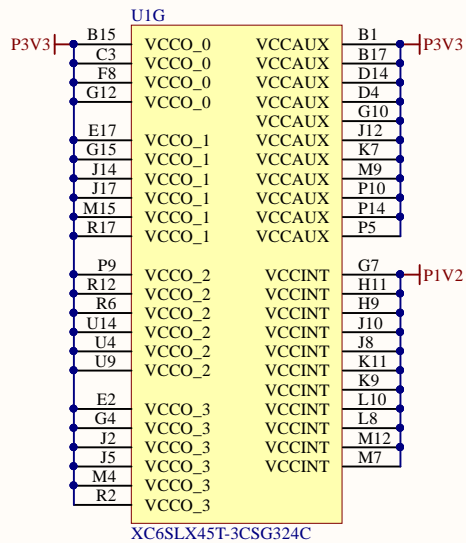



When CS_n is high, Q will stay high impedance

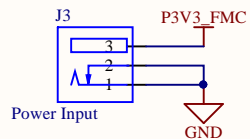
CCLK Termination. See Spartan6 FPGA Configuration User Guide P52



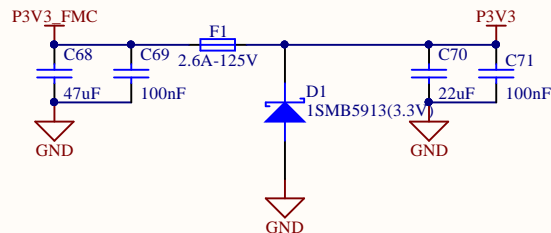
Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 7-FPGA_Config.SchDoc				



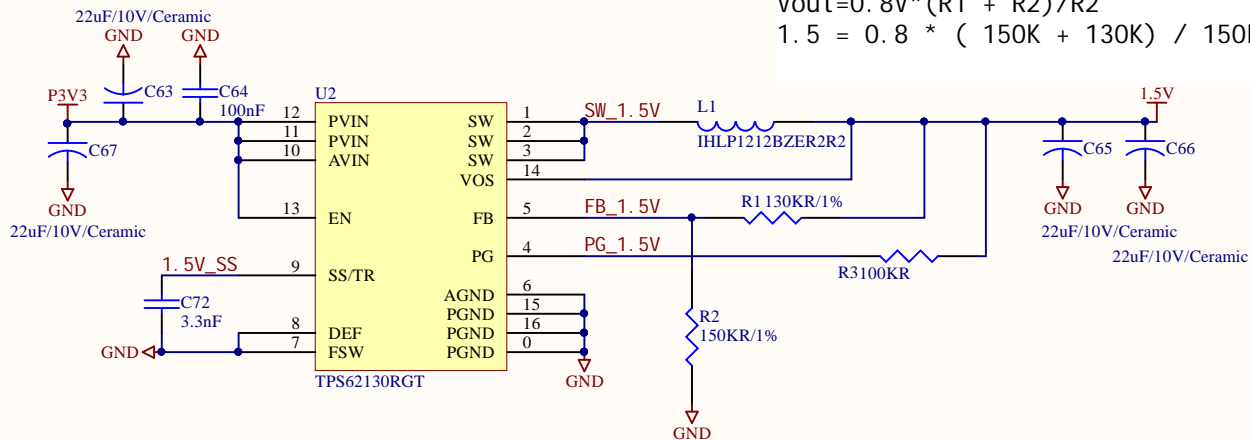
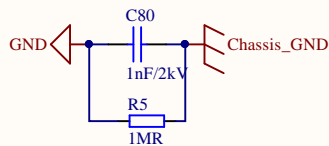
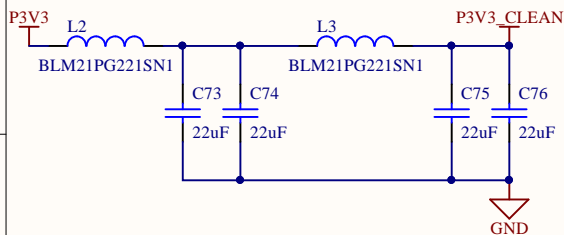
Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 8-FPGA_Power.SchDoc				



The CUTE-WR can be powered either from FMC or Power Jack



4-pole LC filter. It supplies clean 3.3V for clock distribution circuit

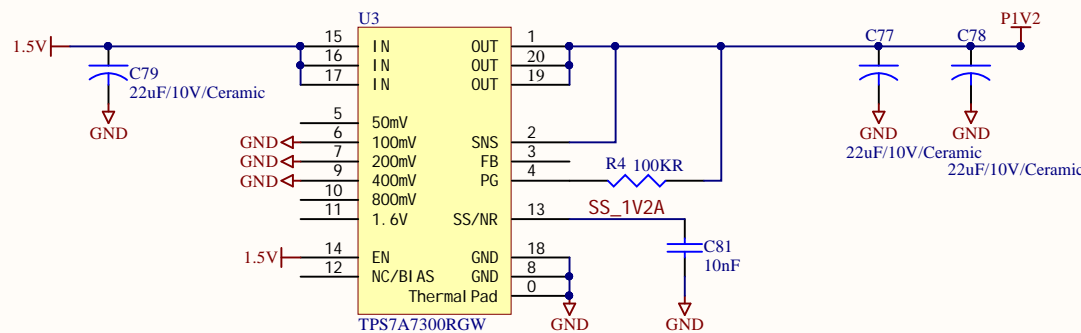



$$V_{out} = 0.8V * (R1 + R2) / R2$$

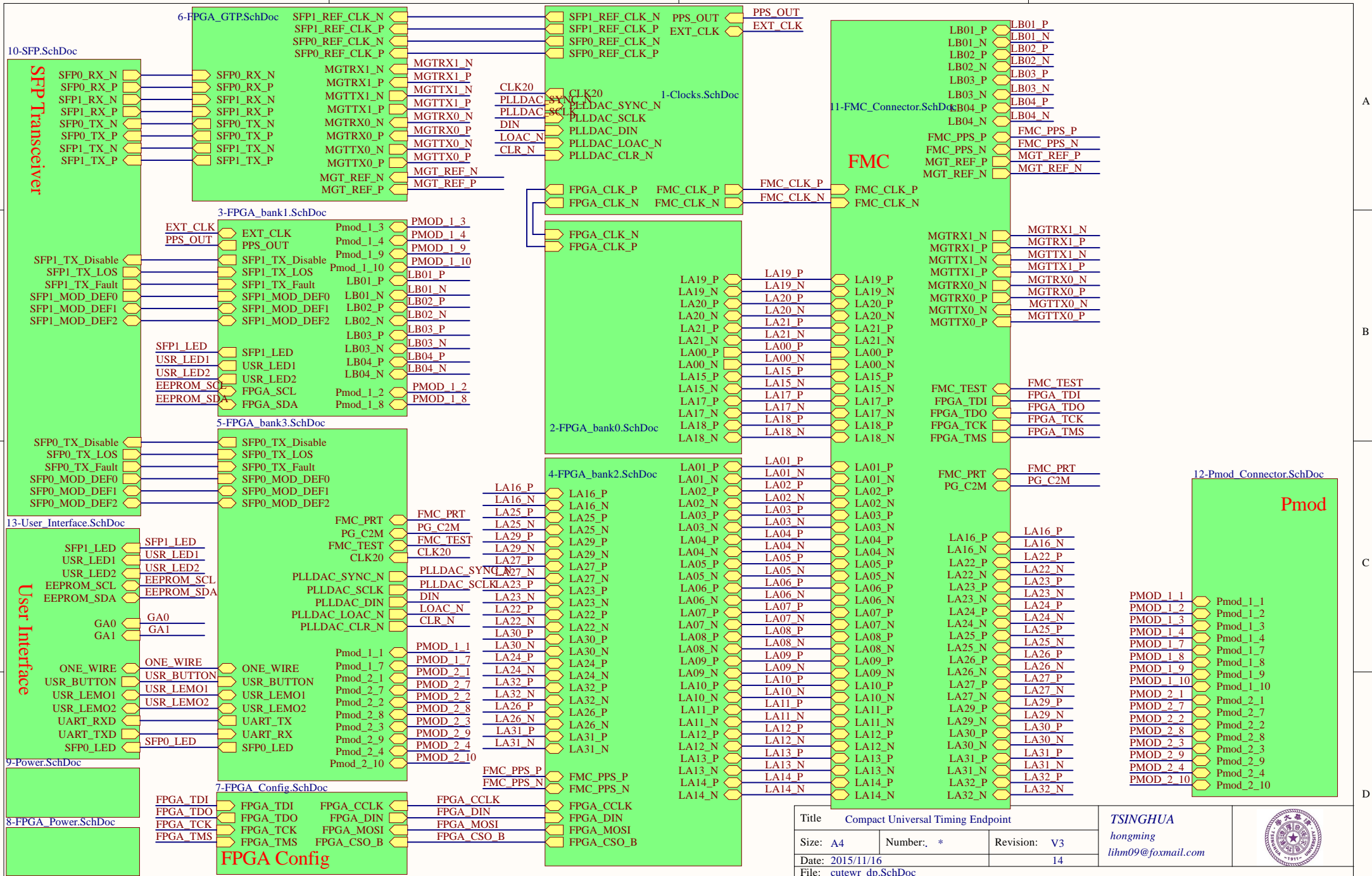
$$1.5 = 0.8 * (150K + 130K) / 150K$$

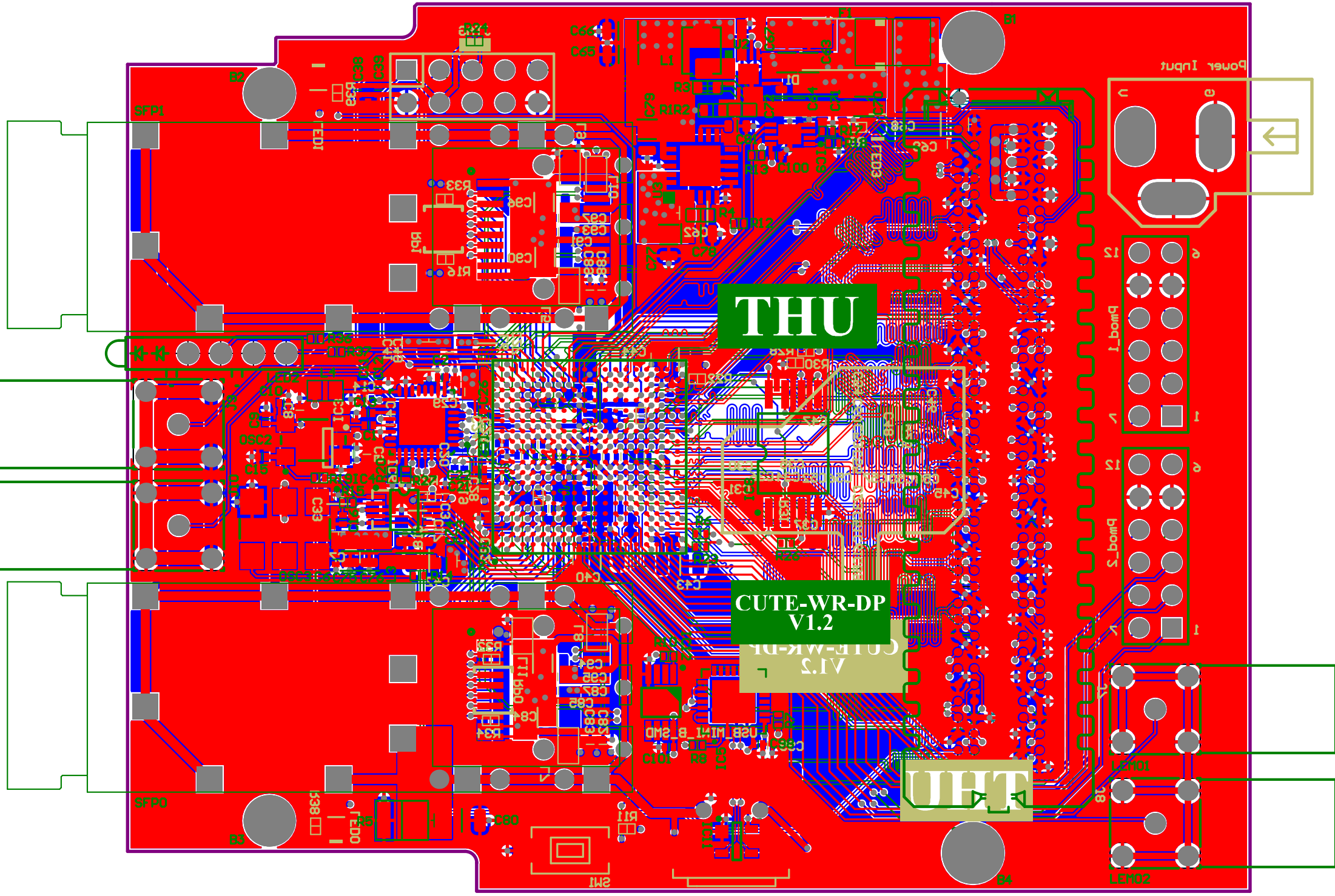
When VCC out is 5V do not mount R13

$$V_{out} = 0.5V * (R4 + R5 + R6) / R6$$



Title Compact Universal Timing Endpoint			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: *	Revision: V3		
Date: 2015/11/16		14		
File: 9-Power.SchDoc				





THU

CUTE-WR-DP
V1.2

U1

CUTE-WR-DP
V1.2

