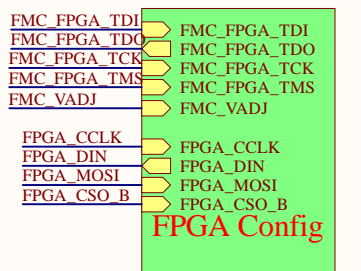
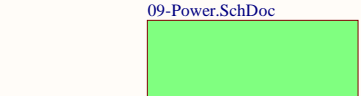
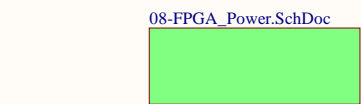
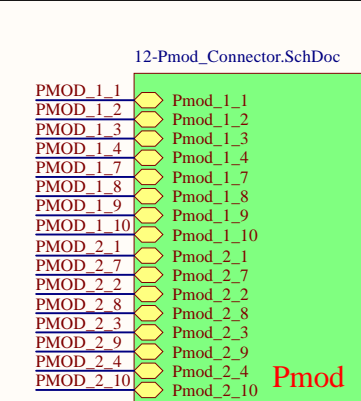
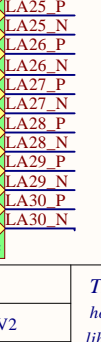
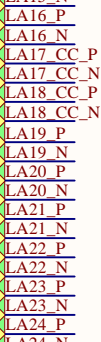
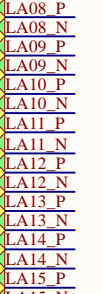
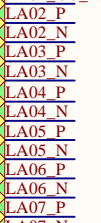
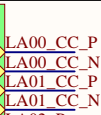
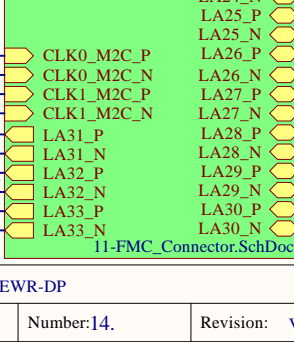
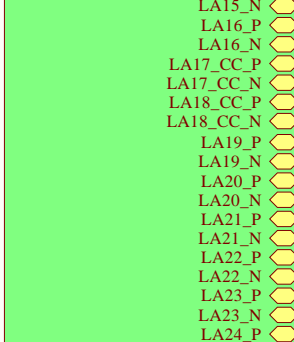
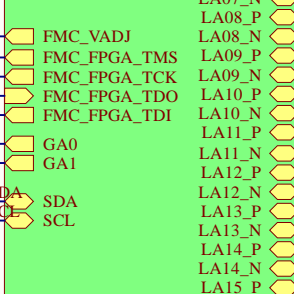
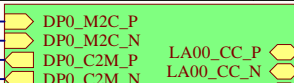
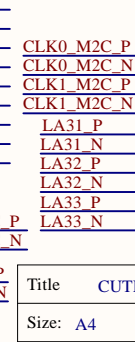
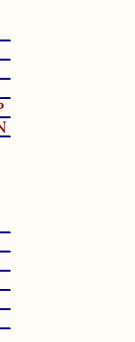
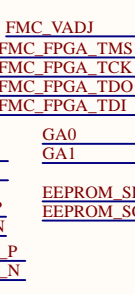
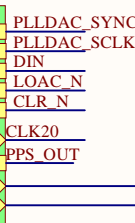
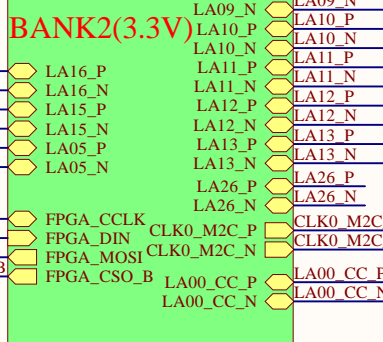
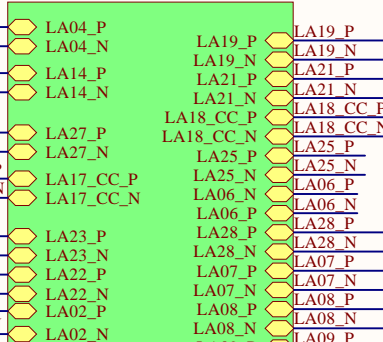
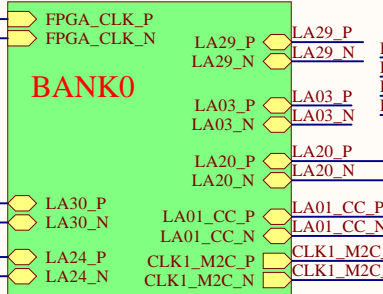
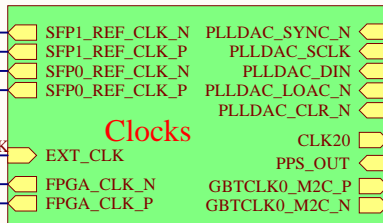
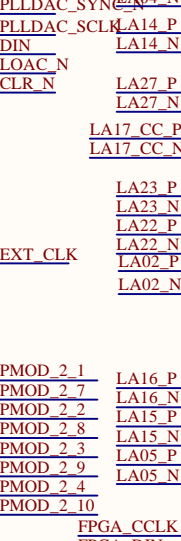
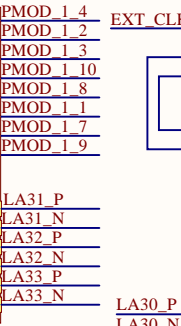
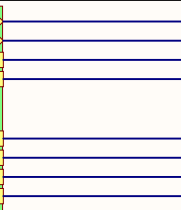


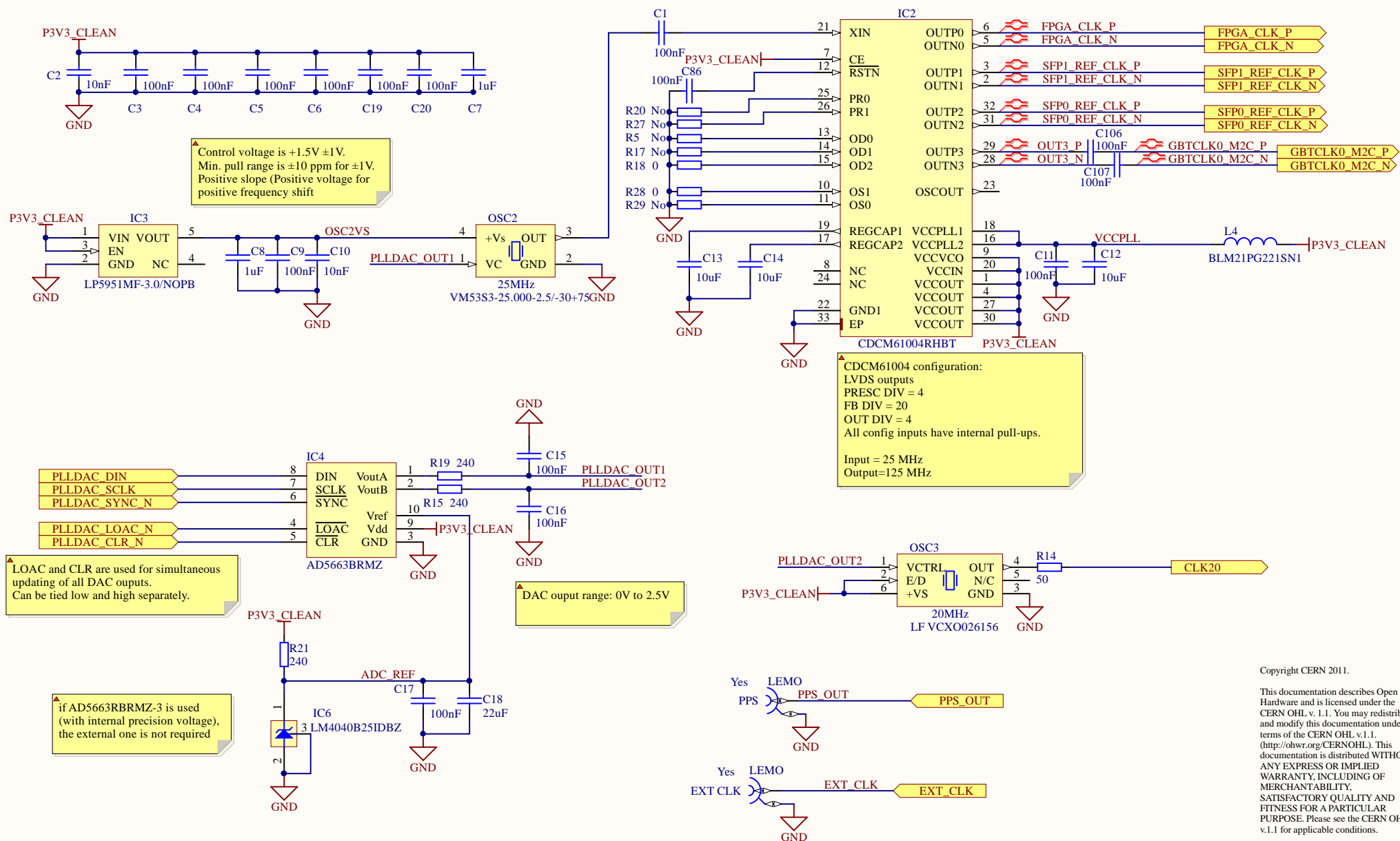
Watch out:  
As the LVDS in BANK3 only supports input.  
The LA31/LA32/LA33 only supports input!




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Title CUTEWR-DP			TSINGHUA	
Size: A4	Number: 14.	Revision: V2	hongming	
Date: 2017/02/14		14	lihm09@foxmail.com	
File: 00cutewr_dp.SchDoc				



Title CUTEWR-DP			TSINGHUA	
Size: A4	Number: 1.	Revision: V2	hongming	
Date: 2017/02/14		14	lihm09@foxmail.com	
File: 01-Clocks.SchDoc				

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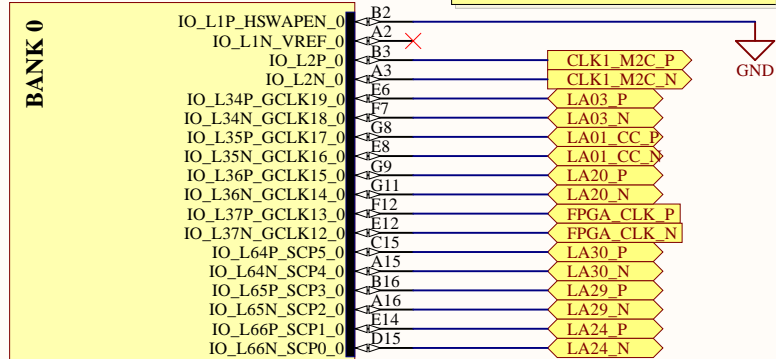
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▲ Bank 0 Supports differential output

VCCO\_0 = 3.3V

U1A


▲ FPGA IO pulled-up during configuration



XC6SLX45T-3CSG324C

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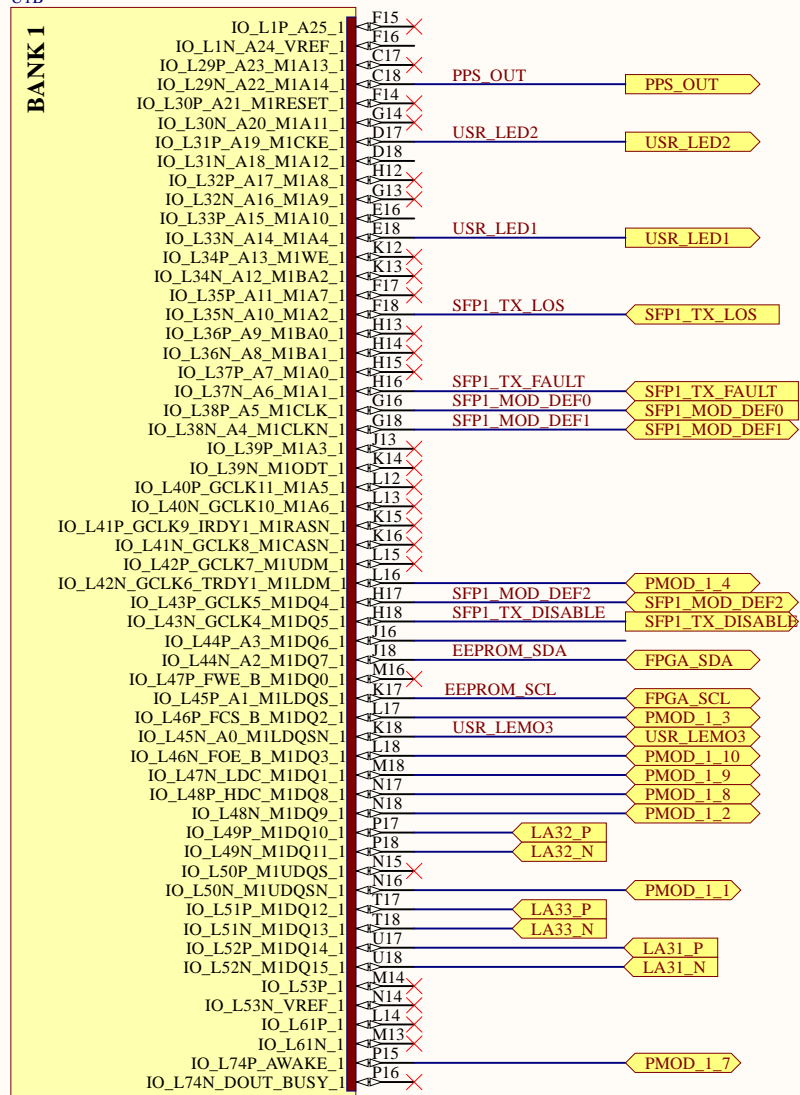
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Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:2.	Revision: V2		
Date: 2017/02/14		14		
File: 02-FPGA_bank0.SchDoc				

▲ Bank 1 DOESNT Supports differential output

VCCO\_1 = 3.3V


UIB



XC6SLX45T-3CSG324C

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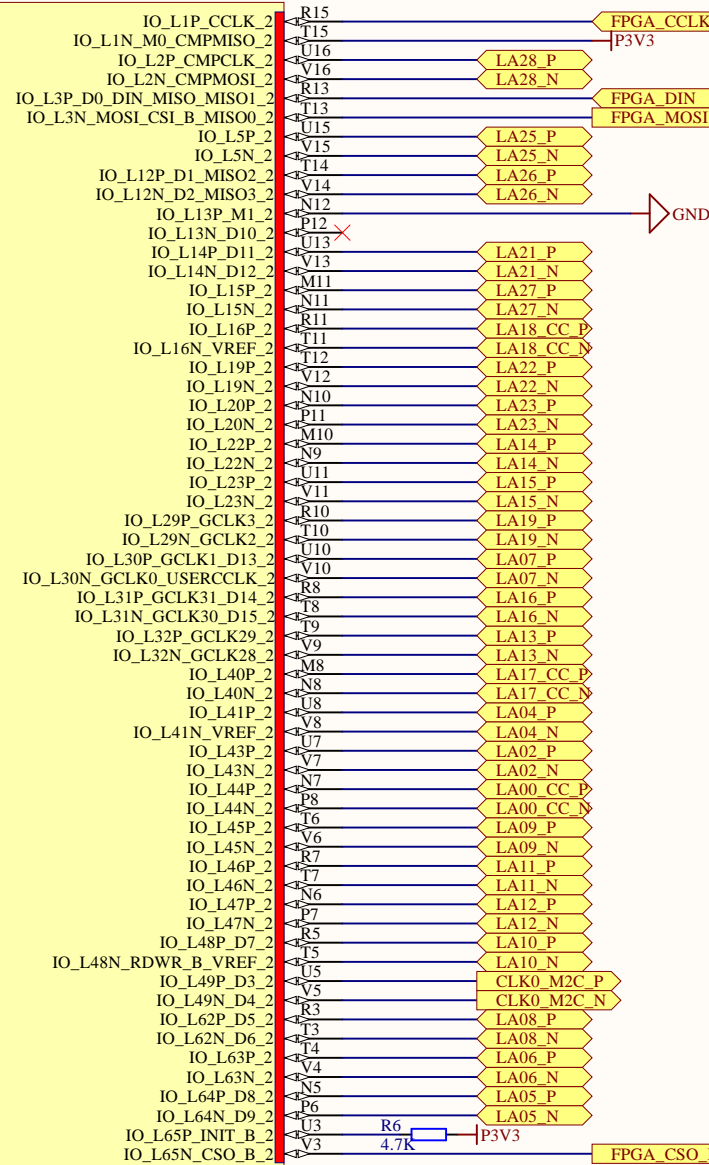
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Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:3,	Revision: V2		
Date: 2017/02/14		14		
File: 03-FPGA_bank1.SchDoc				

VCCO\_2 = 3.3V


U1C

BANK 2



FPGA configuration modes:  
1) Master SPI (default mode)  
M0=high  
M1=low  
M1 = '0'

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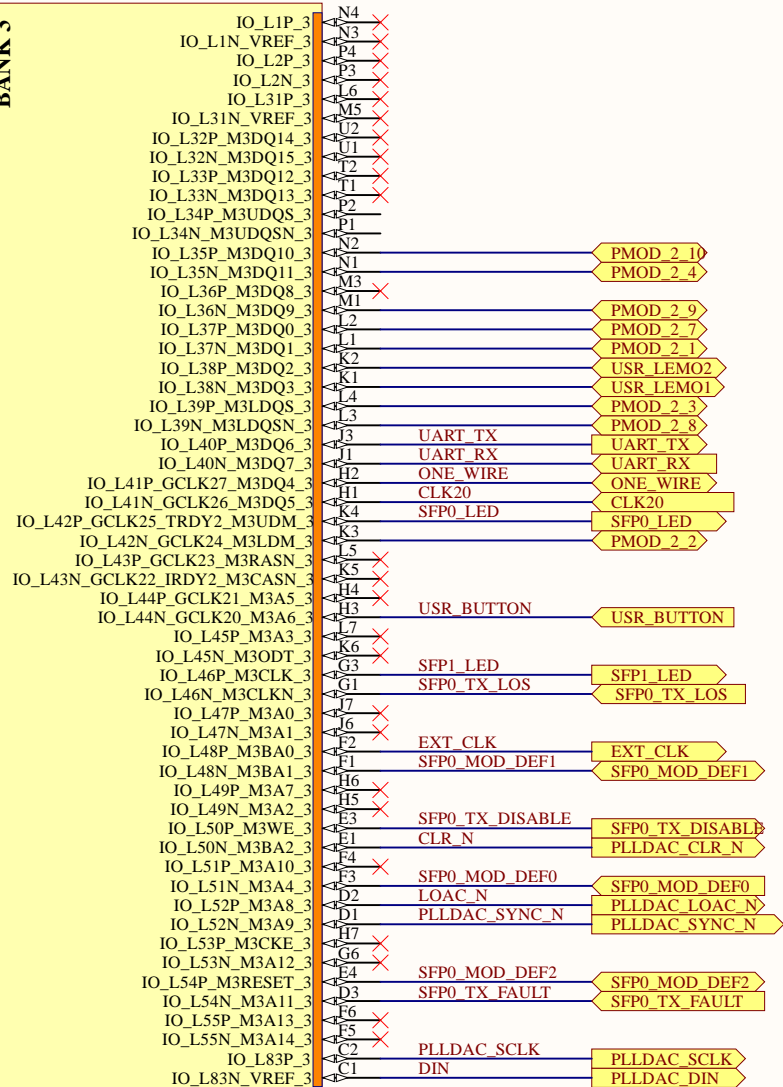
Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:4.	Revision: V2		
Date: 2017/02/14		14		
File: 04-FPGA_bank2.SchDoc				

Bank 3 DOESN'T Supports differential output

VCCO\_3 = 3.3V

UID


BANK 3

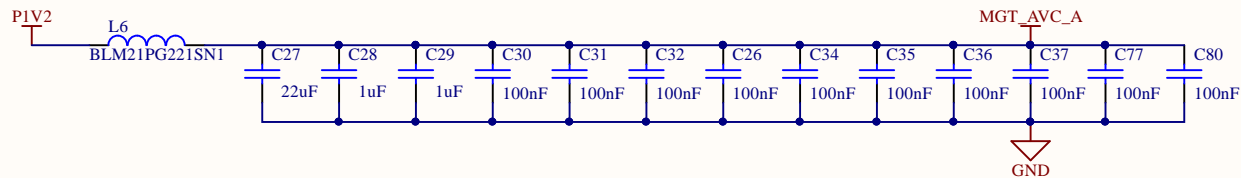
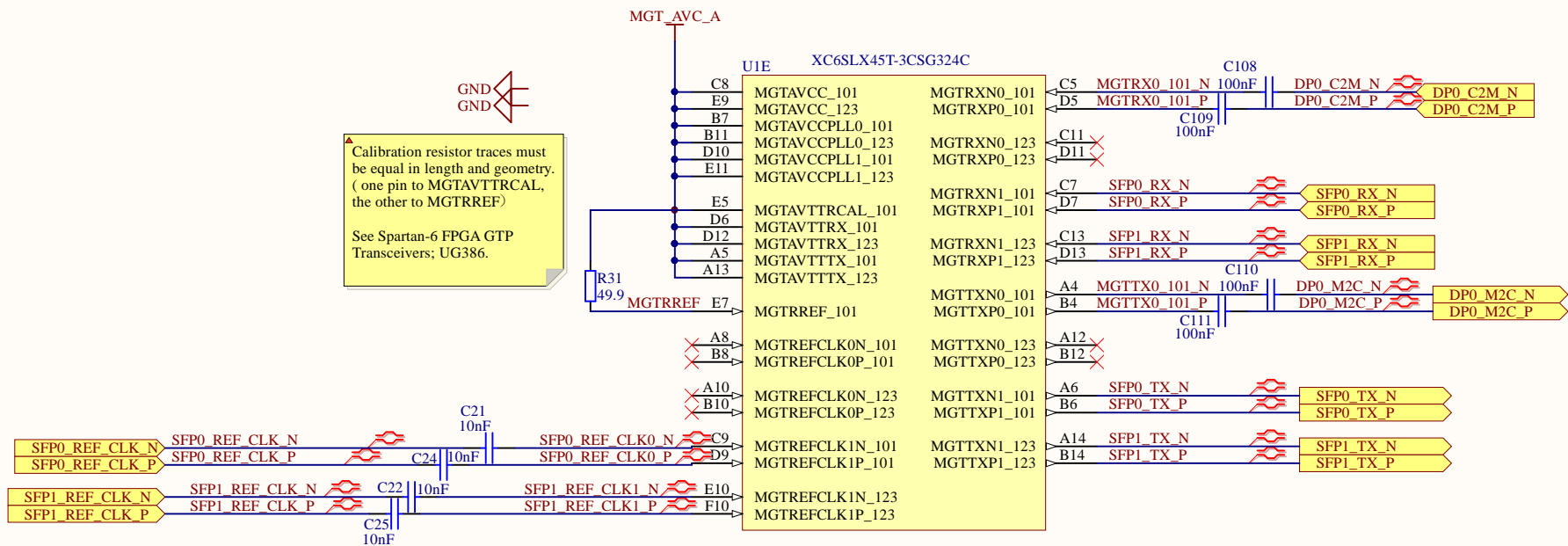



XC6SLX45T-3CSG324C

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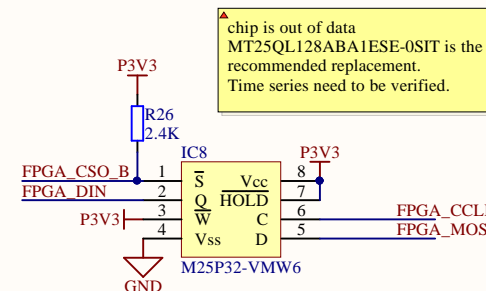
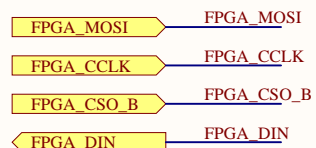
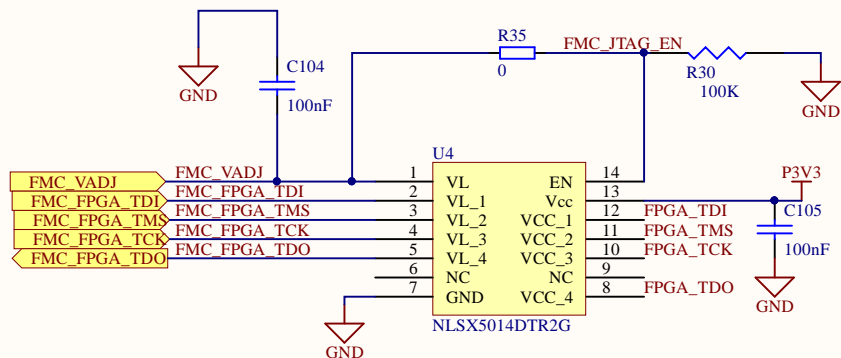
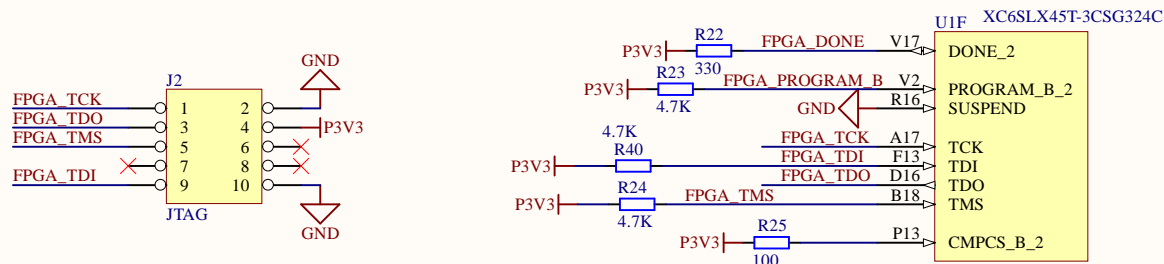
Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:5	Revision: V2		
Date: 2017/02/14		14		
File: 05-FPGA_bank3.SchDoc				



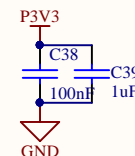
Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:6.	Revision: V2		
Date: 2017/02/14		14		
File: 06-FPGA_GTP.SchDoc				

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▲ CCLK Termination. See Spartan6 FPGA Configuration User Guide P52

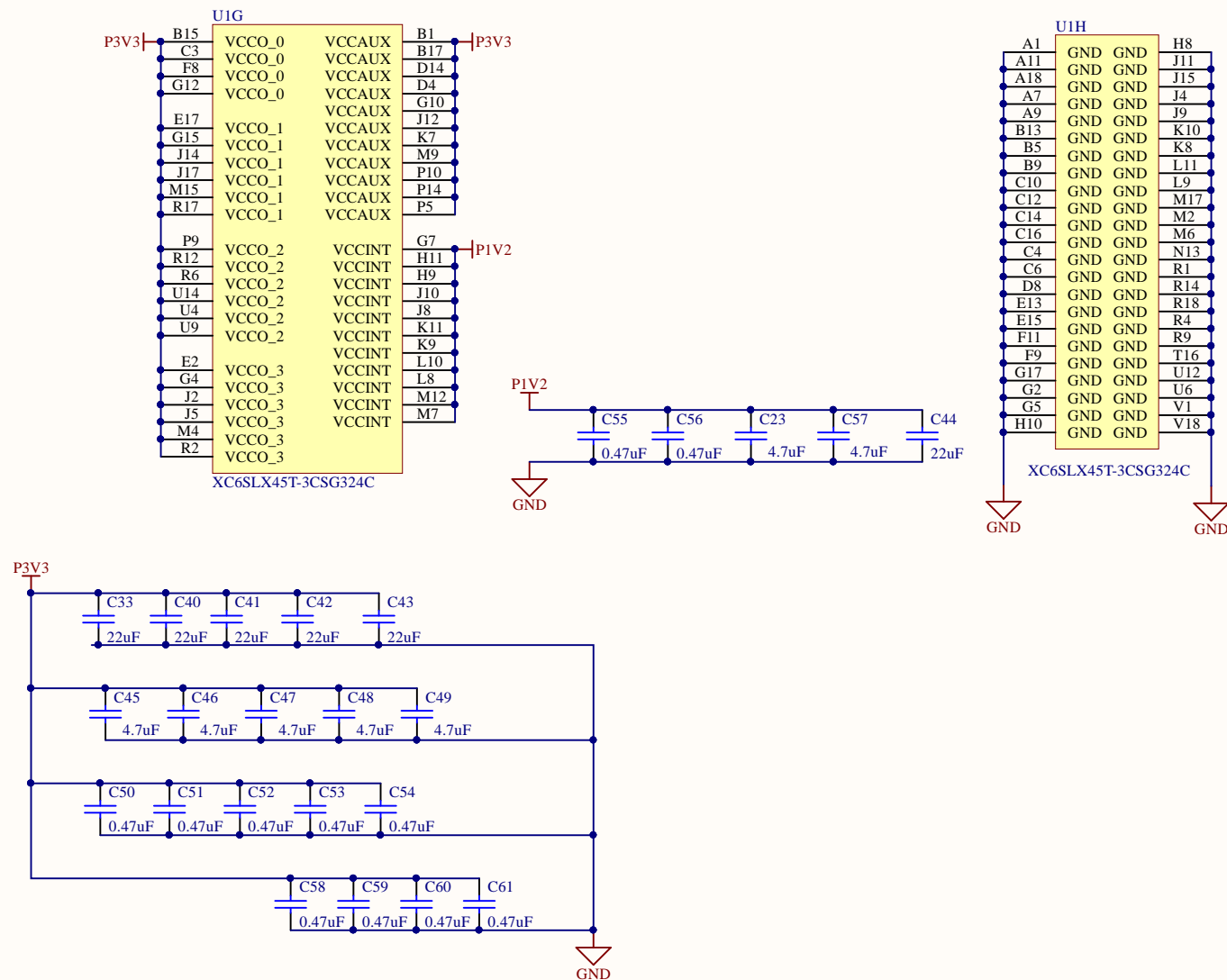


▲ When CS\_n is high, Q will stay high impedance

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Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:7.	Revision: V2		
Date: 2017/02/14		14		
File: 07-FPGA Config.SchDoc				



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Title CUTEWR-DP

Size: A4 Number: 8.

Date: 2017/02/14

File: 08-FPGA\_Power.SchDoc

TSINGHUA

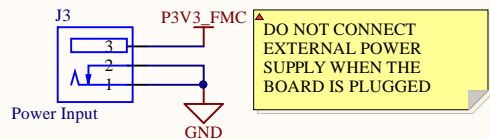
hongming

lihm09@foxmail.com

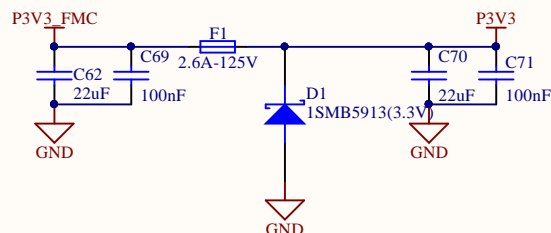
Revision: V3

14

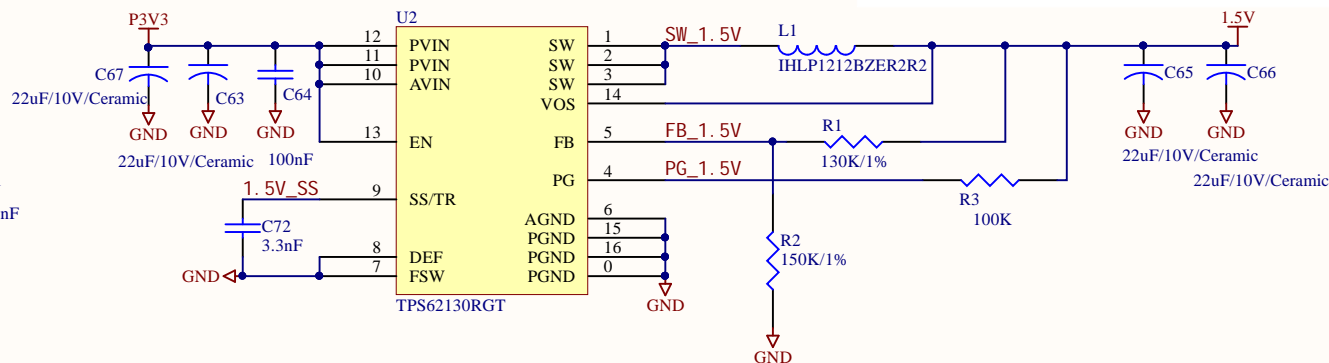
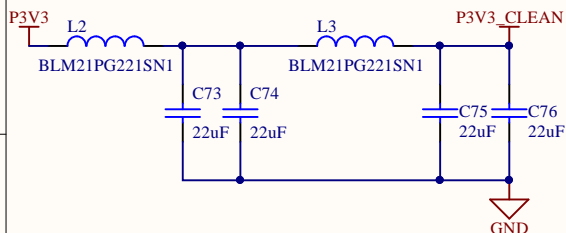




The CUTE-WR can be powered either from FMC or Power Jack

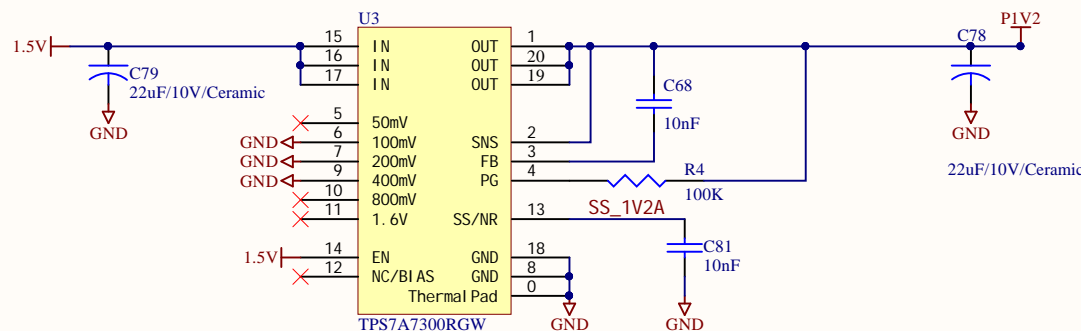


4-pole LC filter. It supplies clean 3.3V for clock distribution circuit



$$V_{out} = 0.8V \cdot (R1 + R2) / R2$$

$$1.5 = 0.8 \cdot (150K + 130K) / 150K$$



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Title CUTEWR-DP

Size: A4 Number:9.

Date: 2017/02/14

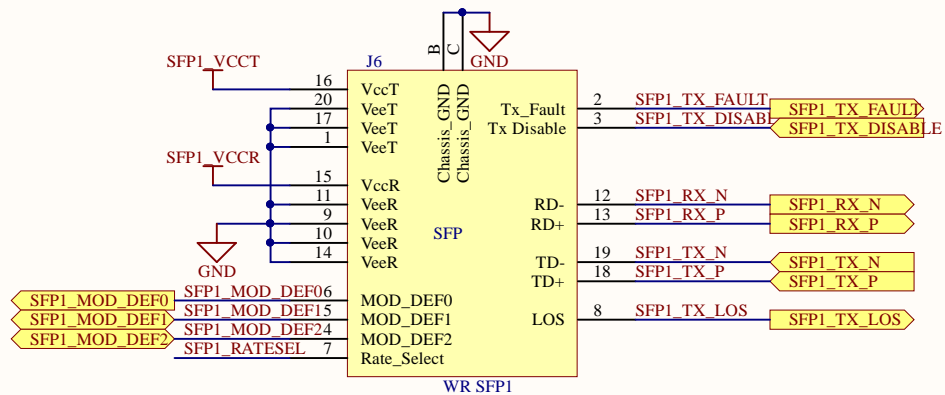
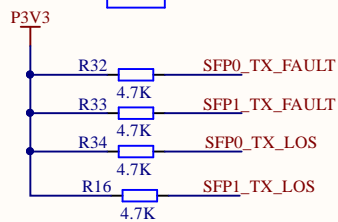
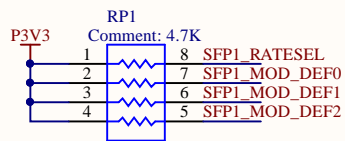
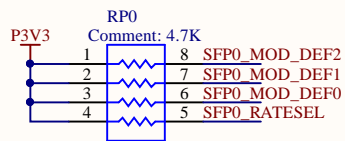
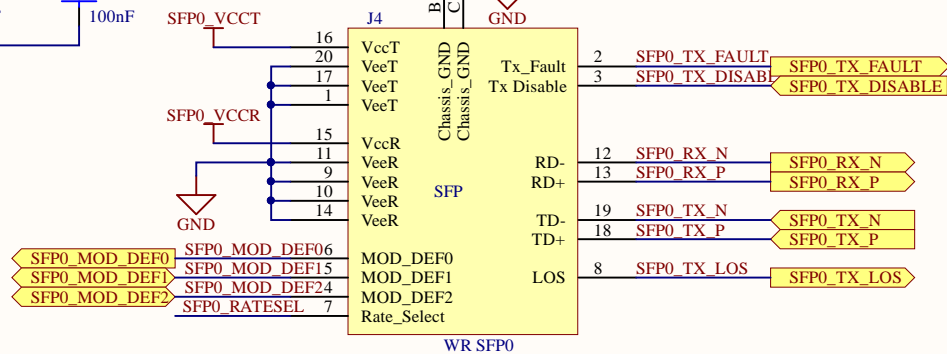
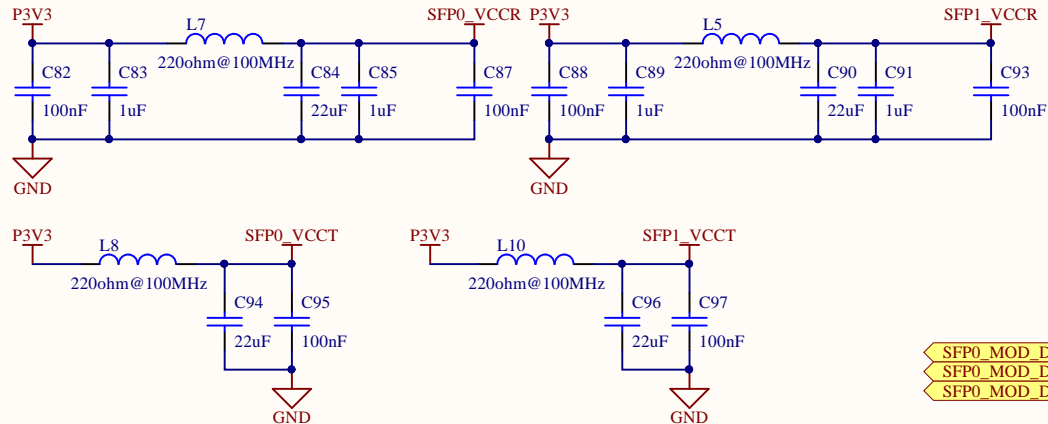
File: 09-Power.SchDoc


TSINGHUA

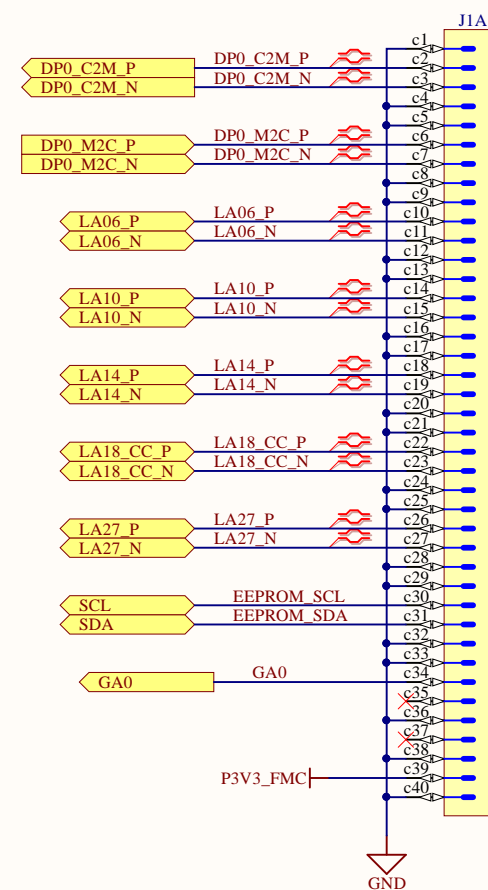
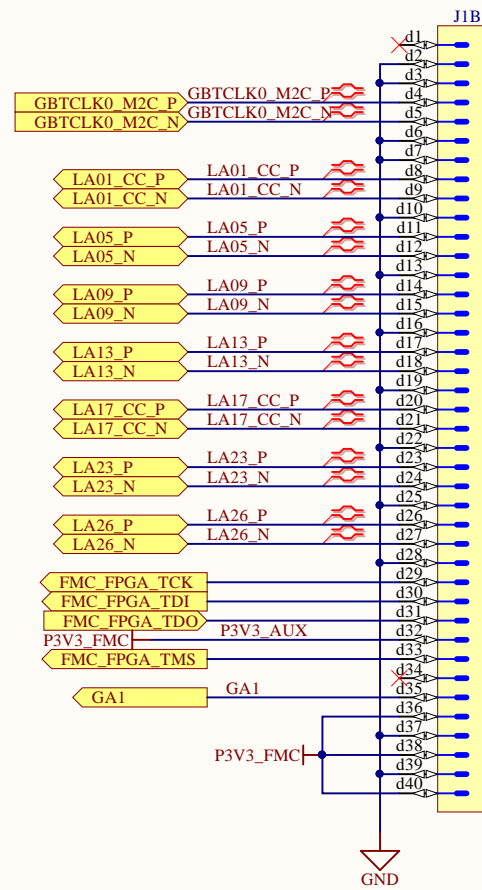
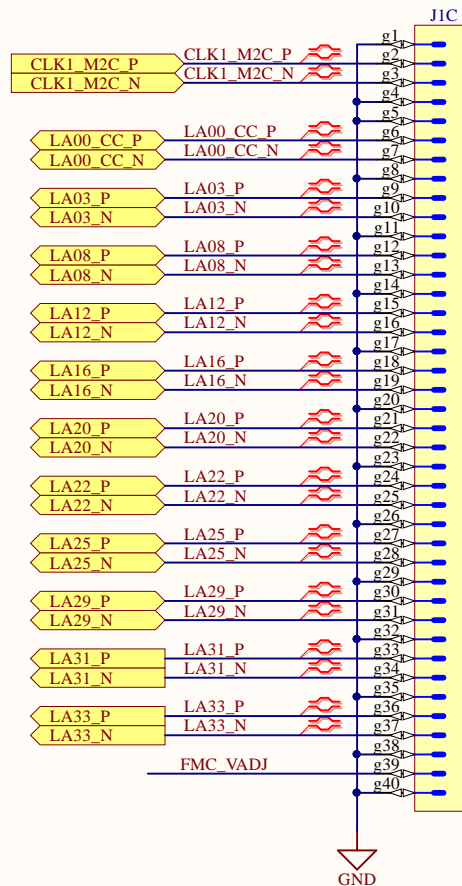
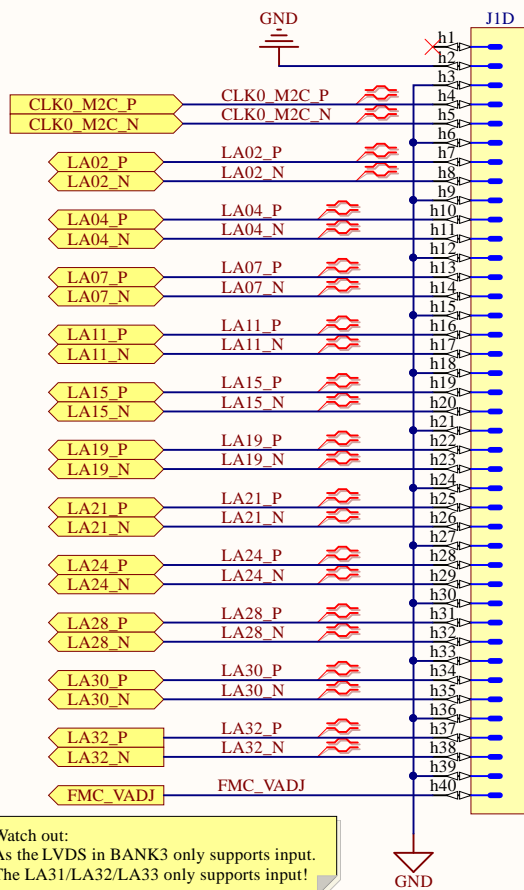
hongming

lihm09@foxmail.com



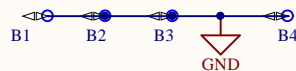


Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number: 10.	Revision: V2		
Date: 2017/02/14		14		
File: 10-SFP.SchDoc				



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NB: the LVDS pairs must have a differential impedance of 100 ohm (+/-10%) and be routed with no skew between the P and the N lines. The skew between the various LA pairs should be kept as low as possible (<200ps).

Title CUTEWR-DP

Size: A4 Number:11.

Revision: V2

Date: 2017/02/14

14

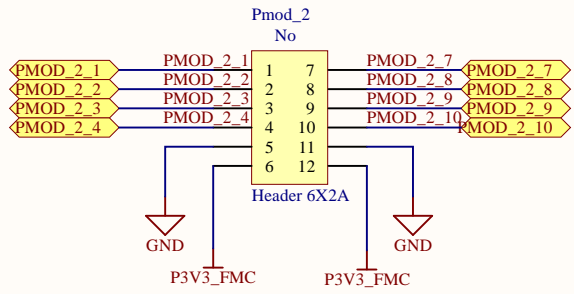
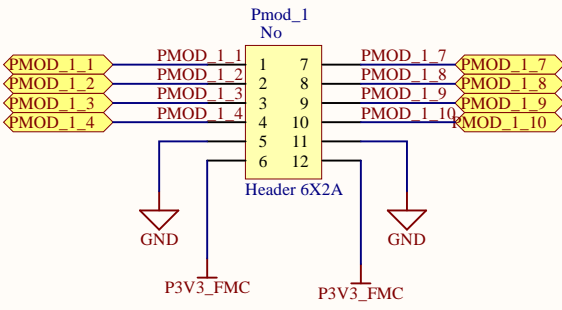
File: 11-FMC\_Connector.SchDoc

TSINGHUA

hongming


lihm09@foxmail.com

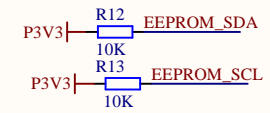
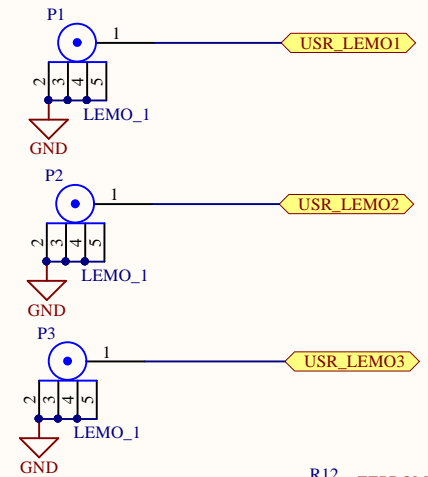
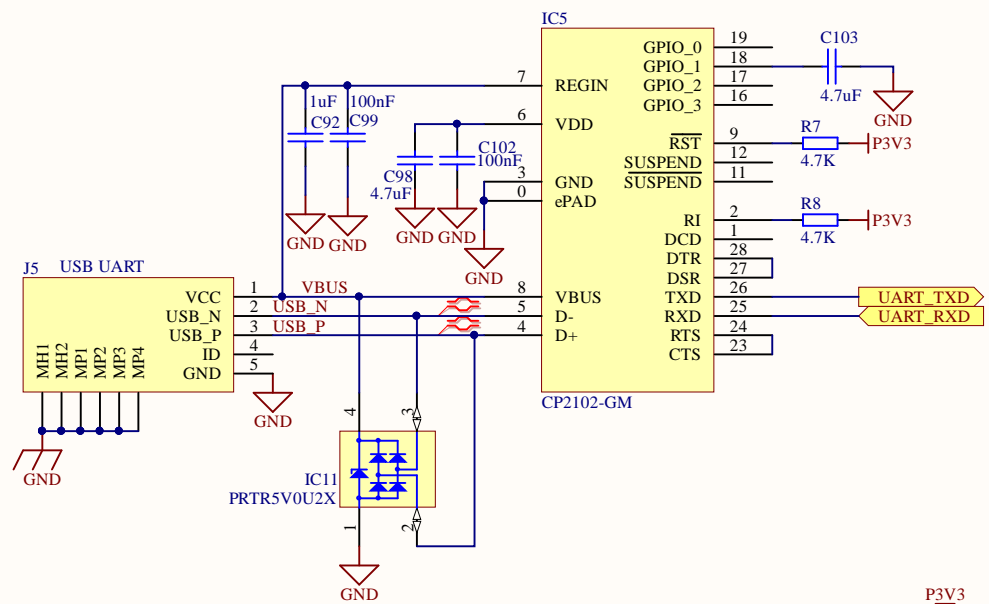




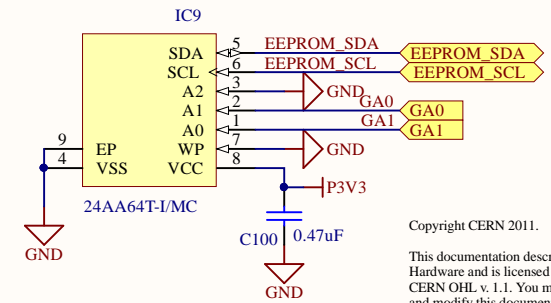
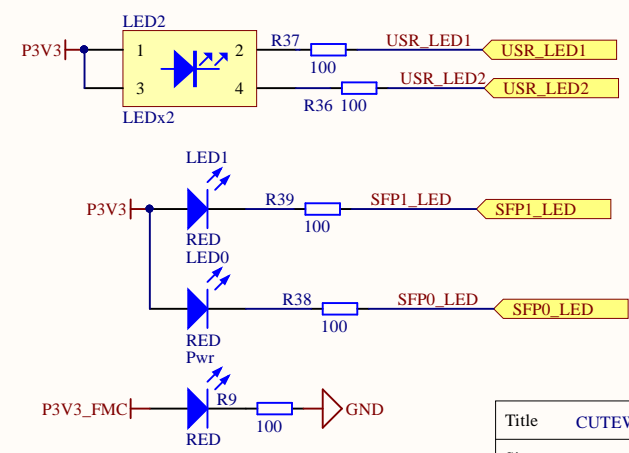
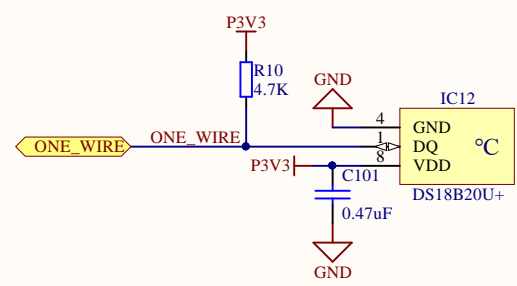
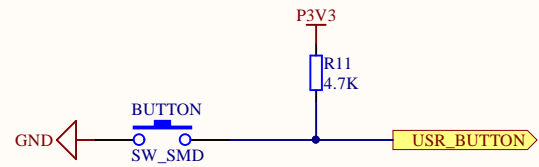
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Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:12.	Revision: V2		
Date: 2017/02/14		14		
File: 12-Pmod_Connector.SchDoc				




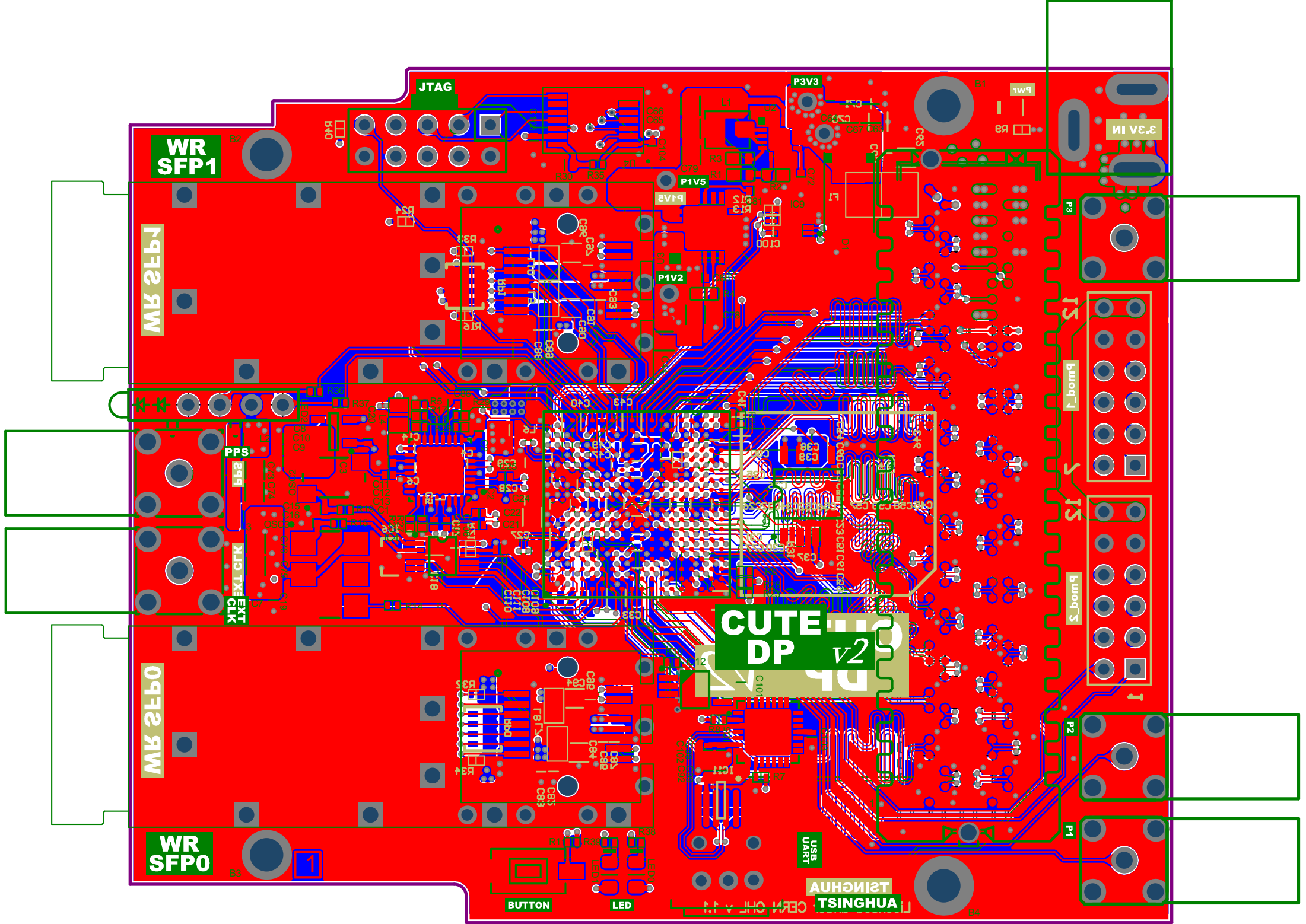
Reduce I2C w/r frequency?



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Title CUTEWR-DP			TSINGHUA hongming lihm09@foxmail.com	
Size: A4	Number:13.	Revision: V2		
Date: 2017/02/14		14		
File: 13-User Interface.SchDoc				



CUTE  
DP v2

WR SFP1

WR SFP1

WR SFP0

WR SFP0

JTAG

TSINGHUA  
UNIVERSITY

BUTTON

LED

NI V3.3

TS

TS

TS

TS

TS

TS