

DI/OT CPCI–serial 9 Slot backplane
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P12V

GND

P12V

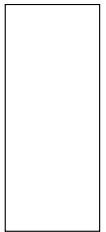
GND

P5V

P5V

GND

EXT Power

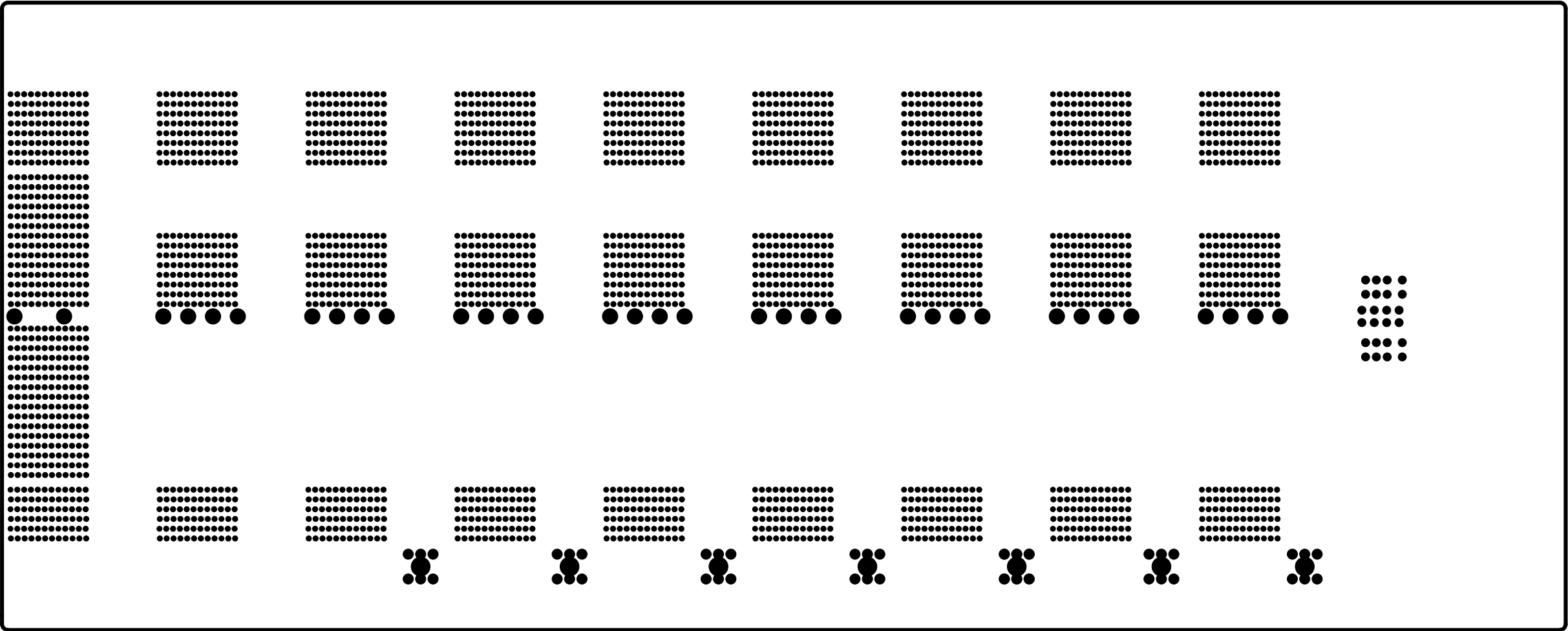


EDA–04211–V1


Top Layer

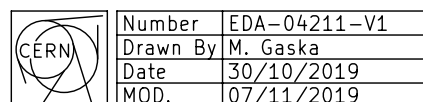
Top Overlay

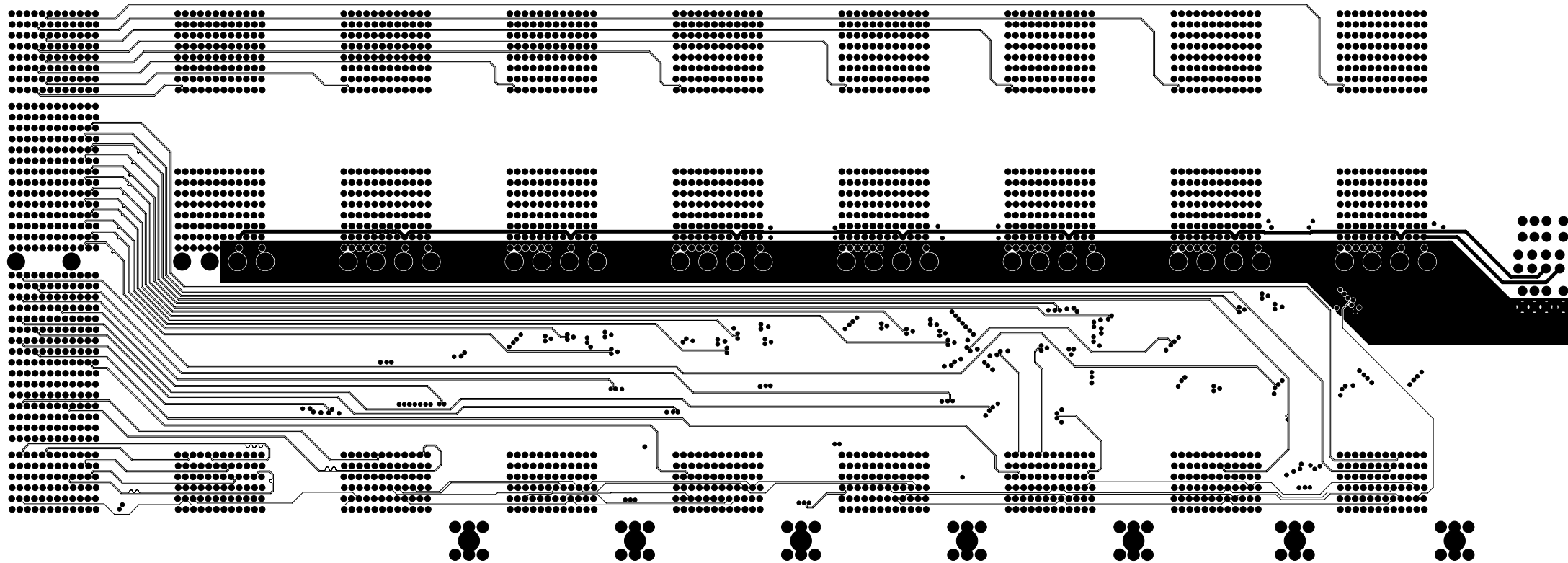
	Number	EDA–04211–V1
	Drawn By	M. Gaska
	Date	30/10/2019
	MOD.	07/11/2019




Top Solder

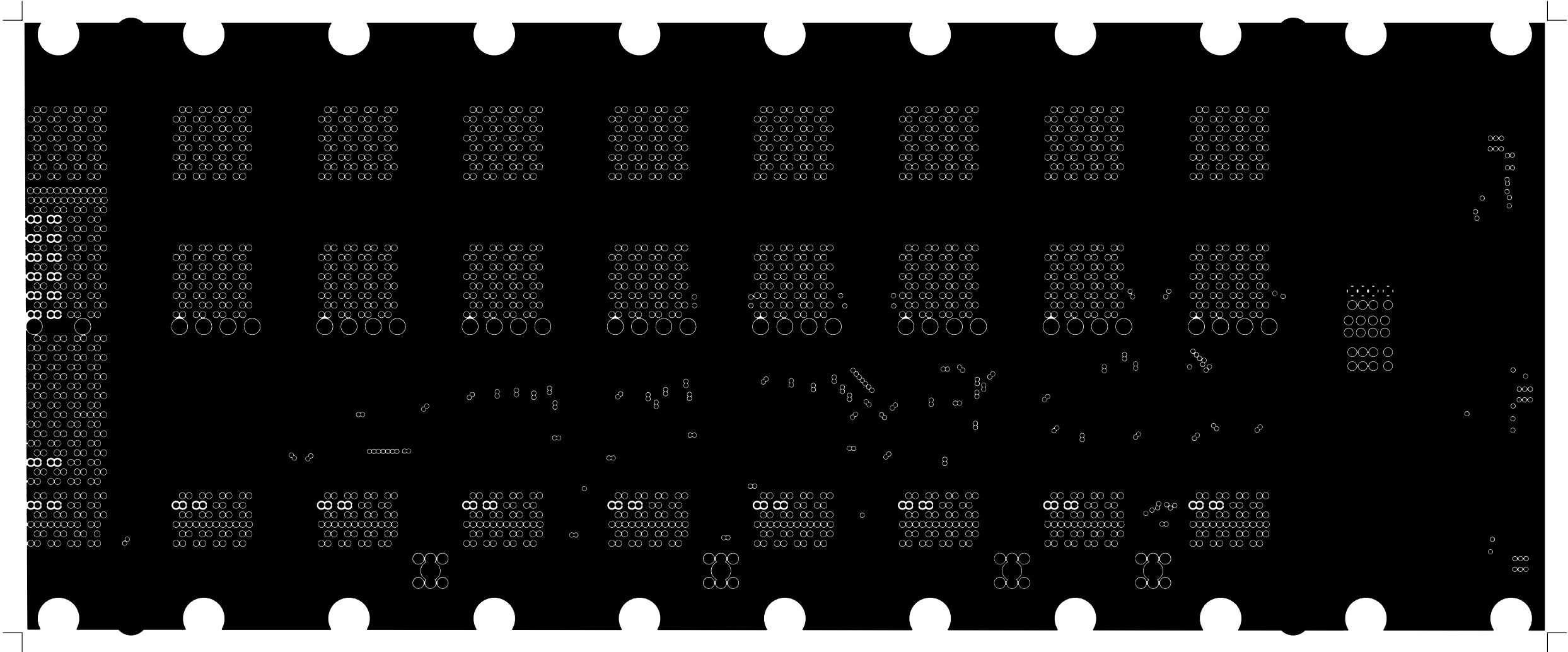
	Number	EDA-04211-V1
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[illegible]



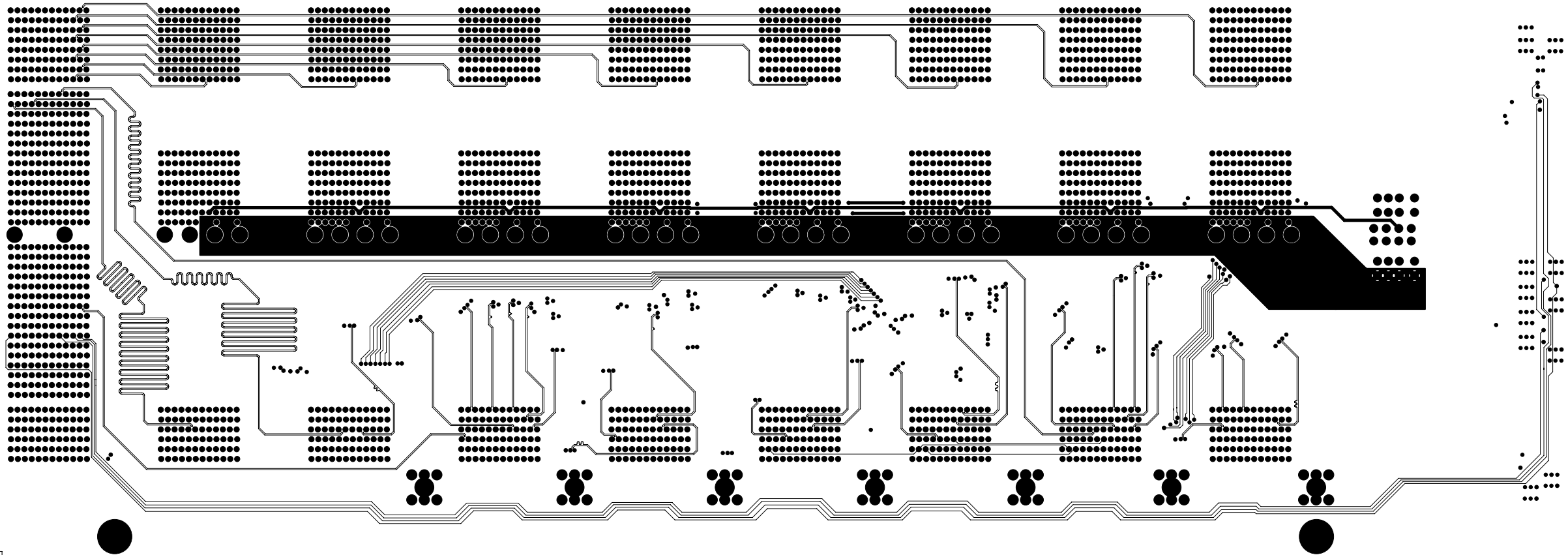
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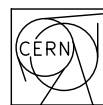
5192									
		4							



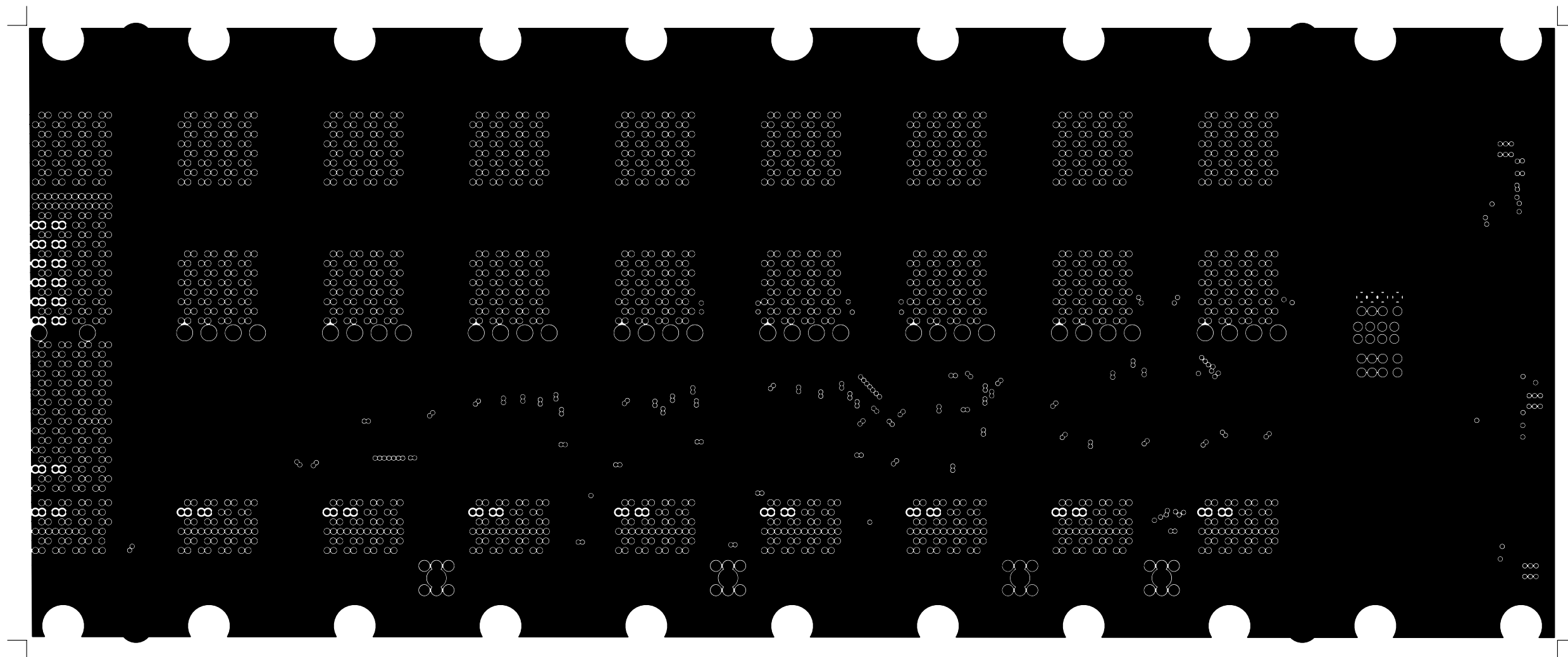
Number	EDA-04211-V1
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GND											
				5							



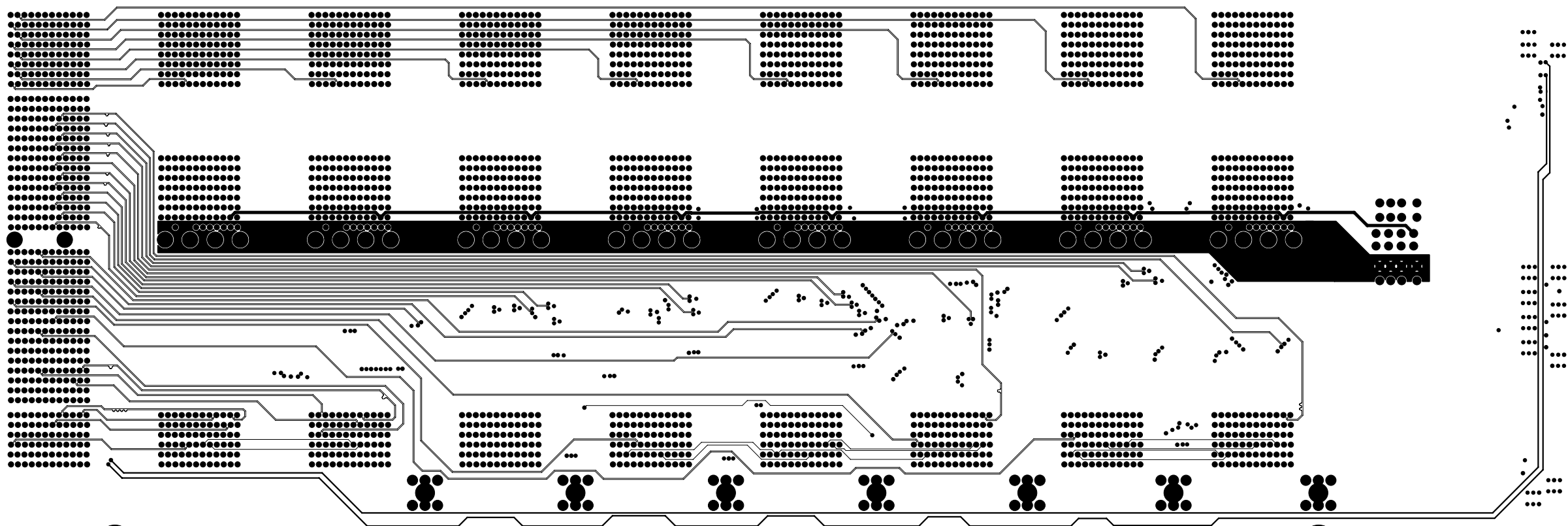
	Number	EDA-04211-V1
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5193											
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	Number	EDA-04211-V1
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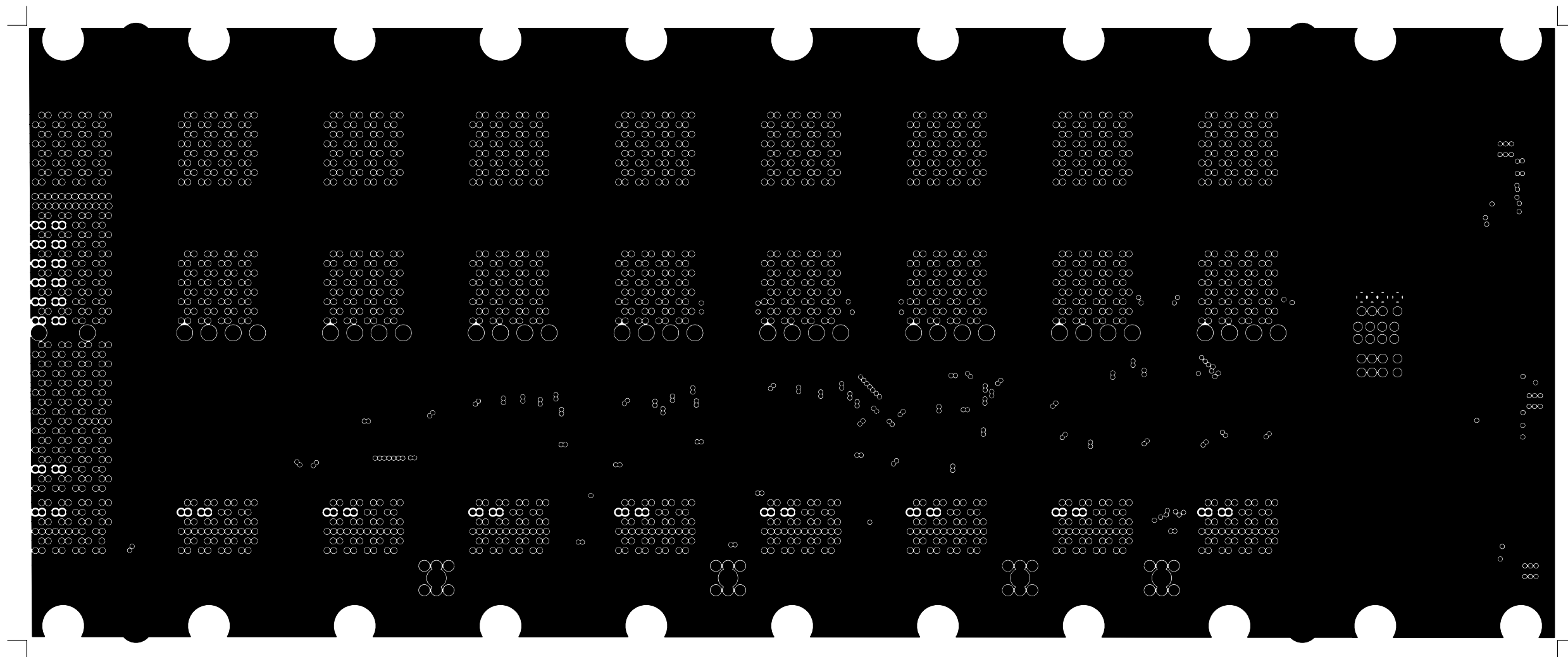
GND											
						7					




	Number	EDA-04211-V1
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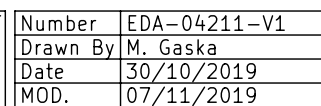
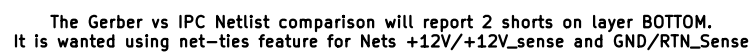
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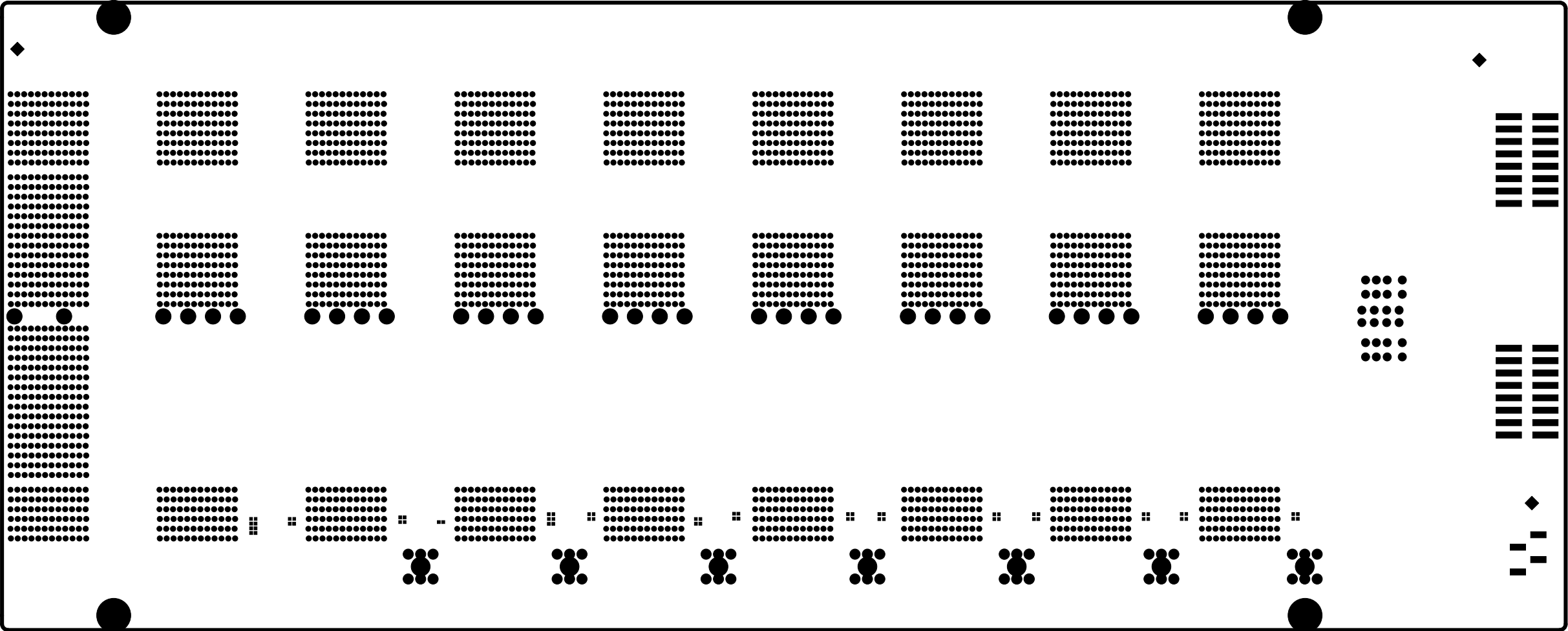
	Number	EDA-04211-V1
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										GND	
								9			

[illegible]



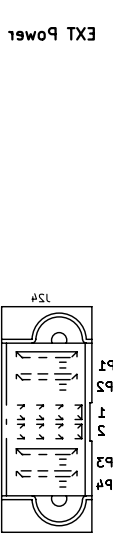
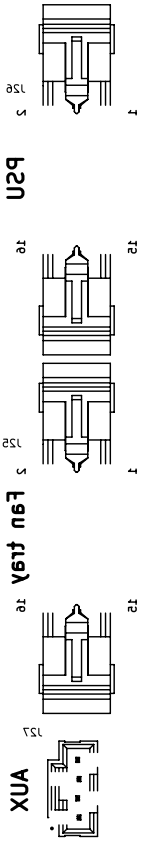
Bottom Layer



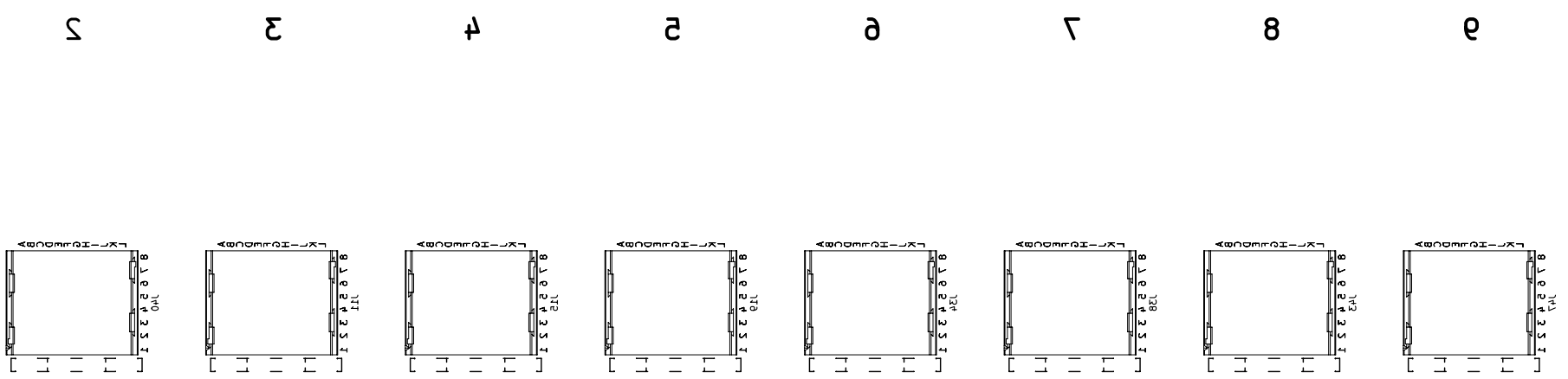
Bottom 2019s



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EDA-04211-V1



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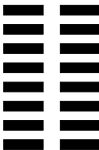
8

9

GND b2v b2v b2v GND b2v b2v GND b2v

Bottom Overlay

	Number	EDA-04211-V1
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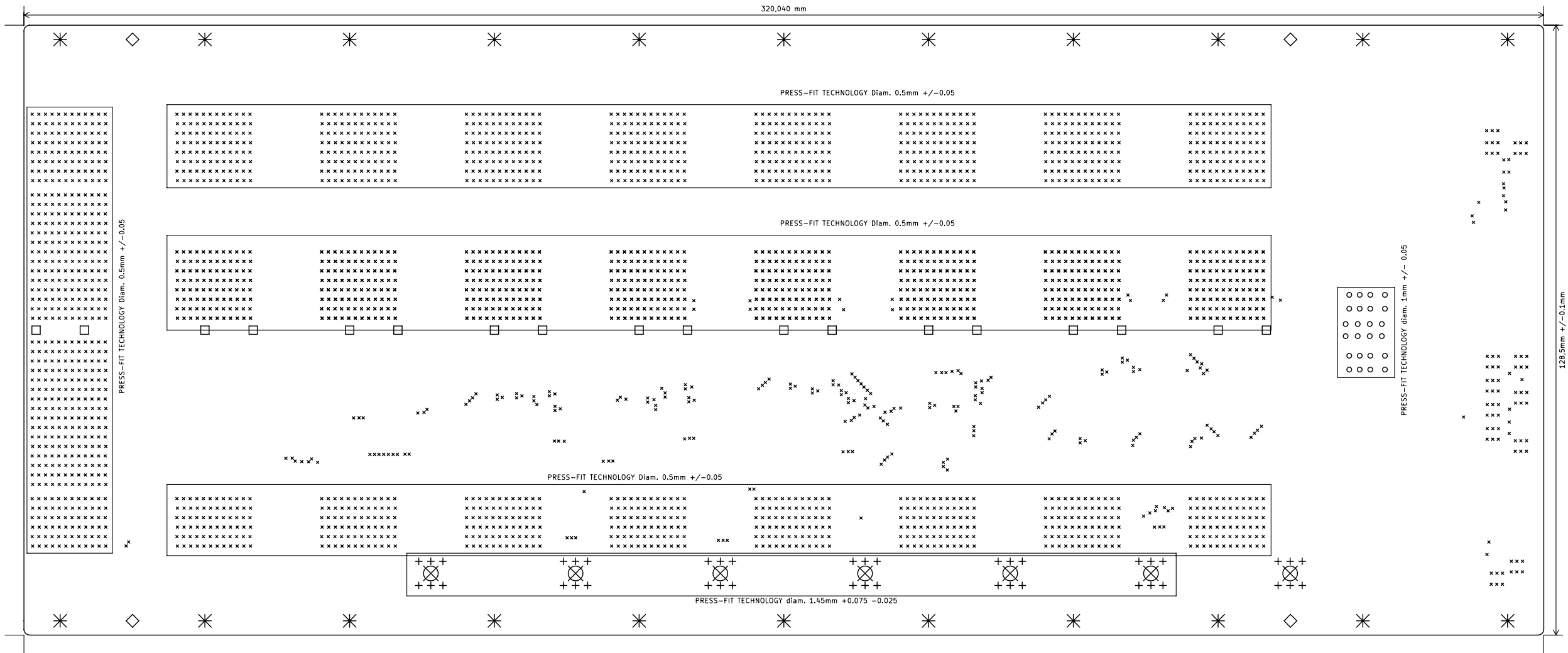


Bottom Paste



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LAYER IDENTIFICATION		LINE (mils)		FINISHED COPPER THICKNESS	CONTROLLED IMPEDANCE +/- 10%		DIELECTRIC THICKNESS *= CRITICAL	Er
		WIDTH	WIDTH/GAP		Single	Differential		
TOP LAYER	GND PLANE	-	-	35 um	-	-	0.180mm	4,3
LAYER 2	SIGNAL LAYER	-	4 / 5	18 um	-	100 Ohms	0.200mm	4,3
LAYER 3	GND PLANE	-	-	18 um	-	-	0.180mm	4,3
LAYER 4	SIGNAL LAYER	-	4 / 5	18 um	-	100 Ohms	0.200mm	4,3
LAYER 5	GND PLANE	-	-	18 um	-	-	0.180mm	4,3
LAYER 6	SIGNAL LAYER	-	4.7 / 5.9	18 um	-	100 Ohms	1.900mm	4,3
LAYER 7	GND PLANE	-	-	18 um	-	-	0.180mm	4,3
LAYER 8	SIGNAL LAYER	-	4 / 5	18 um	-	100 Ohms	0.200mm	4,3
LAYER 9	GND PLANE	-	-	18 um	-	-	0.180mm	4,3
LAYER 10	SIGNAL LAYER	-	4 / 5	18 um	-	100 Ohms	0.200mm	4,3
LAYER 11	GND PLANE	-	-	18 um	-	-	0.180mm	4,3
BOTTOM LAYER	SIGNAL LAYER	-	5.9 / 4	35 um	-	*100 Ohms	* 0.180mm	4,3
FINISHED BOARD THICKNESS +/- 10%							4.03mm	



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Drill Map:

- * 0.50mm / 0.020" (3720 holes)
- o 1.00mm / 0.039" (24 holes)
- + 1.45mm / 0.057" (42 holes)
- 2.50mm / 0.098" (18 holes)
- ◇ 2.70mm / 0.106" (4 holes)
- ⊗ 3.10mm / 0.122" (7 holes)
- * 2.70mm / 0.106" (22 holes) (not plated)