

1 2 3 4 5 6 7 8

A

A

B

B

C

C

D

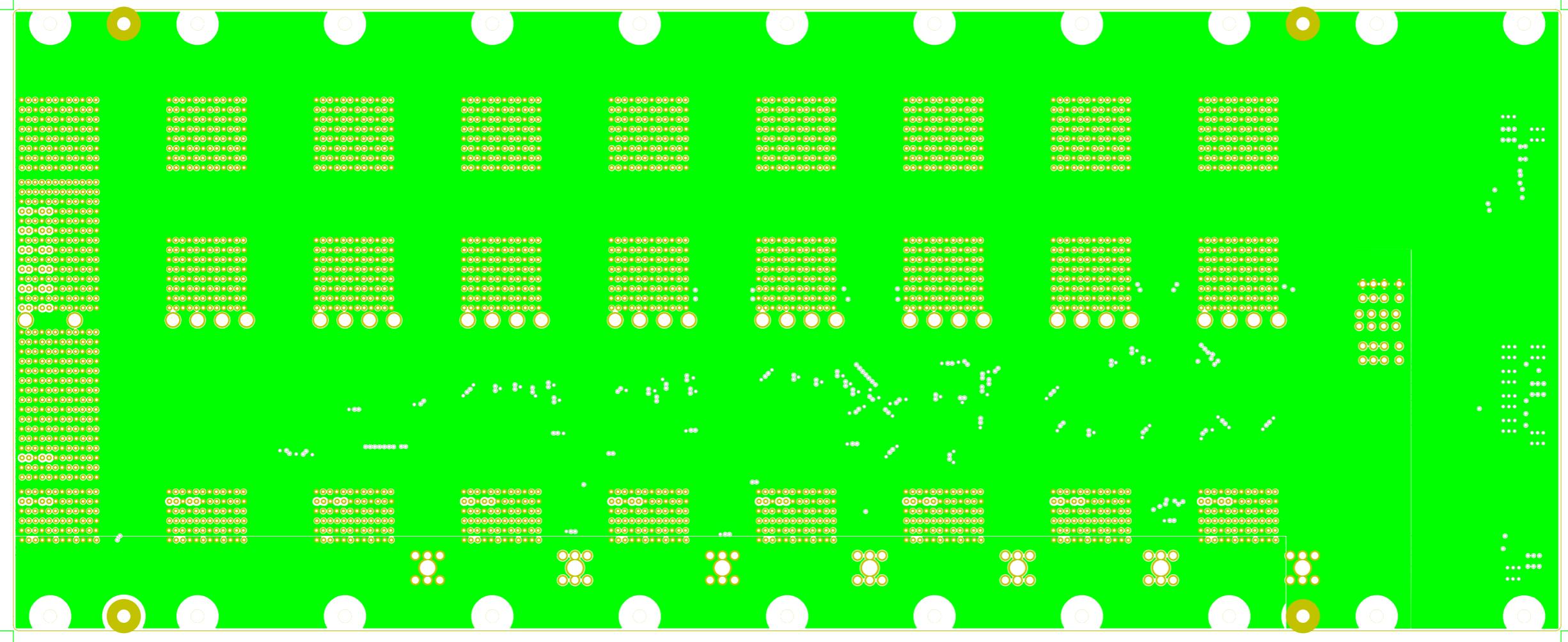
D

E

E

F

F



Number	EDA-04211-V1
Drawn By	M. Gaska
Date	30/10/2019
MOD.	07/11/2019

Top Layer
1

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Project/Equipment: DI/OT

KiCad E.D.A. kicad (5.1.5)-3

Document

DI/OT CPCI-serial 9 Slot Backplane

Designer

Michał Gaska

Drawn by

Checked by

Last Mod.

2020-04-26

File:

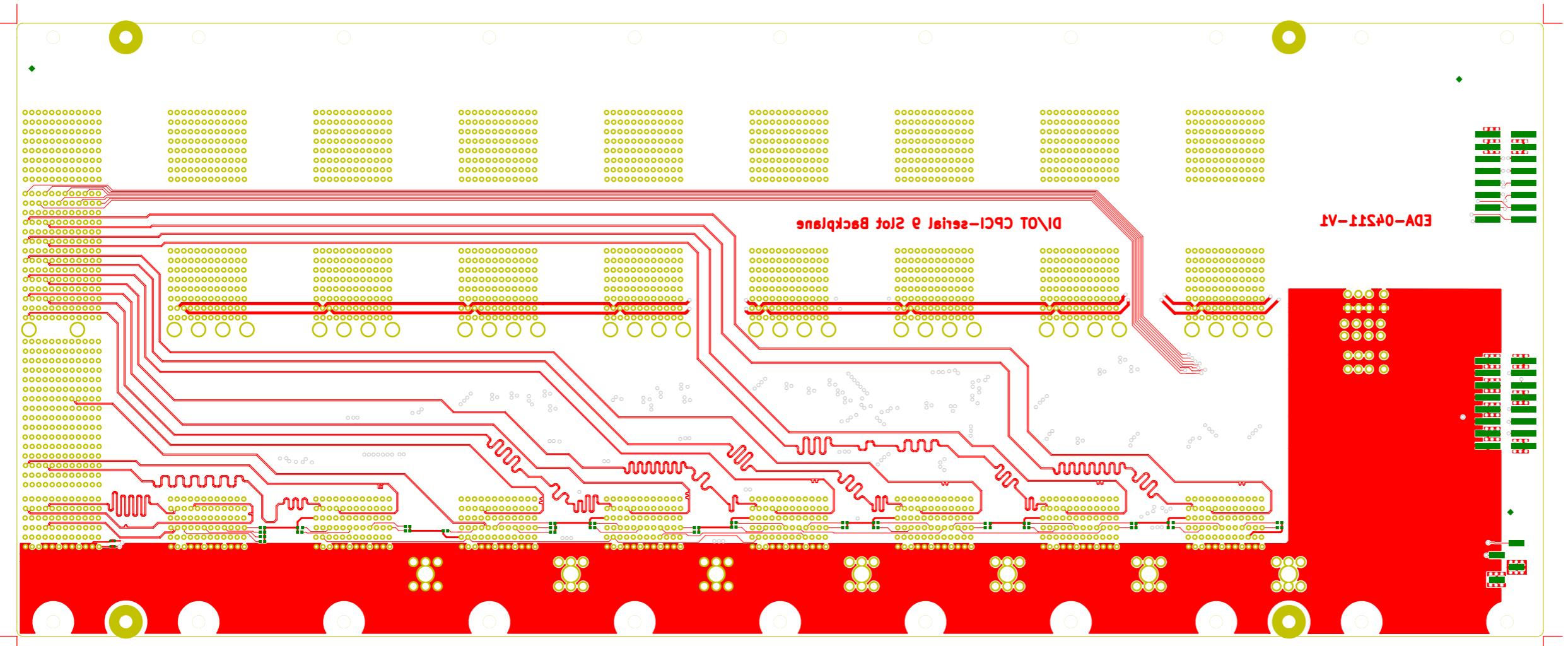
EDA-04211-V1-0.kicad_pcb

Sheet: 1 of 1



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The Gerber vs IPC Netlist comparison will report 2 shorts on layer BOTTOM.
It is wanted using net-ties feature for Nets +12V/+12V_sense and GND/RTN_Sense



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Bottom Layer

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DI/OT CPCi-serial 9 Slot Backplane

Designer Michal Gaska

BE-CO

Drawn by

CERN

Checked by

2020-04-26

Last Mod.

File: EDA-04211-V1-0.kicad_pcb

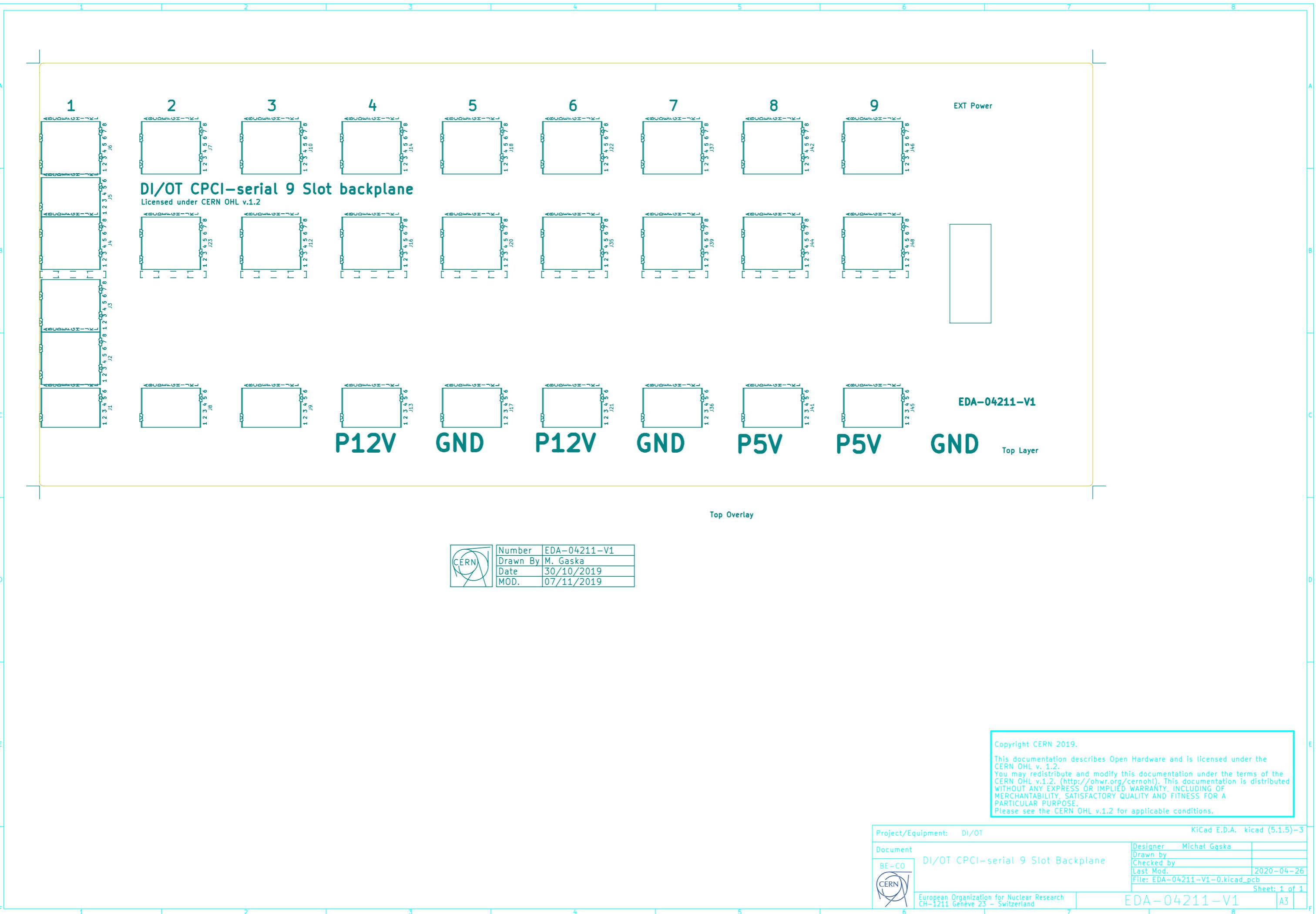
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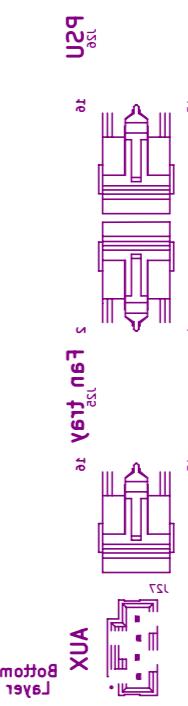
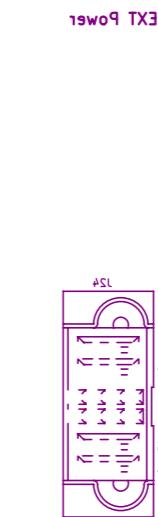
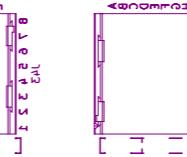
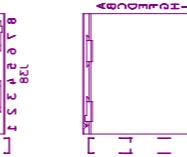
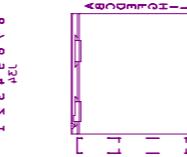
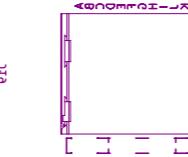
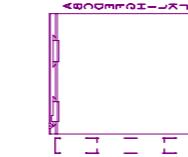
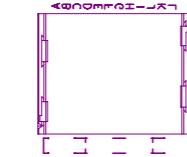
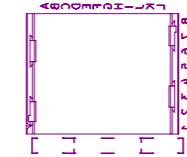
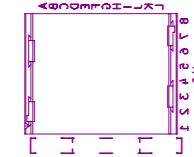
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A3

1 2 3 4 5 6 7 8 F





GND P5A P5A P5A P5A P5A P5A P5A

Bottom Overlay



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Project/Equipment: DI/OT

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DI/OT CPCI-serial 9 Slot Backplane

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