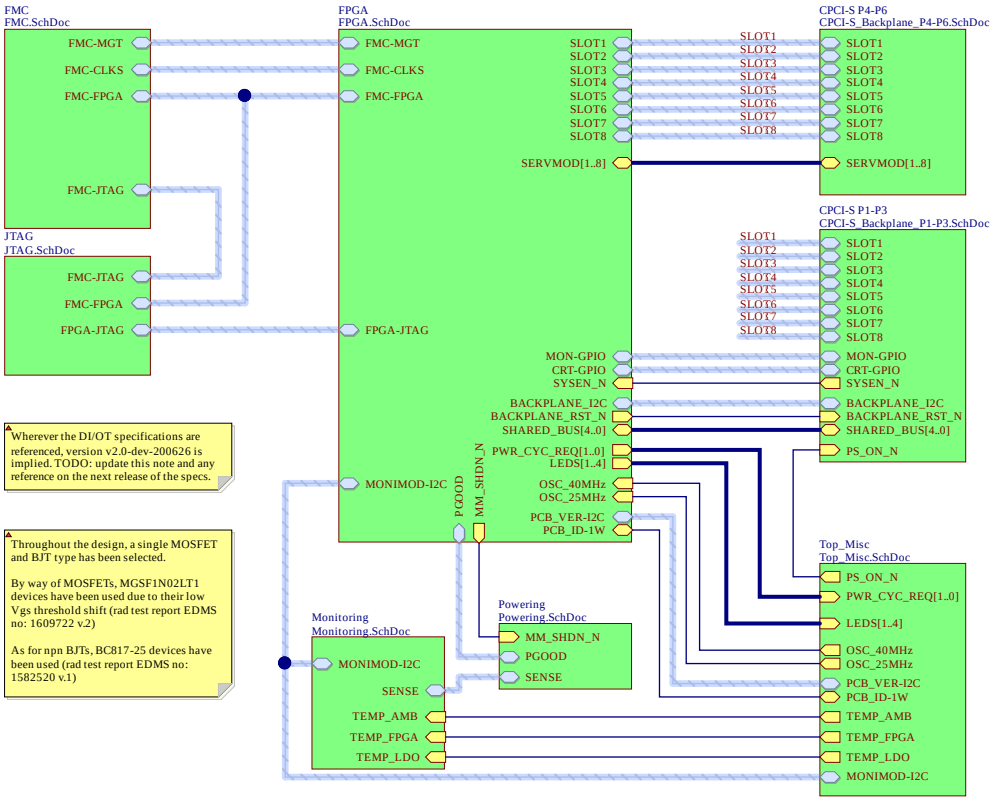
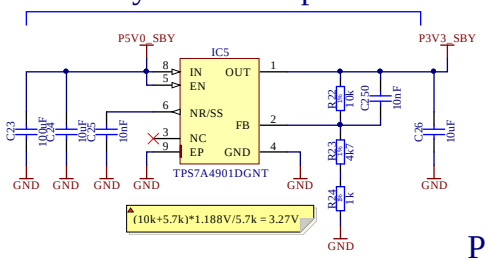


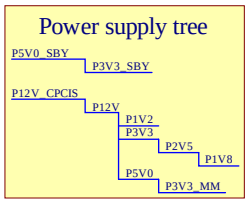
Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Top Level**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	11/11/2020
		File DIOT-sb-igl_top.SchDoc	
		Print Date 16/11/2020 16:33:28	Sheet 1 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev *

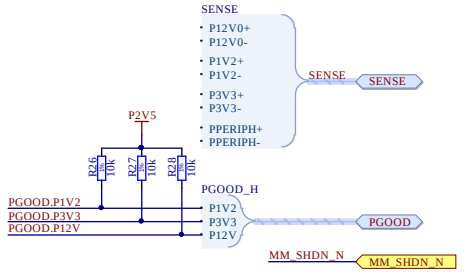
Always-on P3V3 power



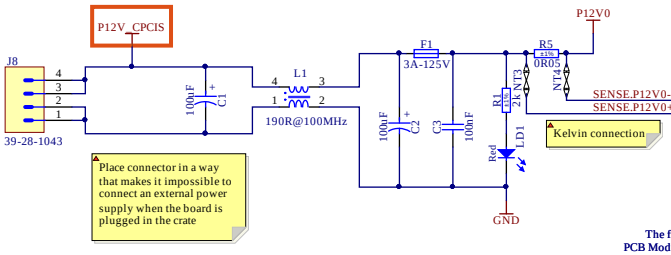
P12V is only enabled after P3V3_SBY is up because of PS_ON_N (see Top_Misc)

Power supply tree

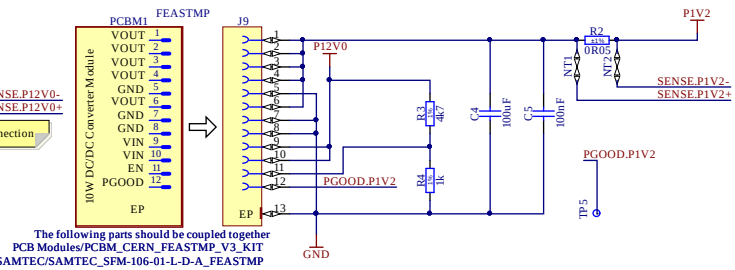




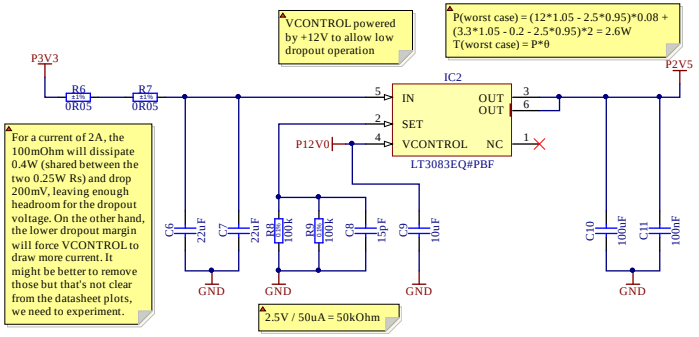
12V0 power cleanup



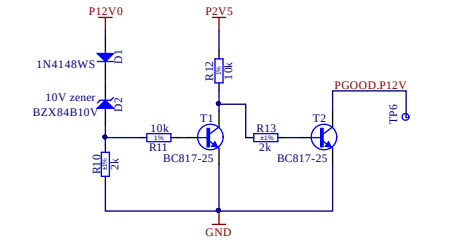
P1V2 power



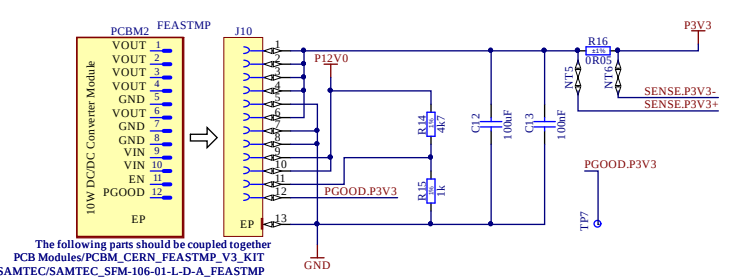
P2V5 power



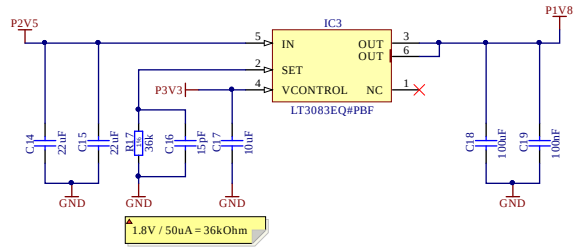
12V brownout detection



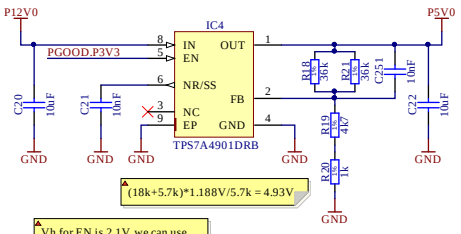
P3V3 power



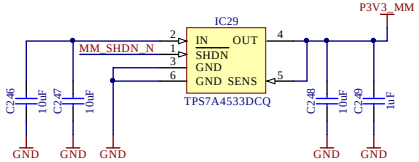
P1V8 power



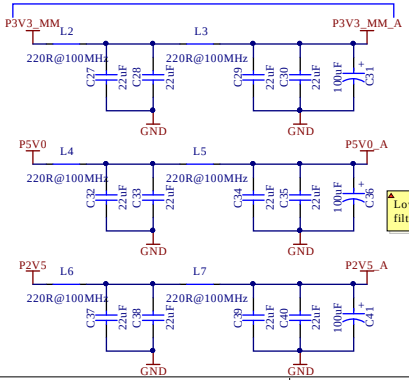
P5V0 power



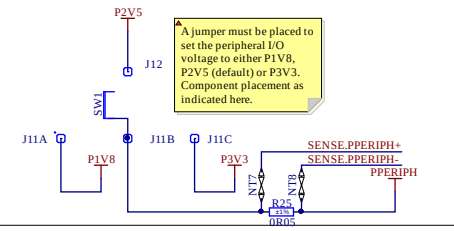
MoniMod P3V3 power



Analog power filtering

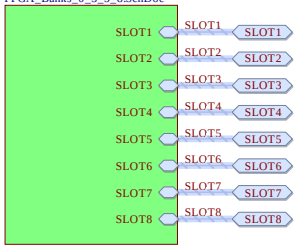


Peripheral voltage selection

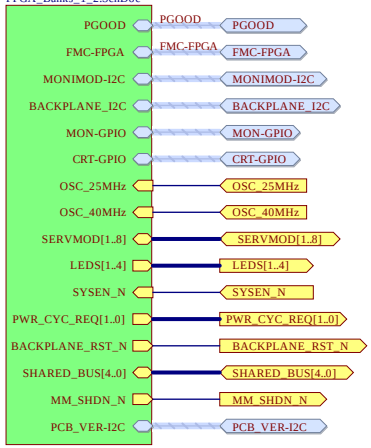


Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Power	Designer	C. Gentsos
		Drawn by	C. Gentsos 28/08/2020
		Check by	* -
		Last Mod.	C. Gentsos 16/11/2020
		File	Powering.SchDoc
		Print Date	16/11/2020 16:33:29 Sheet 2 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev *

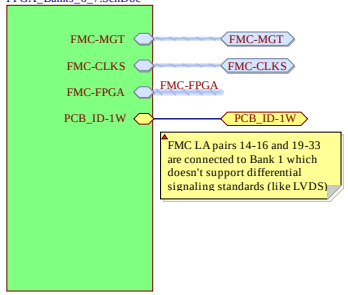
FPGA Banks 0,3,5,8
FPGA_Banks_0_3_5_8.SchDoc



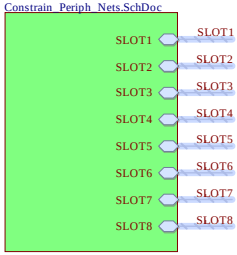
FPGA Banks 1,2
FPGA_Banks_1_2.SchDoc



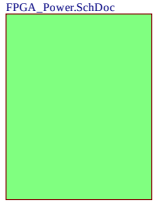
FPGA Banks 6,7
FPGA_Banks_6_7.SchDoc



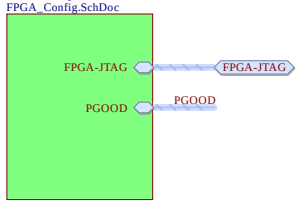
Constrain Peripheral Board Nets
Constrain_Periph_Nets.SchDoc



FPGA Power
FPGA_Power.SchDoc



FPGA Config
FPGA_Config.SchDoc



Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board FPGA Top**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	16/11/2020
		File FPGA.SchDoc	
		Print Date 16/11/2020 16:33:29	Sheet 3 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

IC1M
M2GL090T-FGG676I

IC1L
M2GL090T-FGG676I

IC1K
M2GL090T-FGG676I

PLL power, 2.5V or 3.3V? 2.5V will be smoother due to the LDO so better jitter but is any of the two better for radiation?

VPPNVM must be shorted to VPP

PLL RC filters

Place the 0402 100nF caps close to the FPGA pins

25 VDD pins: 13x 10n, 12x 100n, 1x 100u, 3x 220u, 1x 330u

Some recent advice (URL below) indicates that if one MLCC is used per pin it's best to use the highest value of a given package size (here 0402). Microsemi still recommends using two different values (100n and 10n). Also, looking at the impedance-freq curves from a few same-package capacitors of different values, doesn't fully support that the inductance is the same for a given package. Still, we might want to consider this advice when we run an SIwave PI simulation after we have some layout.

7 VPP pins: 4x 10n, 3x 100n, 1x 10u

3 VREF1 pins: 2x 10n, 1x 100n, 1x 10u

1 VPPNVM pin: 1x 10n, 1x 10u

1 VDDI6 pin: 1x 100n, 1x 10u

12 VDDI1 pins: 6x 10n, 6x 100n, 1x 10u

1 VDDI4 pin: 1x 100n, 1x 10u

13 VDDI3 pins: 6x 10n, 7x 100n, 1x 10u

4 VDDI0 pins: 2x 10n, 2x 100n, 1x 10u

10 VDDI5 pins: 5x 10n, 5x 100n, 1x 10u

3 VDDI2 pins: 1x 10n, 2x 100n, 1x 10u

10 VDDI8 pins: 5x 10n, 5x 100n, 1x 10u

4 VDDI7 pins: 2x 10n, 2x 100n, 1x 10u

Project/Equipment	DI/OT
Document	DI/OT Rad-tol System Board FPGA Power
Designer	C. Gentsos
Drawn by	C. Gentsos 28/08/2020
Check by	* -
Last Mod.	C. Gentsos 16/11/2020
File	FPGA_Power.SchDoc
Print Date	16/11/2020 16:33:29 Sheet 4 of 17
Size	A3
Rev	*
	EDA-XXXXX-VX-X

BE/CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

Parts powered by 2.5V

JTAG
- TCK
- TDI
- TDO
- TMS
- TRST_N

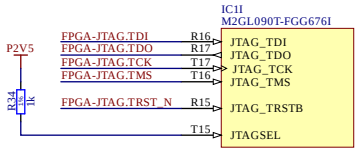
Matched Net Lengths [Tolerance = 10mm]
ClassName: FPGA-JTAG
Parameter Set

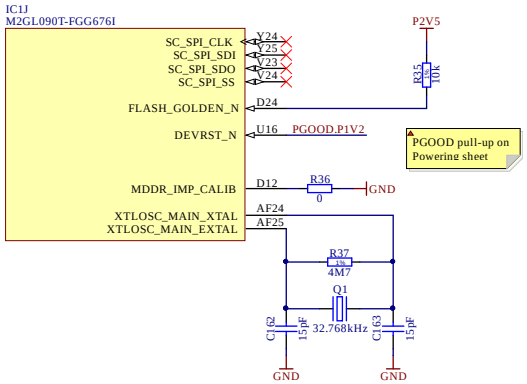
FPGA-JTAG

PGOOD_H
- P1V2
- P3V3
- P12V

PGOOD

The JTAG and configuration pins are referred to as Bank 4





Project/Equipment	DI/OT		
Document	*DI/OT Rad-tol System Board FPGA Configuration and reset*	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check.by *	-
		Last Mod. C. Gentsos	16/11/2020
		File FPGA_Config.SchDoc	
		Print Date 16/11/2020 16:33:30	Sheet 5 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev *

Banks powered by PPERIPH

Caution on pin-swapping: the S0_P pins are connected to Global I/O pins to be able to drive FPGA clocks and can't be swapped with other peripheral I/Os.
Boards 1-3 can drive global buffers directly or use CCC blocks;
Boards 4-6 can drive global buffers directly or through VCCC crossbars; and
Boards 7-8 can only reach global buffers through CCC blocks.

IC1A
M2GL090T-FGG676I

BANK 0

MSIO111NB0	J12	SLOT1.LVDS_1_N
MSIO111PB0	J11	SLOT1.LVDS_1_P
MSIO112NB0	A9	SLOT1.LVDS_2_N
MSIO112PB0	A8	SLOT1.LVDS_2_P
MSIO113NB0	H11	SLOT1.LVDS_3_N
MSIO113PB0	G10	SLOT1.LVDS_3_P
MSIO114NB0	B8	SLOT1.LVDS_4_N
MSIO114PB0	A7	SLOT1.LVDS_4_P
MSIO115NB0	H10	SLOT1.LVDS_5_N
MSIO115PB0	H9	SLOT1.LVDS_5_P
MSIO116NB0	C8	SLOT1.LVDS_6_N
MSIO116PB0	D8	SLOT1.LVDS_6_P
MSIO117NB0	E10	SLOT1.LVDS_7_N
MSIO117PB0	E9	SLOT1.LVDS_7_P
MSIO118NB0	B7	SLOT1.LVDS_8_N
MSIO118PB0	B6	SLOT1.LVDS_8_P
MSIO119NB0	F9	SLOT1.LVDS_9_N
MSIO119PB0	G8	SLOT1.LVDS_9_P
MSIO120NB0	A5	SLOT1.LVDS_10_N
MSIO120PB0	A4	SLOT1.LVDS_10_P
MSIO121NB0	F7	SLOT1.LVDS_11_N
MSIO121PB0	E8	SLOT1.LVDS_11_P
MSIO122NB0	B5	SLOT1.LVDS_12_N
MSIO122PB0	C6	SLOT1.LVDS_12_P
MSIO123NB0	E5	SLOT1.LVDS_13_N
MSIO123PB0	E4	SLOT1.LVDS_13_P
MSIO124NB0	D7	SLOT1.LVDS_14_N
MSIO124PB0	D6	SLOT1.LVDS_14_P
MSIO125NB0	E6	SLOT1.LVDS_15_N
MSIO125PB0	E7	SLOT1.LVDS_15_P

IC1D
M2GL090T-FGG676I

BANK 3

MSIO0NB3	W22	SLOT1.LVDS_16_N	
MSIO0PB3	W21	SLOT1.LVDS_16_P	
MSIO1NB3	AA23	SLOT1.LVDS_17_N	
MSIO1PB3	Y22	SLOT1.LVDS_17_P	
MSIO2NB3	AC25	SLOT2.LVDS_1_N	
MSIO2PB3	AC24	SLOT2.LVDS_1_P	
MSIO3NB3	Y21	SLOT2.LVDS_2_N	
MSIO3PB3	Y20	SLOT2.LVDS_2_P	
MSIO4NB3	AC26	SLOT2.LVDS_3_N	
MSIO4PB3	AD26	SLOT2.LVDS_3_P	
MSIO5NB3	U21	SLOT2.LVDS_4_N	
MSIO5PB3	U20	SLOT2.LVDS_4_P	
MSIO6NB3	W24	SLOT2.LVDS_5_N	
MSIO6PB3	V23	SLOT2.LVDS_5_P	
MSIO7NB3	AA25	SLOT2.LVDS_6_N	
MSIO7PB3	AA24	SLOT2.LVDS_6_P	
MSIO8NB3	AB26	SLOT2.LVDS_7_N	
MSIO8PB3	AB25	SLOT2.LVDS_7_P	
MSIO11NB3/CCC_NE1_CLKI0	T22	SLOT8.LVDS_0_N	
MSIO11PB3/CCC_NE0_CLKI0	T22	SLOT8.LVDS_0_P	CC
MSIO12NB3/SPI_0_SDI	W26	SLOT2.LVDS_8_N	
MSIO12PB3/SPI_0_CLK	V26	SLOT2.LVDS_8_P	
MSIO13NB3/SPI_0_SS0	T23	SLOT2.LVDS_9_N	
MSIO13PB3/SPI_0_SDO	T23	SLOT2.LVDS_9_P	
MSIO14NB3	V26	SLOT2.LVDS_10_N	
MSIO14PB3	V25	SLOT2.LVDS_10_P	
MSIO15NB3	T20	SLOT2.LVDS_11_N	
MSIO15PB3	T19	SLOT2.LVDS_11_P	
MSIO16NB3	U26	SLOT2.LVDS_12_N	
MSIO16PB3	U25	SLOT2.LVDS_12_P	
MSIO17NB3	T18	SLOT2.LVDS_13_N	
MSIO17PB3	U18	SLOT2.LVDS_13_P	
MSIO18NB3	T25	SLOT2.LVDS_14_N	
MSIO18PB3	T24	SLOT2.LVDS_14_P	
MSIO19NB3	R21	SLOT2.LVDS_15_N	
MSIO19PB3	R22	SLOT2.LVDS_15_P	
MSIO20NB3/GB13/VCCC_SE1_CLKI	R25	SLOT4.LVDS_0_N	
MSIO20PB3/GB9/VCCC_SE0_CLKI	R24	SLOT4.LVDS_0_P	CC
MSIO21NB3	R19	SLOT2.LVDS_16_N	
MSIO21PB3	R20	SLOT2.LVDS_16_P	
MSIO22NB3	P26	SLOT2.LVDS_17_N	
MSIO22PB3	R26	SLOT2.LVDS_17_P	
MSIO23NB3	P19	SLOT3.LVDS_1_N	
MSIO23PB3	P18	SLOT3.LVDS_1_P	
MSIO24NB3	P24	SLOT3.LVDS_2_N	
MSIO24PB3	P23	SLOT3.LVDS_2_P	
MSIO25NB3	P22	SLOT3.LVDS_3_N	
MSIO25PB3	P21	SLOT3.LVDS_3_P	
MSIO26NB3	N25	SLOT3.LVDS_4_N	
MSIO26PB3	N26	SLOT3.LVDS_4_P	
MSIO27NB3	P16	SLOT3.LVDS_5_N	
MSIO27PB3	P17	SLOT3.LVDS_5_P	
MSIO28NB3	N23	SLOT3.LVDS_6_N	
MSIO28PB3	N24	SLOT3.LVDS_6_P	
MSIO29NB3	N19	SLOT3.LVDS_7_N	
MSIO29PB3	N18	SLOT3.LVDS_7_P	
MSIO30NB3	M25	SLOT3.LVDS_8_N	
MSIO30PB3	M26	SLOT3.LVDS_8_P	
MSIO32NB3	M22	SLOT3.LVDS_9_N	
MSIO32PB3	M23	SLOT3.LVDS_9_P	
MSIO33NB3	Y19	SLOT3.LVDS_10_N	
MSIO33PB3	Y18	SLOT3.LVDS_10_P	
MSIO34NB3	M24	SLOT3.LVDS_11_N	
MSIO34PB3	L25	SLOT3.LVDS_11_P	
MSIO35NB3	M18	SLOT3.LVDS_12_N	
MSIO35PB3	M17	SLOT3.LVDS_12_P	
MSIO36NB3	L26	SLOT3.LVDS_13_N	
MSIO36PB3	L26	SLOT3.LVDS_13_P	
MSIO37NB3	M20	SLOT3.LVDS_14_N	
MSIO37PB3	M21	SLOT3.LVDS_14_P	
MSIO38NB3	L24	SLOT3.LVDS_15_N	
MSIO38PB3	K25	SLOT3.LVDS_15_P	
MSIO39NB3	K19	SLOT3.LVDS_16_N	
MSIO39PB3	K20	SLOT3.LVDS_16_P	
MSIO40NB3	H25	SLOT3.LVDS_17_N	
MSIO40PB3	H26	SLOT3.LVDS_17_P	
MSIO41NB3	J19	SLOT4.LVDS_1_N	
MSIO41PB3	J20	SLOT4.LVDS_1_P	
MSIO42NB3	K25	SLOT4.LVDS_2_N	
MSIO42PB3	K26	SLOT4.LVDS_2_P	
MSIO43NB3	J18	SLOT4.LVDS_3_N	
MSIO43PB3	J17	SLOT4.LVDS_3_P	
MSIO44NB3	J22	SLOT4.LVDS_4_N	
MSIO44PB3	J23	SLOT4.LVDS_4_P	
MSIO45NB3	J23	SLOT4.LVDS_5_N	
MSIO45PB3	J24	SLOT4.LVDS_5_P	
MSIO46NB3	K21	SLOT4.LVDS_6_N	
MSIO46PB3	K22	SLOT4.LVDS_6_P	
MSIO47NB3	H23	SLOT4.LVDS_7_N	
MSIO47PB3	H24	SLOT4.LVDS_7_P	
MSIO48NB3	H19	SLOT4.LVDS_8_N	
MSIO48PB3	H19	SLOT4.LVDS_8_P	
MSIO49NB3	J21	SLOT4.LVDS_9_N	
MSIO49PB3	J22	SLOT4.LVDS_9_P	
MSIO50NB3	H20	SLOT4.LVDS_10_N	
MSIO50PB3	H21	SLOT4.LVDS_10_P	

IC1E
M2GL090T-FGG676I

BANK 5

MSIO195NB5	W13	SLOT4.LVDS_11_N	
MSIO195PB5	W12	SLOT4.LVDS_11_P	
MSIO196NB5/CCC_SW0_CLKI2	AC11	SLOT4.LVDS_12_N	
MSIO196PB5	AB11	SLOT4.LVDS_12_P	
MSIO197NB5/PROBE_B	AD12	SLOT4.LVDS_13_N	
MSIO197PB5/PROBE_A	AE12	SLOT4.LVDS_13_P	
MSIO198NB5	Y12	SLOT4.LVDS_14_N	
MSIO198PB5	AA12	SLOT4.LVDS_14_P	
MSIO199NB5	AF13	SLOT4.LVDS_15_N	
MSIO199PB5	AF12	SLOT4.LVDS_15_P	
MSIO201NB5/GB7/CCC_SW1_CLKI2	AB13	SLOT3.LVDS_0_N	
MSIO201PB5/GB3/CCC_SW0_CLKI3	AB12	SLOT3.LVDS_0_P	CC
MSIO202NB5	AE14	SLOT4.LVDS_16_N	
MSIO202PB5	AF14	SLOT4.LVDS_16_P	
MSIO203NB5	V14	SLOT4.LVDS_17_N	
MSIO203PB5	V13	SLOT4.LVDS_17_P	
MSIO204NB5	AD14	SLOT5.LVDS_1_N	
MSIO204PB5	AD13	SLOT5.LVDS_1_P	
MSIO205NB5	AC14	SLOT5.LVDS_2_N	
MSIO205PB5	AC13	SLOT5.LVDS_2_P	
MSIO206NB5	AF17	SLOT5.LVDS_3_N	
MSIO206PB5	AF18	SLOT5.LVDS_3_P	
MSIO207NB5	AA14	SLOT5.LVDS_4_N	
MSIO207PB5	AA13	SLOT5.LVDS_4_P	
MSIO208NB5	AE15	SLOT7.LVDS_0_N	
MSIO208PB5/CCC_SW1_CLKI3	AF15	SLOT7.LVDS_0_P	CC
MSIO209NB5	Y14	SLOT5.LVDS_5_N	
MSIO209PB5/VCCC_SE0_CLKI	W14	SLOT5.LVDS_5_P	
MSIO210NB5	AE17	SLOT5.LVDS_0_N	
MSIO210PB5/GB11/VCCC_SE0_CLKI	AE16	SLOT5.LVDS_0_P	CC
MSIO211NB5	Y17	SLOT5.LVDS_6_N	
MSIO211PB5	AA17	SLOT5.LVDS_6_P	
MSIO212NB5	AD17	SLOT6.LVDS_0_N	
MSIO212PB5/GB15/VCCC_SE1_CLKI	AD16	SLOT6.LVDS_0_P	CC
MSIO213NB5	AB15	SLOT5.LVDS_7_N	
MSIO213PB5/VCCC_SE1_CLKI	AC15	SLOT5.LVDS_7_P	
MSIO214NB5	Y15	SLOT5.LVDS_8_N	
MSIO214PB5	AA15	SLOT5.LVDS_8_P	
MSIO215NB5	AB16	SLOT5.LVDS_9_N	
MSIO215PB5	AC16	SLOT5.LVDS_9_P	
MSIO216NB5	AB17	SLOT5.LVDS_10_N	
MSIO216PB5	AB18	SLOT5.LVDS_10_P	
MSIO217NB5	V16	SLOT5.LVDS_11_N	
MSIO217PB5	V15	SLOT5.LVDS_11_P	
MSIO218NB5	AF20	SLOT5.LVDS_12_N	
MSIO218PB5	AF19	SLOT5.LVDS_12_P	
MSIO221NB5	W17	SLOT5.LVDS_13_N	
MSIO221PB5	W18	SLOT5.LVDS_13_P	
MSIO222NB5	AE20	SLOT5.LVDS_14_N	
MSIO222PB5	AE19	SLOT5.LVDS_14_P	
MSIO223NB5	W16	SLOT5.LVDS_15_N	
MSIO223PB5	Y16	SLOT5.LVDS_15_P	
MSIO224NB5	AD19	SLOT5.LVDS_16_N	
MSIO224PB5	AD18	SLOT5.LVDS_16_P	
MSIO225NB5	AE21	SLOT5.LVDS_17_N	
MSIO225PB5	AF22	SLOT5.LVDS_17_P	
MSIO226NB5	Y19	SLOT6.LVDS_1_N	
MSIO226PB5	W19	SLOT6.LVDS_1_P	
MSIO227NB5	AE22	SLOT6.LVDS_2_N	
MSIO227PB5	AF23	SLOT6.LVDS_2_P	
MSIO228NB5	Y20	SLOT6.LVDS_3_N	
MSIO228PB5	Y21	SLOT6.LVDS_3_P	
MSIO229NB5	AC19	SLOT6.LVDS_4_N	
MSIO229PB5	AC18	SLOT6.LVDS_4_P	
MSIO230NB5	V18	SLOT6.LVDS_5_N	
MSIO230PB5	V19	SLOT6.LVDS_5_P	
MSIO231NB5	AA19	SLOT6.LVDS_6_N	
MSIO231PB5	AA18	SLOT6.LVDS_6_P	
MSIO232NB5	AD23	SLOT6.LVDS_7_N	
MSIO232PB5	AD22	SLOT6.LVDS_7_P	
MSIO233NB5	AC20	SLOT6.LVDS_8_N	
MSIO233PB5	AD21	SLOT6.LVDS_8_P	
MSIO234NB5	AD24	SLOT6.LVDS_9_N	
MSIO234PB5	AE24	SLOT6.LVDS_9_P	
MSIO235NB5	AB21	SLOT6.LVDS_10_N	
MSIO235PB5	AC21	SLOT6.LVDS_10_P	
MSIO236NB5	AB23	SLOT6.LVDS_11_N	
MSIO236PB5	AC23	SLOT6.LVDS_11_P	
MSIO237NB5	AB22	SLOT6.LVDS_12_N	
MSIO237PB5	AA22	SLOT6.LVDS_12_P	
MSIO238NB5	AA20	SLOT6.LVDS_13_N	
MSIO238PB5	AB20	SLOT6.LVDS_13_P	

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BANK 8

MSIO126NB8	G7	SLOT6.LVDS_14_N	
MSIO126PB8	H8	SLOT6.LVDS_14_P	
MSIO127NB8	H6	SLOT6.LVDS_15_N	
MSIO127PB8	H5	SLOT6.LVDS_15_P	
MSIO128NB8	J7	SLOT6.LVDS_16_N	
MSIO128PB8	J6	SLOT6.LVDS_16_P	
MSIO129NB8	G6	SLOT6.LVDS_17_N	
MSIO129PB8	G5	SLOT6.LVDS_17_P	
MSIO131NB8	F5	SLOT7.LVDS_1_N	
MSIO131PB8	E5	SLOT7.LVDS_1_P	
MSIO132NB8	E4	SLOT7.LVDS_2_N	
MSIO132PB8	D4	SLOT7.LVDS_2_P	
MSIO133NB8	D3	SLOT7.LVDS_3_N	
MSIO133PB8	C3	SLOT7.LVDS_3_P	
MSIO134NB8	B3	SLOT7.LVDS_4_N	
MSIO134PB8	B4	SLOT7.LVDS_4_P	
MSIO135NB8	H4	SLOT7.LVDS_5_N	
MSIO135PB8	H3	SLOT7.LVDS_5_P	
MSIO136NB8	F3	SLOT7.LVDS_6_N	
MSIO136PB8	F3	SLOT7.LVDS_6_P	
MSIO137NB8	J9	SLOT7.LVDS_7_N	
MSIO137PB8	J8	SLOT7.LVDS_7_P	
MSIO138NB8	A3	SLOT7.LVDS_8_N	
MSIO138PB8	A2	SLOT7.LVDS_8_P	
MSIO139NB8	K9	SLOT7.LVDS_9_N	
MSIO139PB8	K10	SLOT7.LVDS_9_P	
MSIO140NB8	B2	SLOT7.LVDS_10_N	
MSIO140PB8	B1	SLOT7.LVDS_10_P	
MSIO142NB8	L10	SLOT7.LVDS_11_N	
MSIO142PB8	L9	SLOT7.LVDS_11_P	
MSIO143NB8	J4	SLOT7.LVDS_12_N	
MSIO143PB8	J3	SLOT7.LVDS_12_P	
MSIO145NB8	K7	SLOT7.LVDS_13_N	
MSIO145PB8	L7	SLOT7.LVDS_13_P	
MSIO146NB8	K5	SLOT7.LVDS_14_N	
MSIO146PB8	K6	SLOT7.LVDS_14_P	
MSIO147NB8	L8	SLOT7.LVDS_15_N	
MSIO147PB8	M8	SLOT7.LVDS_15_P	
MSIO148NB8	D2	SLOT7.LVDS_16_N	
MSIO148PB8	E1	SLOT7.LVDS_16_P	
MSIO149NB8	E2	SLOT7.LVDS_17_N	
MSIO149PB8	D1	SLOT7.LVDS_17_P	
MSIO150NB8	F2	SLOT8.LVDS_1_N	
MSIO150PB8	F1	SLOT8.LVDS_1_P	
MSIO151NB8	L5	SLOT8.LVDS_2_N	
MSIO151PB8	M5	SLOT8.LVDS_2_P	
MSIO152NB8	L4	SLOT8.LVDS_3_N	
MSIO152PB8	K4	SLOT8.LVDS_3_P	
MSIO153NB8	M6	SLOT8.LVDS_4_N	
MSIO153PB8	M7	SLOT8.LVDS_4_P	
MSIO154NB8	G2	SLOT8.LVDS_5_N	
MSIO154PB8	G1	SLOT8.LVDS_5_P	
MSIO156NB8	P4	SLOT2.LVDS_0_N	
MSIO156PB8/GB6/CCC_NW1_CLKI1	N4	SLOT2.LVDS_0_P	CC
MSIO157NB8	N5	SLOT1.LVDS_0_N	
MSIO157PB8/GB2/CCC_NW0_CLKI1	N6	SLOT1.LVDS_0_P	CC
MSIO158NB8	M3	SLOT8.LVDS_6_N	
MSIO158PB8/CCC_NW1_CLKI0	N3	SLOT8.LVDS_6_P	
MSIO159NB8	N8	SLOT8.LVDS_7_N	
MSIO159PB8/CCC_NW0_CLKI0	N9	SLOT8.LVDS_7_P	
MSIO160NB8	L3	SLOT8.LVDS_8_N	
MSIO160PB8	L2	SLOT8.LVDS_8_P	
MSIO161NB8	L2	SLOT8.LVDS_9_N	
MSIO161PB8	M2	SLOT8.LVDS_9_P	
MSIO163NB8	M10	SLOT8.LVDS_10_N	
MSIO163PB8	N10	SLOT8.LVDS_10_P	
MSIO165NB8	P6	SLOT8.LVDS_11_N	
MSIO165PB8	P7	SLOT8.LVDS_11_P	
MSIO166NB8	J2	SLOT8.LVDS_12_N	
MSIO166PB8	J1	SLOT8.LVDS_12_P	
MSIO167NB8	J1	SLOT8.LVDS_13_N	
MSIO167PB8	K1	SLOT8.LVDS_13_P	
MSIO168NB8	P3	SLOT8.LVDS_14_N	
MSIO168PB8	P4	SLOT8.LVDS_14_P	
MSIO170NB8	M1	SLOT8.LVDS_15_N	
MSIO170PB8	N1	SLOT8.LVDS_15_P	
MSIO172NB8	P2	SLOT8.LVDS_16_N	
MSIO172PB8	R2	SLOT8.LVDS_16_P	
MSIO173NB8	P1	SLOT8.LVDS_17_N	
MSIO173PB8	R1	SLOT8.LVDS_17_P	

PERIPH_CONN

- LVDS_0_P
- LVDS_0_N
- LVDS_1_P
- LVDS_1_N
- LVDS_2_P
- LVDS_2_N
- LVDS_3_P
- LVDS_3_N
- LVDS_4_P
- LVDS_4_N
- LVDS_5_P
- LVDS_5_N
- LVDS_6_P
- LVDS_6_N
- LVDS_7_P
- LVDS_7_N
- LVDS_8_P
- LVDS_8_N
- LVDS_9_P
- LVDS_9_N
- LVDS_10_P
- LVDS_10_N
- LVDS_11_P
- LVDS_11_N
- LVDS_12_P
- LVDS_12_N
- LVDS_13_P
- LVDS_13_N
- LVDS_14_P
- LVDS_14_N
- LVDS_15_P
- LVDS_15_N
- LVDS_16_P
- LVDS_16_N
- LVDS_17_P
- LVDS_17_N

Intra-diff pair rule. Inter-diff pair rules can be found on a dedicated sheet.

Matched Net Lengths [Tolerance = 2mm]
ClassName: PERIPH_DP

SLOT1	SLOT1
SLOT2	SLOT2
SLOT3	SLOT3
SLOT4	SLOT4
SLOT5	SLOT5
SLOT6	SLOT6
SLOT7	SLOT7
SLOT8	SLOT8

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B0, B3	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	16/11/2020
		File FPGA_Banks_0_3_5_8.SchDoc	
		Print Date 16/11/2020 16:33:31	Sheet 6 of 17
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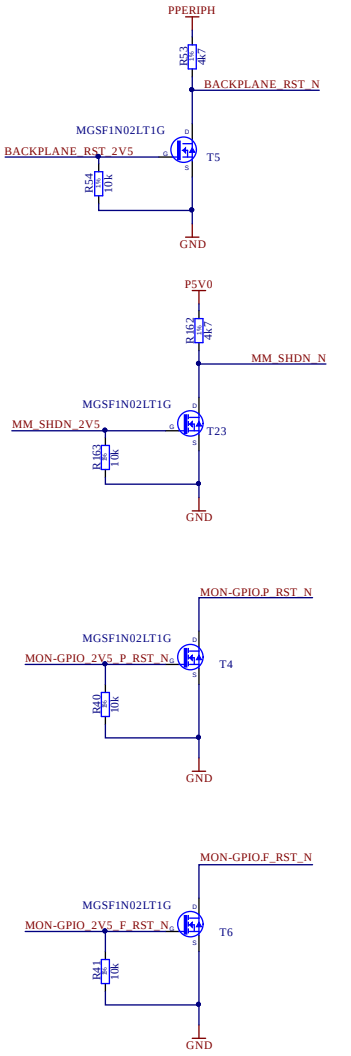
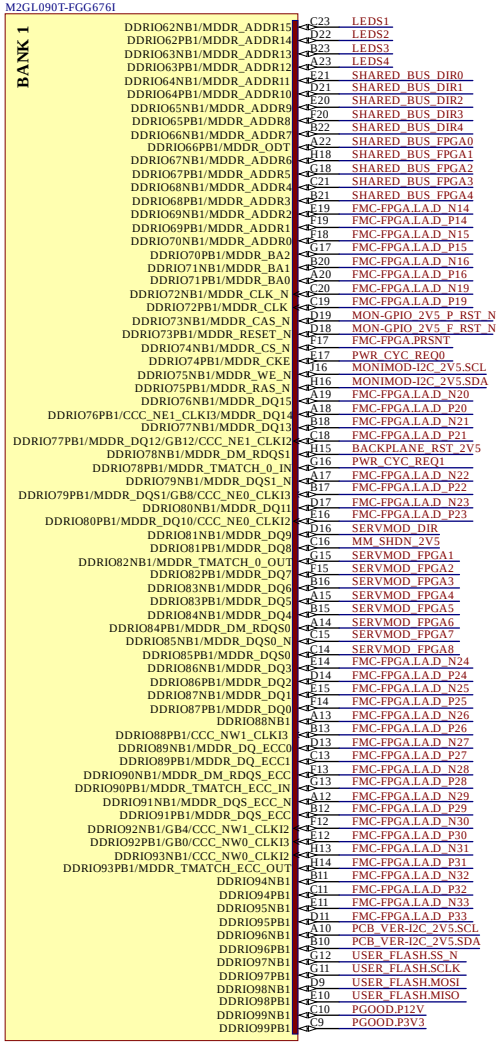
Bank 1 powered by 2.5V, Bank 2 by 3.3V

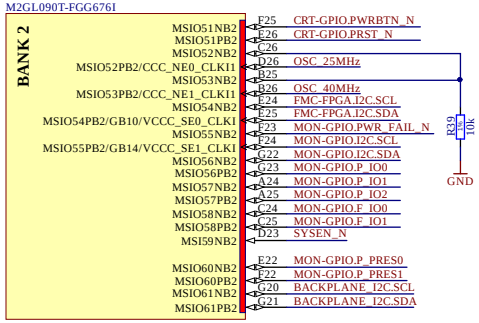
Level translators

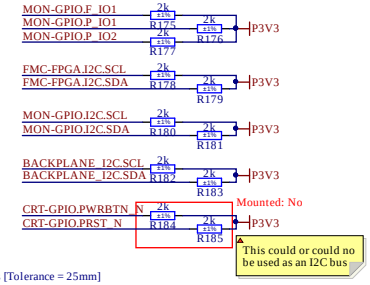


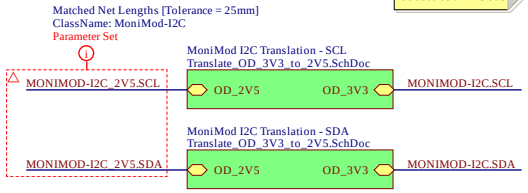
IC1B
M2GL090T-FGG676I

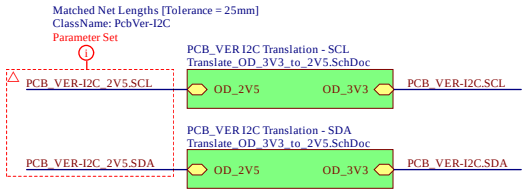


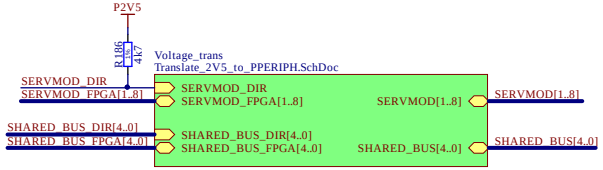
IC1C
M2GL090T-FGG676I

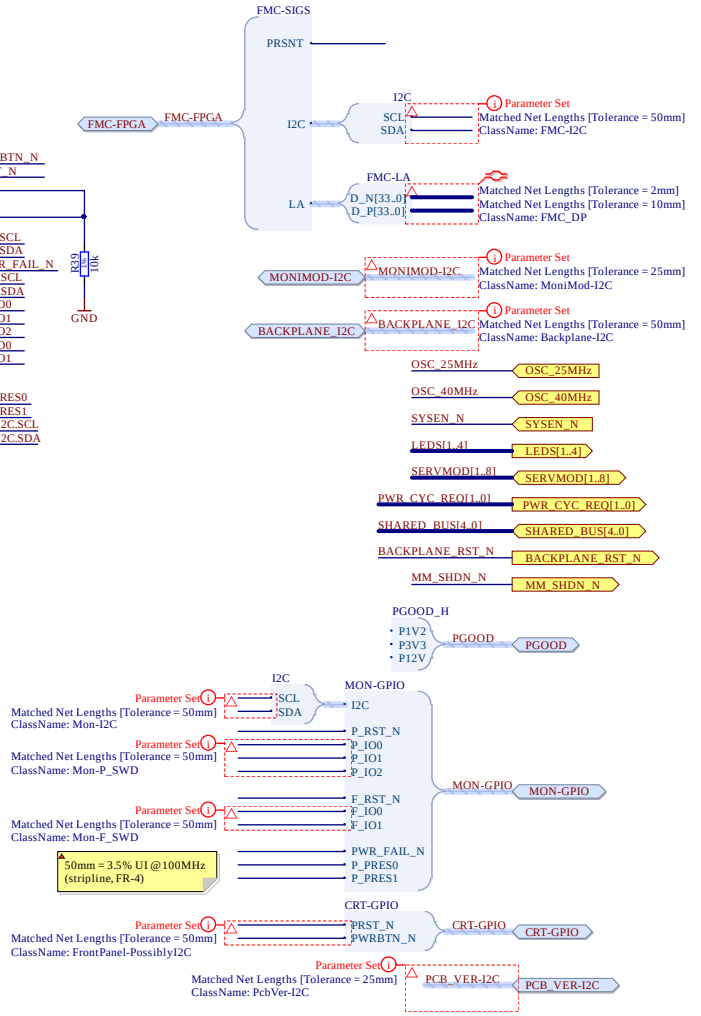




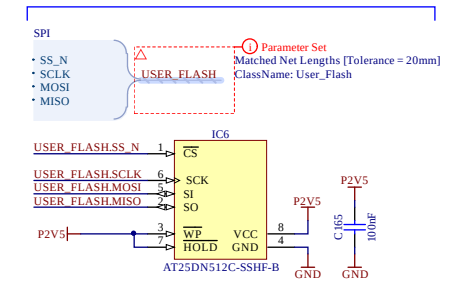








SPI Flash



Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B1, B2	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	16/11/2020
		File FPGA_Banks_1_2.SchDoc	
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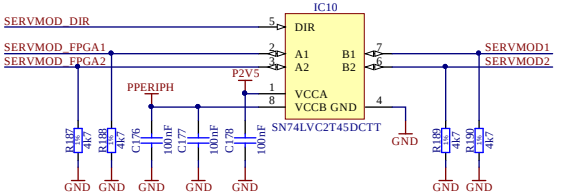
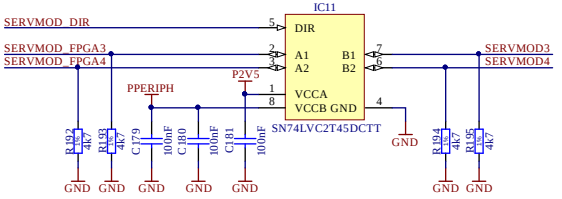
Bi-directional level translators

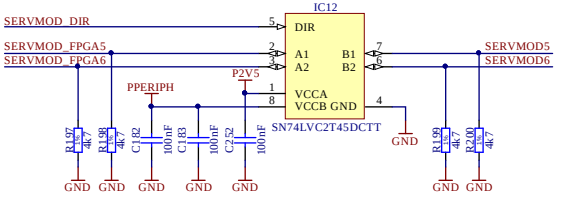
Maybe that's nit-picking but according to the datasheet, VCCB must be ramped-up with or after VCCA. If VCCB is set to 3V3 its ramp-up will come just slightly ahead of VCCA but not by much.

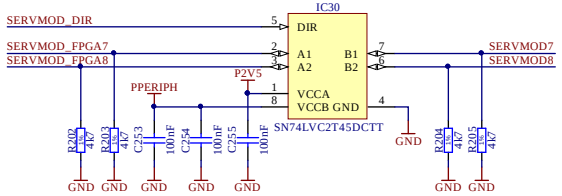
SHARED_BUS_DIR[4..0] → SHARED_BUS_DIR[4..0]
SHARED_BUS_FPGA[4..0] → SHARED_BUS_FPGA[4..0]
SHARED_BUS[4..0] → SHARED_BUS[4..0]

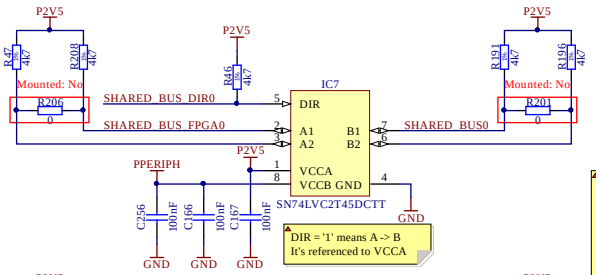
SERVMOD_DIR → SERVMOD_DIR
SERVMOD_FPGA[1..8] → SERVMOD_FPGA[1..8]
SERVMOD[1..8] → SERVMOD[1..8]







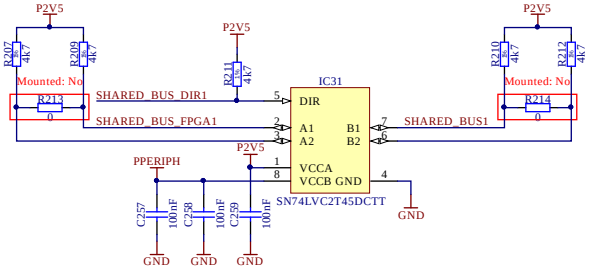


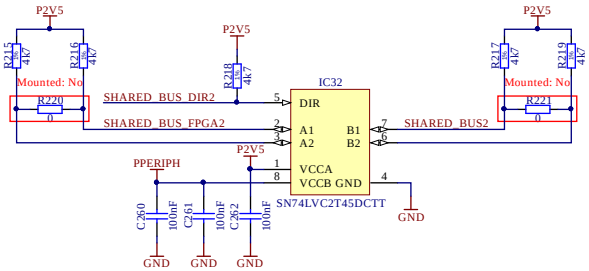


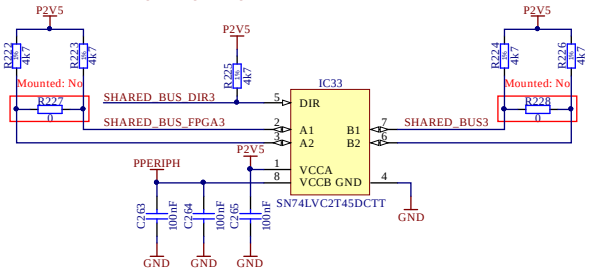
DIR = '1' means A -> B
It's referenced to VCCA

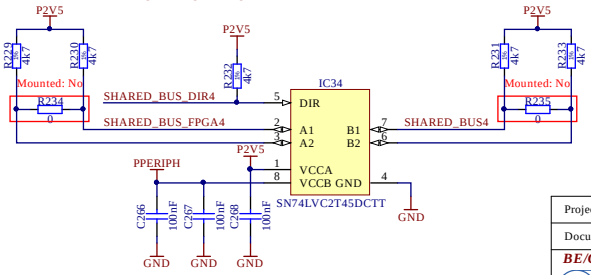
We used to have both I/Os connected together for more drive strength but at 3.3V that might be too much: each pin can already source or sink 24mA.

At 2.5V and 1.8V, however, that quickly drops to 8mA and 4mA, respectively. For applications with low PPERIPH, the optionally-mounted 0R resistors can provide the double drive strength, if necessary.









Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Voltage Translators	Designer C. Gentsos	
		Drawn by C. Gentsos	16/09/2020
		Check by *	-
		Last Mod. C. Gentsos	13/11/2020
		File Translate_2V5_to_PPERIPH.SchDoc	
		Print Date 16/11/2020 16:33:32	Sheet 8 of 17
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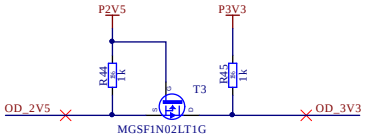
Level translators for open-drain interfaces as described in AN10441

OD_2V5 — OD_2V5

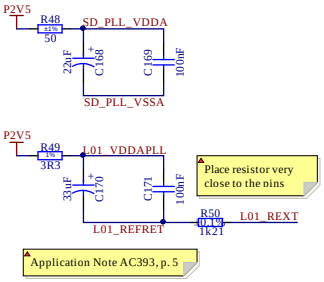
OD_3V3 — OD_3V3

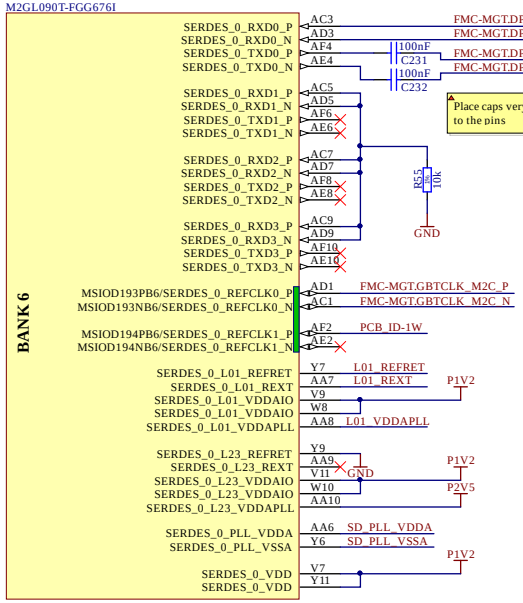


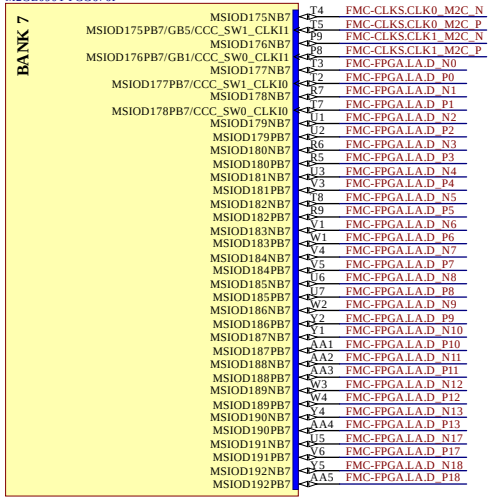
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Open-drain Voltage Translators	Designer C. Gentsos	
		Drawn by C. Gentsos	06/10/2020
		Check by *	-
		Last Mod. C. Gentsos	11/11/2020
		File Translate_OD_3V3_to_2V5.SchDoc	
		Print Date 16/11/2020 16:33:33	Sheet 9 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev *

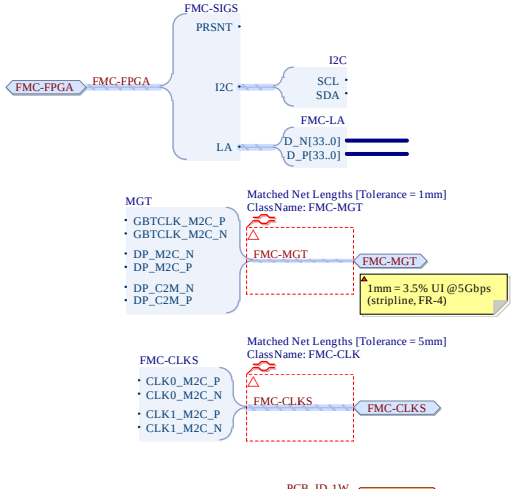
Banks powered by 2.5V

SerDes PLL RC filters





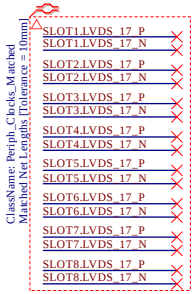


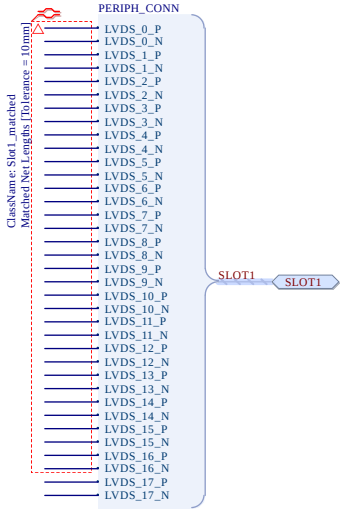


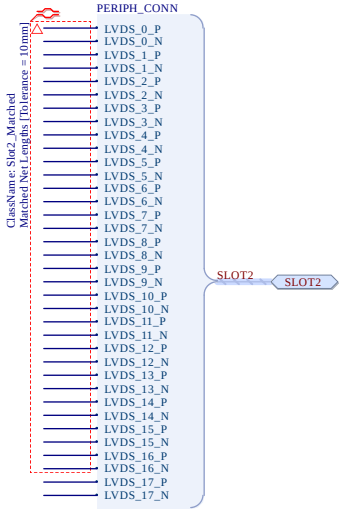
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FPGA I/O Banks B6, B7	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	16/11/2020
		File FPGA_Banks_6_7.SchDoc	
		Print Date 16/11/2020 16:33:33	Sheet 10of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

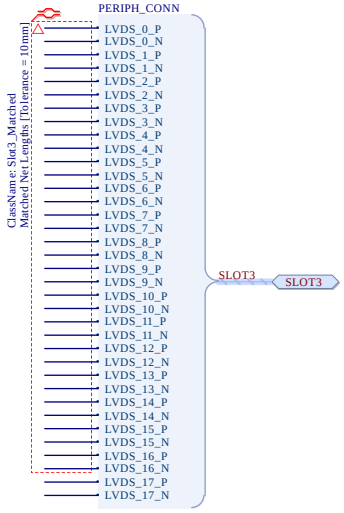
The diff. pairs that go to each peripheral board are length-matched, excluding the clock-capable pair

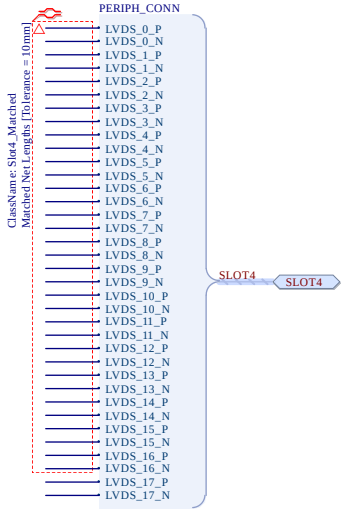
The clock-capable pairs are length-matched between the different peripheral boards, instead

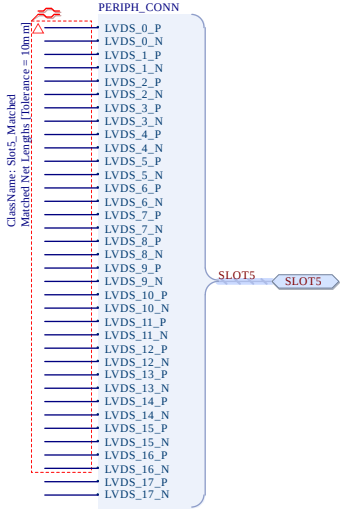


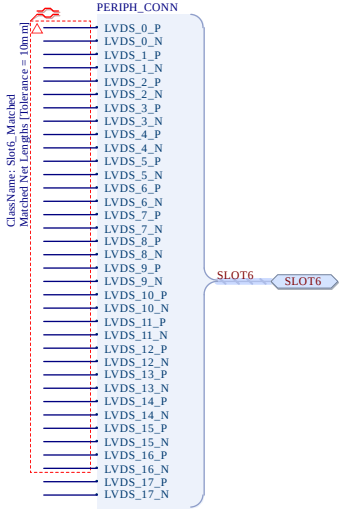


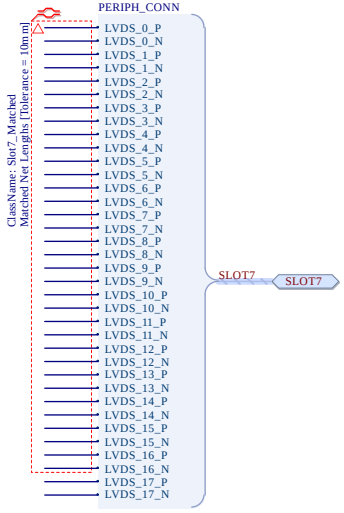


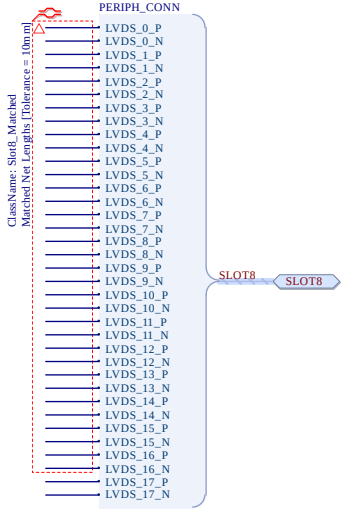












Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board Constrain Periph. Board Signals**	Designer C. Gentsos	
		Drawn by C. Gentsos	09/10/2020
		Check by *	-
		Last Mod. C. Gentsos	16/11/2020
		File Constrain_Periph_Nets.SchDoc	
		Print Date 16/11/2020 16:33:33	Sheet 11 of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

PESD3V3S4UD

CRT-GPIO.PRST_N
CRT-GPIO.PWRBTN_N
PS_ON_N
SHARED_BUS0
SHARED_BUS1
SHARED_BUS2
SHARED_BUS3
SHARED_BUS4

BACKPLANE_I2C.SDA
BACKPLANE_I2C.SCL
BACKPLANE_RST_N
MON-GPIO.P_IO0
MON-GPIO.P_IO1
MON-GPIO.P_IO2
MON-GPIO.F_IO0
MON-GPIO.F_IO1

MON-GPIO.PWR_FAIL_N
MON-GPIO.I2C.SCL
MON-GPIO.I2C.SDA
MON-GPIO.P_PRES0
MON-GPIO.P_PRES1
MON-GPIO.P_RST_N
MON-GPIO.F_RST_N

All the nets that are exposed to the front panel, the power backplane, or that run through all the peripheral boards, are protected

I2C
- SCL
- SDA

MON-GPIO
- I2C
- P_RST_N
- P_IO0
- P_IO1
- P_IO2
- F_RST_N
- F_IO0
- F_IO1
- PWR_FAIL_N
- P_PRES0
- P_PRES1

The P_* signals program and reset the two PSU MoniMods, similarly the F_* signals for the fan MoniMod. The I2C bus runs through all three of those.

MON-GPIO → MON-GPIO

CRT-GPIO
- PRST_N
- PWRBTN_N

General-purpose signals exposed at the front panel

CRT-GPIO → CRT-GPIO

SLOT1 SLOT2 SLOT3 SLOT4 SLOT5 SLOT6 SLOT7 SLOT8

SHARED_BUS[4..0]
BACKPLANE_RST_N
BACKPLANE_I2C
SYSEN_N

SHARED_BUS: 5-bit general-purpose bus that runs through all peripheral boards (DIOT specs 7.1.2)
BACKPLANE_RST_N: reset for the peripheral boards, generated on the System Board.
BACKPLANE_I2C: I2C bus that runs through the system boards.
SYSSLOT_N: 0 when inserted in the system slot, 1 when it's in a peripheral slot

PS_ON_N

Main 12V power supply turned off when that's high

Backplane grounds L2 at the system slot, leaves it open at the peripheral slots. Sensing that we can tell where we're plugged in.

P1 Connector

<slot>_JT_* JTAG functionality is enabled when a peripheral board is in service mode

<slot>_MTX / <slot>_MRX signals can be connected to MGT transceivers on the non-rad-tol system board

P12V_CPCIS
P5V0_SBY
P3V3
4k7 R66
SYSEN_N

J1A J1B J1C J1D J1E J1F

BACKPLANE_I2C.SCL R126
BACKPLANE_I2C.SDA R127
PS_ON_N R128
BACKPLANE_RST_N R129
CRT-GPIO.PRST_N R130
SHARED_BUS0 R131
CRT-GPIO.PWRBTN_N R132
MON-GPIO.PWR_FAIL_N R133
SHARED_BUS1 R134
SHARED_BUS2 R135
SHARED_BUS3 R136
SHARED_BUS4 R137

SLOT1.LVDS_0_P/N
SLOT1.LVDS_1_P/N
SLOT1.LVDS_2_P/N
SLOT1.LVDS_3_P/N
SLOT1.LVDS_4_P/N
SLOT1.LVDS_5_P/N
SLOT1.LVDS_6_P/N
SLOT1.LVDS_7_P/N
SLOT1.LVDS_8_P/N
SLOT1.LVDS_9_P/N
SLOT1.LVDS_10_P/N
SLOT1.LVDS_15_P/N
SLOT1.LVDS_16_P/N

P2 Connector

J2A J2B J2C J2D J2E J2F J2G J2H

MON-GPIO.I2C.SCL R138
MON-GPIO.I2C.SDA R139
MON-GPIO.P_IO1 R140
MON-GPIO.P_IO2 R141
MON-GPIO.P_PRES0 R142
MON-GPIO.P_PRES1 R143
MON-GPIO.F_RST_N R144
MON-GPIO.F_IO0 R145
MON-GPIO.P_RST_N R146
MON-GPIO.P_IO0 R147
MON-GPIO.F_IO1 R148

SLOT2.LVDS_15_P/N
SLOT2.LVDS_16_P/N
SLOT2.LVDS_5_P/N
SLOT2.LVDS_6_P/N
SLOT2.LVDS_7_P/N
SLOT2.LVDS_8_P/N
SLOT2.LVDS_9_P/N
SLOT2.LVDS_10_P/N
SLOT2.LVDS_2_P/N
SLOT3.LVDS_2_P/N
SLOT4.LVDS_2_P/N

P3 Connector

J3A J3B J3C J3D J3E J3F J3G J3H

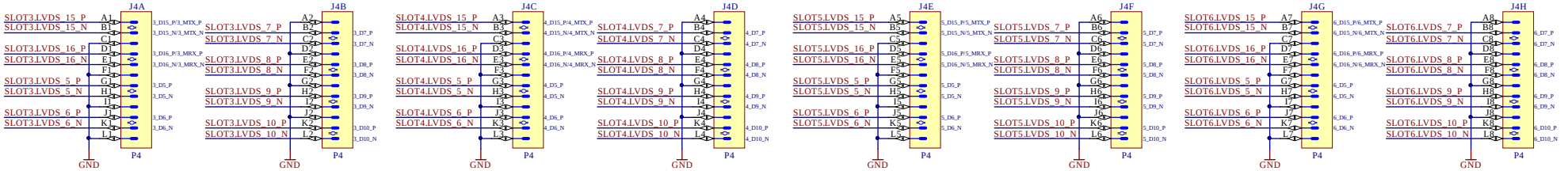
SLOT5.LVDS_2_P/N
SLOT6.LVDS_2_P/N
SLOT7.LVDS_2_P/N
SLOT8.LVDS_2_P/N
SLOT2.LVDS_0_P/N
SLOT2.LVDS_1_P/N
SLOT3.LVDS_0_P/N
SLOT3.LVDS_1_P/N
SLOT4.LVDS_0_P/N
SLOT4.LVDS_1_P/N
SLOT5.LVDS_0_P/N
SLOT5.LVDS_1_P/N
SLOT6.LVDS_0_P/N
SLOT6.LVDS_1_P/N
SLOT7.LVDS_0_P/N
SLOT7.LVDS_1_P/N
SLOT8.LVDS_0_P/N
SLOT8.LVDS_1_P/N
SLOT3.LVDS_3_P/N
SLOT3.LVDS_4_P/N
SLOT4.LVDS_3_P/N
SLOT4.LVDS_4_P/N
SLOT5.LVDS_3_P/N
SLOT5.LVDS_4_P/N
SLOT6.LVDS_3_P/N
SLOT6.LVDS_4_P/N
SLOT7.LVDS_3_P/N
SLOT7.LVDS_4_P/N
SLOT8.LVDS_3_P/N
SLOT8.LVDS_4_P/N

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board CPCI-S Backplane (1/2)	Designer	C. Gentsos
		Drawn by	C. Gentsos 28/08/2020
		Check by	* -
		Last Mod.	C. Gentsos 11/11/2020
		File	CPCI-S_Backplane_P1-P3.SchDoc
		Print Date	16/11/2020 16:33:34 Sheet 12of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 Rev *

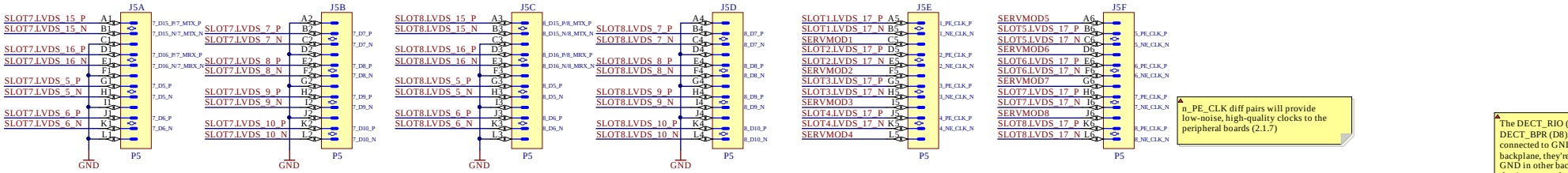
SLOT1 SLOT1
SLOT2 SLOT2
SLOT3 SLOT3
SLOT4 SLOT4
SLOT5 SLOT5
SLOT6 SLOT6
SLOT7 SLOT7
SLOT8 SLOT8

SERVMOD[1..8] SERVMOD[1..8]

P4 Connector



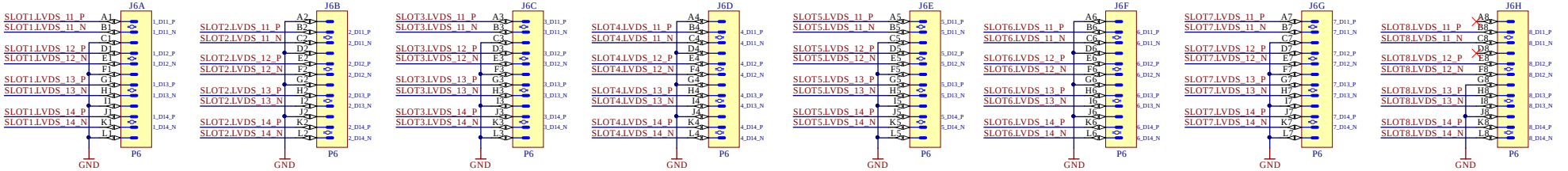
P5 Connector



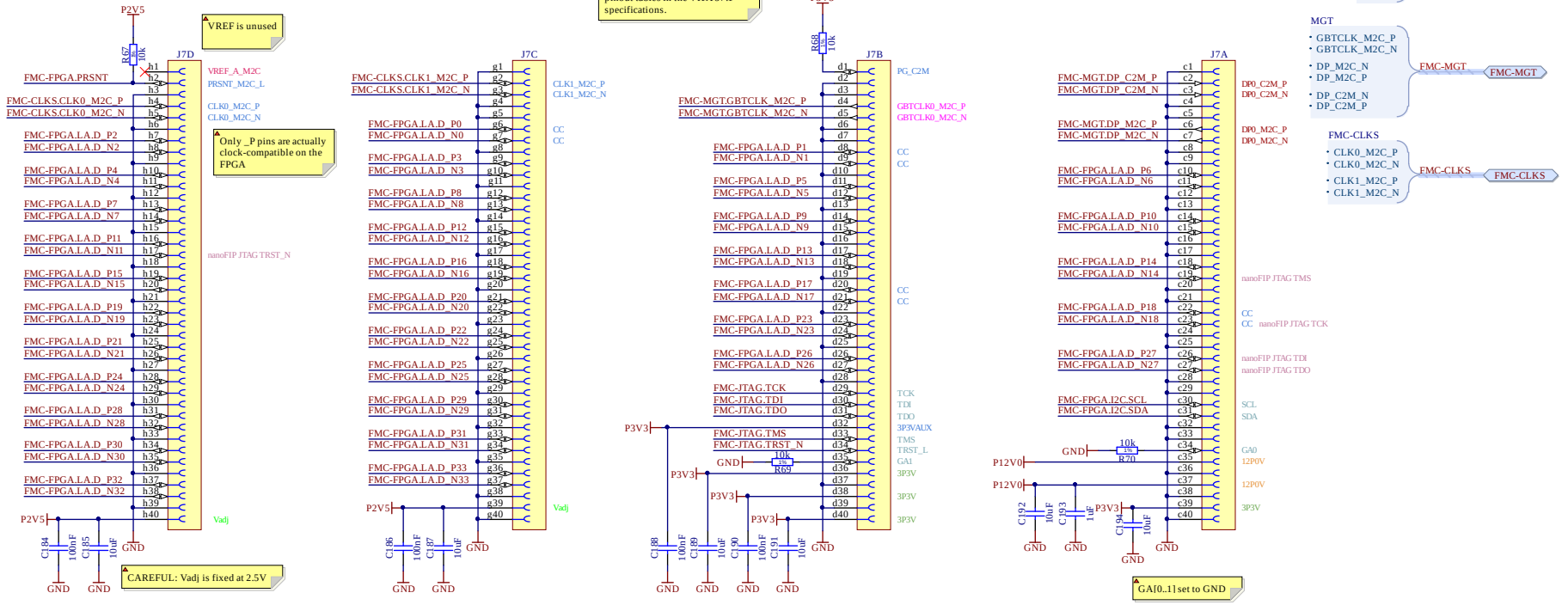
n_PE_CLK diff pairs will provide low-noise, high-quality clocks to the peripheral boards (2.1.7)

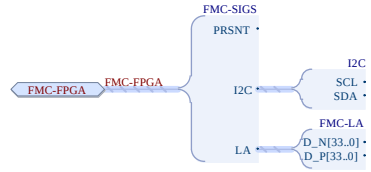
The DECT_RIO (A8) and DECT_BPR (D8) pins are connected to GND in the DI/OT backplane, they're not necessarily GND in other backplanes. As they're not used, they're left unconnected to improve compatibility.

P6 Connector



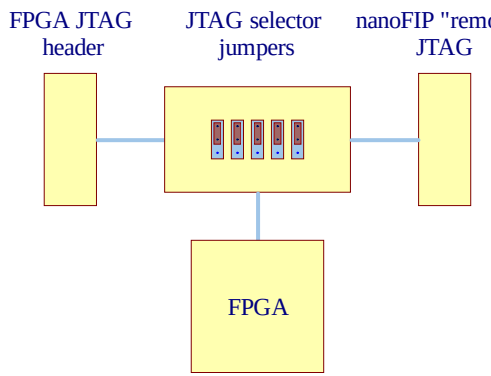
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board CPCI-S Backplane (2/2)	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	11/11/2020
		File CPCI-S_Backplane_P4-P6.SchDoc	
		Print Date 16/11/2020 16:33:36	Sheet 13of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

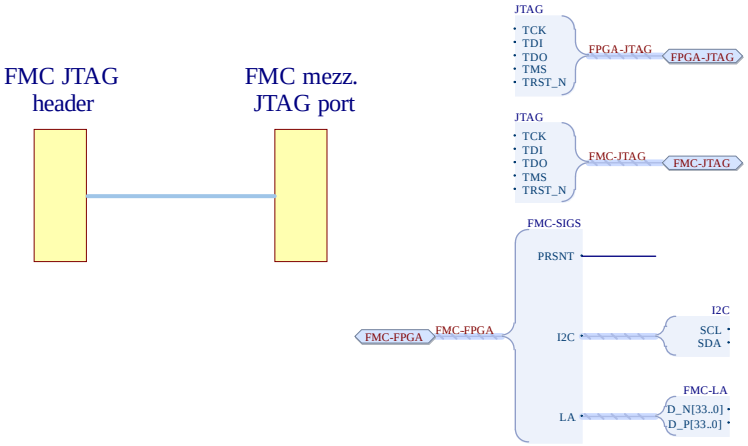




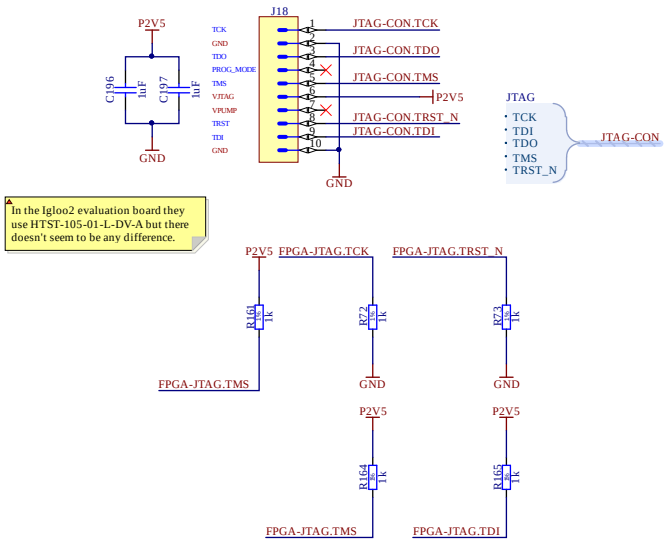
Mounting holes

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board FMC	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	11/11/2020
		File FMC.SchDoc	
		Print Date 16/11/2020 16:33:36	Sheet 14of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	Size A3 / Rev *

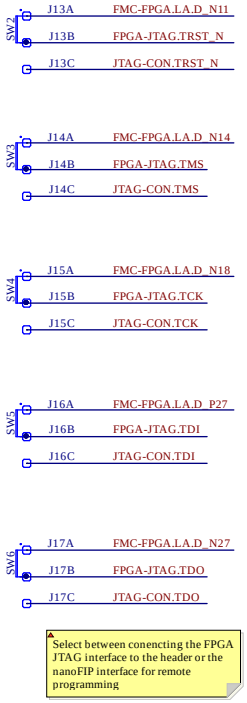




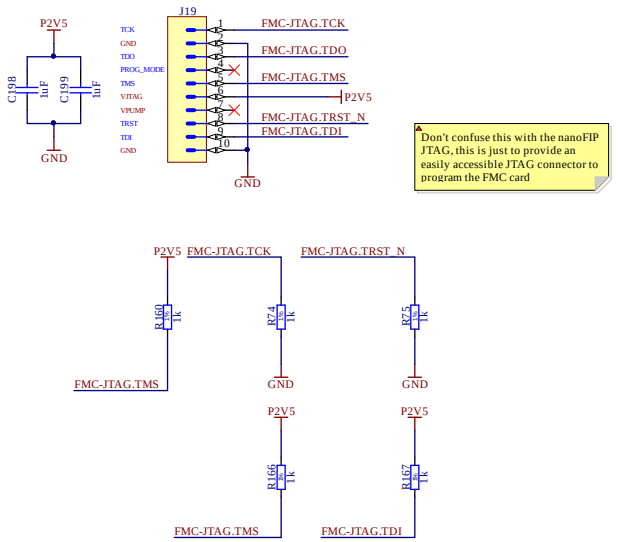
FPGA JTAG header



FPGA JTAG selector



FMC JTAG header



Project/Equipment	DI/OT		
Document	**DI/OT Rad-tol System Board JTAG Chains**	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	11/11/2020
		File JTAG.SchDoc	
		Print Date 16/11/2020 16:33:37	Sheet 15of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev *

SENSE
- P12V0+
- P12V0-
- P1V2+
- P1V2-
- P3V3+
- P3V3-
- PPERIPH+
- PPERIPH-

SENSE → SENSE

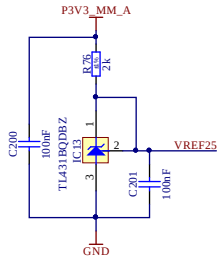
MONIMOD-I2C → MONIMOD-I2C

TEMP_LDO → TEMP_LDO

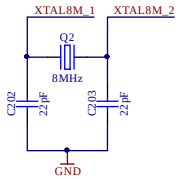
TEMP_FPGA → TEMP_FPGA

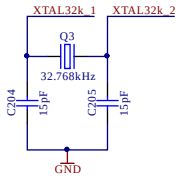
TEMP_AMB → TEMP_AMB

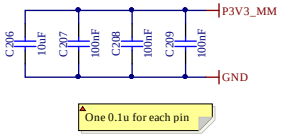
Voltage reference

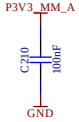


XTALs

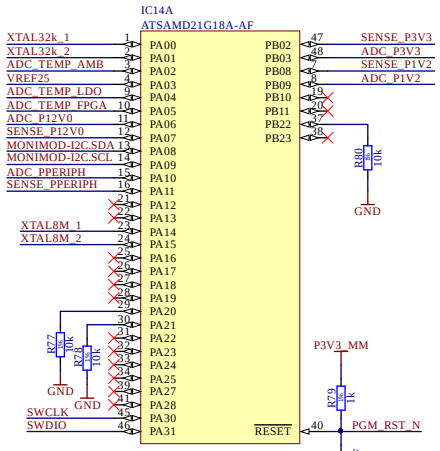


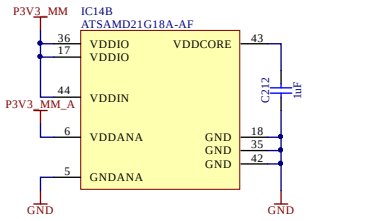


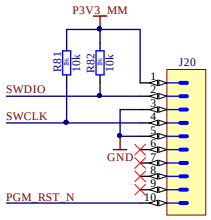




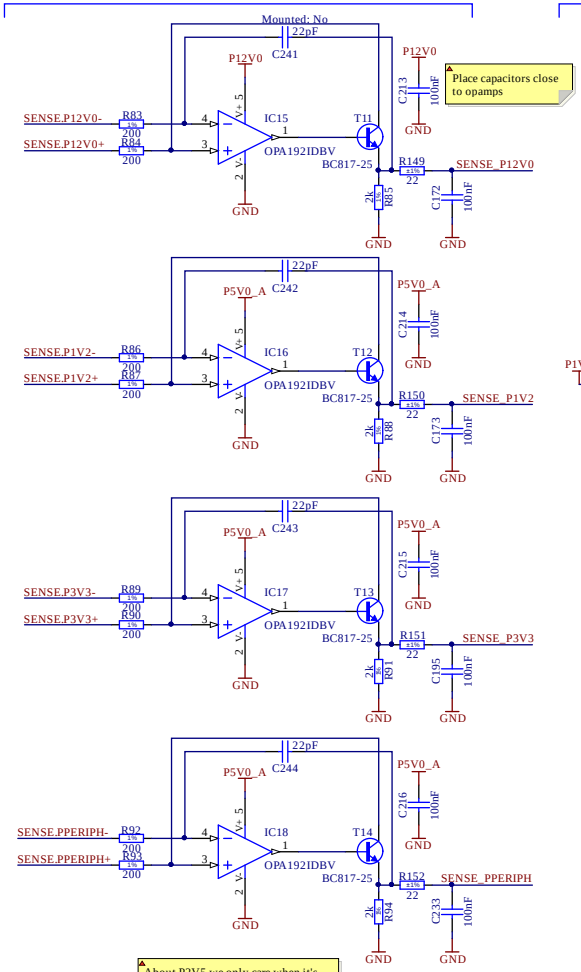
uC running MoniMod FW



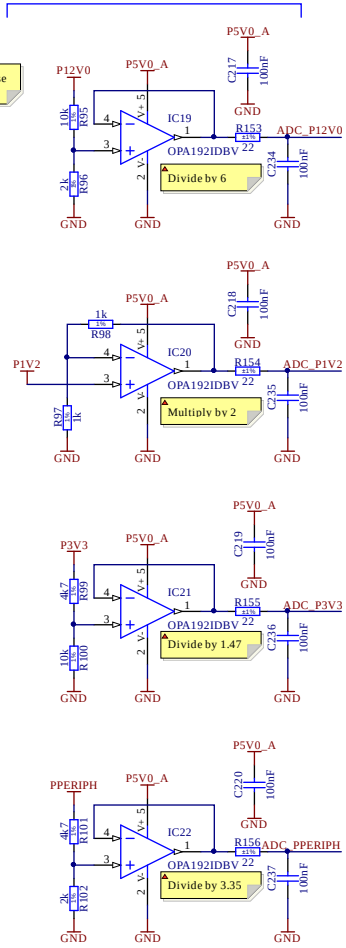




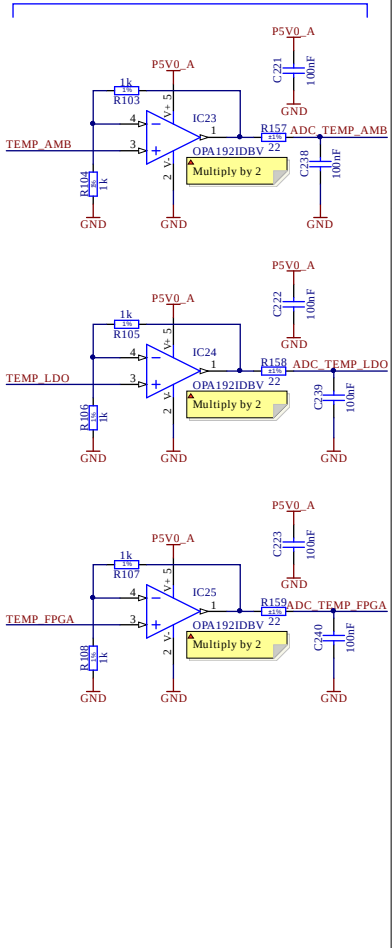
Current sense



Voltage div. and buffers

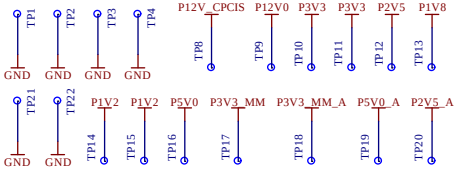


Temp. sensor amps



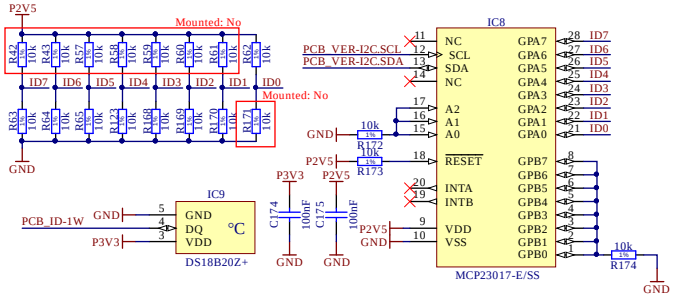
Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Monitoring	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	11/11/2020
		File Monitoring.SchDoc	
		Print Date 16/11/2020 16:33:37	Sheet 16of 17
BE/CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3 / Rev *

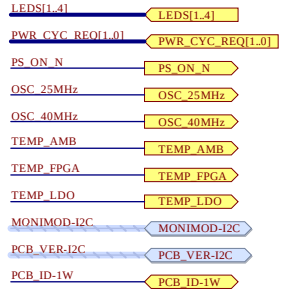
Power rail test points



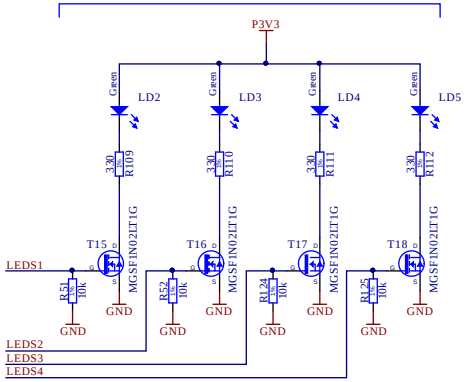
Place Test Points on top layer

Board version encoding and ID

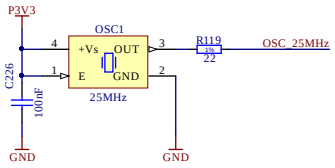




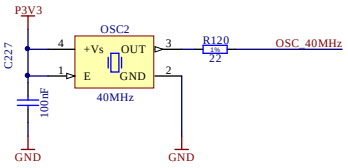
User LEDs



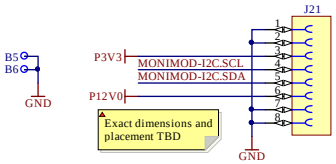
25MHz oscillator



40MHz oscillator

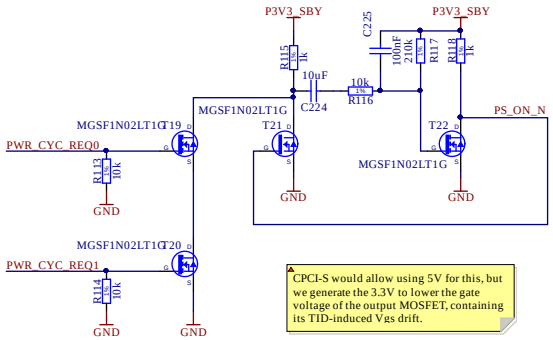


Expansion pin header



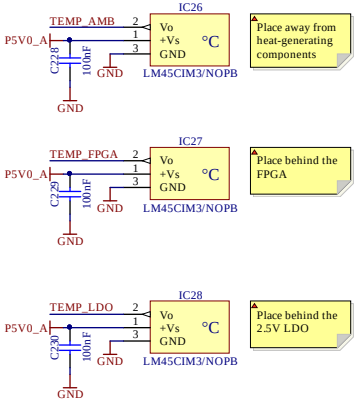
Exact dimensions and placement TBD

Power cycle pulse generator

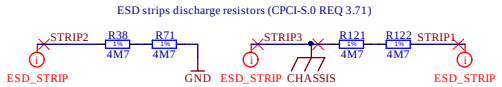


CPCI-S would allow using 5V for this, but we generate the 3.3V to lower the gate voltage of the output MOSFET, containing its TID-induced Vgs drift.

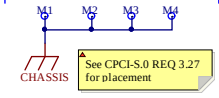
Temp sensors



ESD Protection

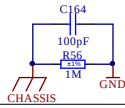


Front panel mounting holes



See CPCI-S.0 REQ 3.27 for placement

Chassis-GND connection



Fiducials

Project/Equipment	DI/OT		
Document	DI/OT Rad-tol System Board Miscellaneous	Designer C. Gentsos	
		Drawn by C. Gentsos	28/08/2020
		Check by *	-
		Last Mod. C. Gentsos	13/11/2020
		File Top_Misc.SchDoc	
		Print Date 16/11/2020 16:33:38	Sheet 17of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev *