Document: DI/OT System Board

Project/Equipment: DI/OT System Board

WR clocks

WR_DAC

SCLK\ D\ VCC\ SYSEX\ SYSEX

WR_DAC

SCLK\ D\ VCC\ SYSEX\ SYSEX

GND

OUT 4
GND
GND
VCC
VCO
9

2Y
6

GND
3

VREF
2

VCC_PLL1
18
GND

TRIM
5

Digilock 23MHz-2.5%/+/-5

OS1
OD2
PR1
OS1:0 = 01 => output type is LVDS, OSC_OUT=off
OD2:0=011, output divider = 4
PR1:0 = 11, prescaler divider =4, feedback divider = 20

<OSI lead to GND to set the output voltage standard to LVDS. Digilock is supported only for SR boards. This choice is available for this FPGA.>

AD5662BRMZ-1

DIN7
SYNC5
VDD1
DIN7
SCLK6
SYNC5

P3V3_CLK

REF5030AID
GND4
TEMP3
NC1
IC12

C78
240
C76
100nF

PLLDAC_OUT1
PLLDAC_OUT2

AD5662BRMZ-1

VIN1

OSC3

VM53S3-25.000-2.5/-30+75

SN74LVT125D

IC20

VCC14

4A12
2A5
1A2
4OE13

25MHz

R235
R234
30
1%

R251
1%

R56
R55

NC 8
REGCAP217
REGCAP119

VCCPLL2 16
GND122

C355
1%

OS110
OD013
PR025
RSTN12
CE7

L19

C364
4.7uF

GND

GND

VFB 3

P3V0_REF

NC 4

C434
1%

VC1

+Vs4

OS1:0 = 01 => output type is LVDS, OSC_OUT=off
OD2:0=011, output divider = 4
PR1:0 = 11, prescaler divider =4, feedback divider = 20

LVPECL is supported only for HR banks

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Source location: (https://www.cern.ch/di/ot-sb-eda)>

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Si5341 is not sensitive to power sequencing. We use P1V8_AUX to also supply the FPGA_CLK_OUT. Otherwise, we would be very close to the 4A limit for 1.8V rail which won't work with correct speed. Must be 50 MHz, otherwise USB UART and some other interfaces won't work with correct speed.

We use P1V8_AUX to also supply the 3.3V for clock distribution circuit. 4-pole LC filter supplies clean 1.8V for clock distribution circuit.
is 600 to 1000ps, Si53340 is 650 to 1050ps IC1 and IC4 have well matched delays. Si53312 IC4 to avoid stubs.

Route Main_DCXO_C_P first to IC1 and then to Helper_DCXO_SDA

Helper_DCXO_SCL

Main_DCXO_SCL

CDR_PLL_CTRL

Main_DCXO_OE

Helper_DCXO_OE

1.10.2019
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* DQ bits swapping within a byte lane is allowed if write CRC is not used.

According to VU11147:
* DQ bus line swapping is allowed. A byte lane includes any signals associated with the aliased 4-bits of DQ, such as DQ, DQS, DQS_N, and DI signals.

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Source Location: https://www.cern.ch/project/ot-sb
Crate power cycle timer

These把控地址及信号必须在

DIOT crate.

This is a startup clock 
before main Si5341 is  
programmed.

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The diagram shows the pin assignments for the FPGA Bank 63 of the DI/OT System Board. It includes various signals such as DQS_P, DQS_N, DQ[0..15], ACT_N, CAS_N, RAS_N, CS_N, DQ[0..15], DQS_P[0..1], BA[0..1], CK_N, CK_P, ODT, CR, and others. The AC-biased clock input option is denoted as DQS_BIAS = TRUE. Exceptions for PMD and RST_N signals are noted. The pin assignment differs only on the exception of PMD and RST_N signals, which is connected instead to the FPGA.
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SLOTx.LVDS0 is clock capable and must be in same bank as SLOTx.LVDS1...7
SLOTx.LVDS8 is clock capable and must be in same bank as SLOTx.LVDS9...15

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Recommended capacitance given in UG583. Check pin 3.

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Recommended capacitance given in UG583.
**European Organization for Nuclear Research**

**CH-1211 Geneve 23 - Switzerland**

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European Organization for Nuclear Research
CH-1211 Genève 23... Group Skew Constraints
max length: 1017 ps
data/dm to DQS: +-10 ps
dqs_p and dqs_n: 2 ps
CK to dqs: -149 to 1796 ps

* Address, Command and Control Skew Constraints
  max length: 1339 ps
  address/command/control to CK: +-8 ps

* Data Group Skew Constraints
  max length: 1017 ps
  differential DQS: =0 ps
  dqs_p and dqs_n: =2 ps
  CK to dqs: -149 to 1796 ps

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**Silkscreen or top copper for a DI/OT System Board PCB or other product**

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CH-1211 Genève 23 ...
4.7uF caps in the proximity of the IC which gives them low impedance contact with power plane that supplies the IC

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Satisfactory quality and fitness for a particular purpose.

Rule 5.49: The differential length mismatch on each differential clock pair shall be 1.2 ps.
Rule 5.43: The differential length mismatch on each differential data pair shall be 1 ps.
Rule 5.22: Clock traces shall provide a differential impedance of 100 Ω for FMCx_CLK0M2C and FMCx_CLK0C2M pairs.
Recommendation 5.3: When signals are routed differentially each pair should provide a differential impedance of 100 Ω.
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**DIOT System Board**

**CPCIS Connectors P1-P3**

Rx/Tx lines are swapped on the backplane

**ETH_A - ETH_B, ETH_C - ETH_D lines are swapped on the backplane**

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**P1 connector**

---

**P2 connector**

---

**P3 connector**

---
I2C MUX
PCA9548APW 1110000 = 0x70

MUX outputs:
MUX
IFPS5404/SMEMRFBE 7-bit I2C address: 0x14; 7-bit PMBUS: 0x44

MUX
LM75 - IC36: 0x48
LM75 - IC39: 0x49
LM75 - IC40: 0x4A

MUX
SFP EEPROM 0x50
SFP DDMII 0x51

Keep the switch in reset state until P3V3 wakes up to prevent from blocking power management I2C bus.
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

The P5V0_MP (therefore also P3V3_MP) are delivered from DI/OT backplane, thus always available.

For external programming

The supply line is 1.2V, allowing FLASH, FPGA and FPGA. It's 4A worst case.

Route differentially

Please consult UM before routing

https://www.infineon.com/dgdl/Infineon-UG-IRSP5401Demoboard-UM-v01_02-EN.pdf?fileId=5546d4625e37f35a015e37f7da400002

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Source location: https://www.ohwr.org/project/diot-sb-zu
C431 is recommended to be NP0. But 220nF, 25V X7R is good enough.

Power supply: Buck2

C431 is recommended to be NP0. But 220nF, 25V X7R is good enough.

Please consult UM before using https://www.infineon.com/dgdl/Infineon-UG-IRSP5401Demoboard-UM-v01_02-EN.pdf?fileId=5546d4625e37f35a015e37f7da400002

Power sequencing:
P2V5 then MGT_0V9, MGT_1V2

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power-supply-3.SchDoc

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2V5 rail supplies only DDR Vpp so 300mA is enough.