MTCA 4.1 for Low-Level RF (LLRF) distribution with White Rabbit
MTCA Equipment (1)

- Crate: 12 slots, made by Schroff/Pentair.
- MCH: provides crate management and PCIe/Ethernet backplane connectivity
- AMC: data acquisition/processing. E.g. SIS8300-KU board
  - 10 16-bit ADC channels @ 125 MHz, 1x16-bit DAC @ 500 MHz
  - Built-in White Rabbit support
MTCA Equipment (2)

- RF Backplane: standardized additional backplane for low-noise RF signals (e.g. clocks)

- uRTM: analog signal processing. Connected to one AMC and RF backplane E.g. DS8VM1 RTM Module:
  - Analog front-end for the ADCs
  - Vector modulator/upconverter for the DACs.
Overview of the WR LLRF crate
Clocks and RF distribution via RF backplane (1)

- RF backplane distribute RF signals and Clock signals using a star topology. eRTM15 is the center of the star.
- RF signals
  - Each uRTM receive LO, REF and CAL signals at 12 dBm (2 Vpp @ 50 ohm)
  - Total: 27 RF signals (WR eRTM15 provide only LO and REF!)
- Clock signals
  - Each uRTM (and eRTM13-14) receives two dedicated differential clock signals (CLKA and CLKB)
  - Total: 22 clock signals
Clocks and RF distribution via RF backplane (2)

- SIS8300

- eRTM 15

- e.g. Slot #4
Data distribution via RF backplane (1)

- Not much to say
- No data connectivity from (to) eRTM15 to (from) eRTM13-14 and uRTMs

![Diagram of data distribution via RF backplane (1)]
Data distribution via RF backplane (1)

- Not much to say
- No data connectivity from (to) eRTM15 to (from) eRTM13-14 and uRTMs
- Data connectivity from eRTMs to MCH-RTM (star topology)
Data distribution via RF backplane (1)

- Not much to say
- No data connectivity from (to) eRTM15 to (from) eRTM13-14 and uRTMs
- Data connectivity from eRTMs to MCH-RTM (star topology), but
  - Supported only by MCH-RTM-FPGA-BM, very constrained solution
  - we have MCH-RTM-BM (without FPGA)
Data distribution via RF backplane (2)

- Data distribution required to synchronize AMC boards (e.g. SIS8300)
  - 1-PPS (one-off, after cold start-up)
  - UTC (one-off, after cold start-up)
- AMC synchronization is not officially supported by eRTM15
- On-going: AMC synchronization via SIS8300’s optical interface (with WR)
  - in the future by Creotech WR MCH?
- BE/RF would like to not have WR on future AMC boards. What if WR-MCH is not commercially available?
  - 1-PPS synchronization can be done via AC-coupled clocks modulation
    - **Mandatory requirements**: No PLLs in the clock path from eRTM15 to AMC’s FPGA, AMC must have an FPGA
    - Hardware support in eRTM15 already present
  - UTC via network (e.g. NTP), as it’s not a time critical task once 1-PPS is recovered
Slot #14: WR Main Board

- Helper VCXO & PLL
- Main VCTCXO
- PLL / clock mux
- Power & Management
- Board-to-board connector
- Kintex-7 WR PTP Core
- GTX x2
- RF board control logic
- USB
- PLL
- 10MHz IN
- PPS IN
- WR CLK OUT
- PPS OUT
- SFP 2
- SFP 1

Slot #15: RF Board

- HQCD-060 Cable QSH/QTH 120 pins

This board requires a WR Main Board to operate correctly.

The connector is designed to support up to 3 DDS.
Specifications

❖ Clock signals, 1-PPS aligned, LVPECL standard:
  ❏ 12x CLKA operating at 125, 250 or 500 MHz
  ❏ 12x CLKB operating at 125, 250 or 500 MHz
  ❏ Other custom frequencies might be generable (i.e. 10, 100, ... MHz)
  ❏ Phase noise better than $-120 \text{ dBc/Hz @ 1 kHz (250 MHz carrier)}$
❖ RF signals, phase aligned (and resettable) in a (user selectable) arbitrary WR clock cycle
  ❏ 11x LO channels at 12 dBm (from 10 MHz to 250 MHz)
  ❏ 11x REF channels at 12 dBm (from 10 MHz to 250 MHz)
  ❏ Phase noise better than $-120 \text{ dBc/Hz @ 1 kHz (223.5 MHz carrier)}$
  ❏ RF power detectors on all channels
❖ Temperature sensors on RF stage, OCXO and power
❖ Current sensor on OCXO to monitor power consumption
❖ MTCA.4 management by STM32 microcontroller
  ❏ it can run FreeRTOS
❖ Kintex-7 FPGA on eRTM14, to use GTX transceivers
❖ Unique IDs
  ❏ Two MAC address on eRTM14 for Ethernet interfaces, one EUI-48 for storage
  ❏ One EUI-48 on eRTM15 for storage