Diffential trace with 100 ohm differential impedance.

LTC6950 require high slew rate signals to achieve for a phase noise at 1 kHz offset. The CE_PLL transformer boosts the input signal as much symmetric as possible. Layout: keep the two traces above placed near LTC6950.

100nF capacitors shall be placed near LTC6950, one per pin (VP). Avoid sharing 100nF capacitors for multiple pins to prevent cross talk. 100nF on opposite side.

*100nF capacitors shall be placed near LTC6950, one per pin (VP). Avoid sharing 100nF capacitors for multiple pins to prevent cross talk. 100nF on opposite side.

PLL control

PLL CONTROL

LVDPLL outputs are internally biased.

Note for layout outputs can be equipped for improved routing. Do not change polarity.

PLL

Used for clock synthesis

VCO PLL outputs are internally biased.

100nF capacitors shall be placed near LTC6950, one per pin (VP). Avoid sharing 100nF capacitors for multiple pins to prevent cross talk. 100nF on opposite side.

*100nF capacitors shall be placed near LTC6950, one per pin (VP). Avoid sharing 100nF capacitors for multiple pins to prevent cross talk. 100nF on opposite side.

LTDPLL control

LTDPLL CONTROL

The VIP support an additional LTC6930 used as clock distribution (CK, DISTR). The additional LTC6930 can be used for further asynchronous conversion using LTC6950 to synthesizer frequencies up to 900 MHz.

The VIP support an additional LTC6930 used as clock distribution (CK, DISTR). The additional LTC6930 can be used for further asynchronous conversion using LTC6950 to synthesizer frequencies up to 900 MHz.
Matching to be adjusted with layout. 5.6 pF capacitor accounts also for PCB capacitance.

Inductance should be 20 nH

Put ufl for network analyzer
SPS200 require two clocks, with the following requirements:

- The two clocks must be aligned.
- The clocks must not be skewed.
- The clocks must not have any differential delay.

For detailed information, refer to the PDS (presented by X).
RF Power Detector
Temperature sensors

OCXO Temperature sensors.
One near package, one under OCXO
Addresses: 0x4E, 0x4F

Power supplies
Address: 0x40

LO RF amplifier chain
Address: 0x41

REF RF amplifier chain
Address: 0x92

Temperature sensor
SDA TEMP SDA
SCL TEMP_SCL

C285 100nF
GND

MP3V3

IC38
SDA TEMP_SDA
SCL TEMP_SCL
ADD0 °C
ADD1
V+
GND

MP3V3

IC39
SDA TEMP_SDA
SCL TEMP_SCL
ADD0 °C
ADD1
V+
GND

MP3V3

IC40
SDA TEMP_SDA
SCL TEMP_SCL
ADD0 °C
ADD1
V+
GND

MP3V3

IC41
SDA TEMP_SDA
SCL TEMP_SCL
ADD0 °C
ADD1
V+
GND

MP3V3

IC42
SDA TEMP_SDA
SCL TEMP_SCL
ADD0 °C
ADD1
V+
GND

Project/Equipment
WR MTCA.4 High End Timing Receiver - RF Board (eRTM15)

Document
EDAXXXXX-VX-X

Designer: M. Rizzi
Drawn by: M. Rizzi
Check by: I. Wnukowski
Last Mod: 6/15/2018
File: temp_monitor.SchDoc
Print Date: 6/26/2018 5:21:03 PM
Sheet: 11 of 1
Note for layout: AIN pin swapping allowed
CLK_A and CLK_B outputs can be between 31.25 MHz and 500 MHz. Default config is:
CLK_A: 125 MHz (ADC clocks)
CLK_B: 250 MHz (DAC clocks)

Warning:
50 ohms and 100 ohms directives to be adjusted accordingly with substrate
NAT RF backplane distributes a RF signal to MTCA_PP12V, MTCA_MP3V3, or MTCA_PP12V. This signal is not reserved. Three lines are reserved for future use (2015).

**MTCA-1** standard requires the use of 50 ohm or 50 ohm between IPMB and MTCA-MCH backplane. Therefore a 50 ohm circuit on the backplane is all that is required for the recommended. Especially a 50 ohm or 50 ohm is not recommended. A circuit has a conductive path to the signal. This reduces the signal and could result in errors to the AMC and JTM’s (the same is true for our components). This should not be used by adding a Clerk. I tried all to get that statement out of the spec, but someone adds to you component in this case. Loops are in that spec. and you have to decide how you will handle it on your board.

**SOLUTIONS** for JTM15: 1) use TPS2412 (+ power mosfet) for power or-ing 2) manual selection using 1R resistors.

Now it is inside that spec. and you have to decide how you will handle it on your board as we do on our MTCA PMs and MTCA-Rear PM. Therefore a OR-ing circuit on the Backplane or eRTM is used.

NAT ANSWER: We are using the same OR-ing circuit on the NAT-MCH-RTM to switch the power of the eRTM15 between the RFU and eRTM15.

**Adopted solution**: 2, to save layout area.

Project Equipment: WB MTCA-4 High End Timing Receiver - RF Board (eRTM15)

Document: MTCA-4 High End Timing Receiver - RF Board (eRTM15)
The cable is Samtec HQCD-060.

The differential pairs must be surrounded by grounded or single-ended lines with low-impedance termination, as defined in the SLEW, EMI guidelines.

Currently, J1B manages all the DDSs. Pin assignments on J1A are arbitrary, can be changed during layout (accordingly with RF board), with the exception of pins 1 to 9 and PRESENCE signals, which are fixed.

Reserved for CALIBRATION DDS.

The differential pairs must be surrounded by grounded or single-ended lines with low-impedance termination, as defined in the SLEW, EMI guidelines.

Reserved for CALIBRATION DDS.