The Node board can operate in stand-alone mode (i.e. without an RF board) or with an RF board.

If an RF board is plugged, the Node board is using the internal timebase (provided by a VCTCXO) as Main Oscillator.

In standalone mode, the board uses the internal timebase (provided by a VCTCXO) as Main Oscillator.

If an RF board is plugged, the Node board is using the internal timebase (provided by a VCTCXO) as Main Oscillator.

The CLK_REF signal is a clean clock operating at 125 MHz. If an RF board is plugged, CLK_REF is used to synthesize the WR clock as well as the GTX clock.

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Virtex-7 devices. Spartan-7 and Artix-7 devices do not have package capacitors.

https://www.xilinx.com/support/documentation/user_guides/ug483_7Series_PCB.pdf
TO BE EVALUATED: use some of the unused transceivers for high-speed bidirectional or front-panel data transfer.

Layout note: make sure MGT_R_REF and MGT_R_REF_VTT traces between R87 and BGA pads are of equal length.

Bank 16 pin assignment: the pins with the "filled" symbol are grounded. All pins with the充裕 are the high-speed data lines (1.25 Gbps) for GTX calibration.

Digital Board (eRTM14)
FPGA Transceivers

European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland
Optional GTX calibration logic: the splitter can feed back 802.3q idle pattern back to the I/O pins of the FPGA where it is sampled by a DDMTD to precisely measure the latency introduced by the transceiver.

The series resistors R115 and R116 improve the LVPECL output impedance matching and attenuate the differential swing. The maximum differential swing declared in the FPGA datasheet (0.6Vpp MAX) can be exceed without damage, however to reduce cross-talks it is better to not use the full LVPECL swing (equal to 1.6Vpp). The attenuated swing is 0.8Vpp.

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62.5MHz Clock for the DMTD Phase Detector in FPGA (LVDS)

PLL Settings:
- AD9516-4
- Phase-locked loop
- 10/11
- Frequency: 62.5/125MHz
- Margin: 50 degrees
- PLL Settings:
  - PLLCS
  - PLLSDI
  - PLLSDO
  - PLL_RESET
  - PLL_LOCK
  - PLL_SYNC
  - PLL_STAT
  - PLL_RCLK

60/120MHz Clock for the DMTD

Synchronous clock for the eRTM15. This clock can be used for the eRTM15, TRSM16, or DMTD. The PLL in the eRTM15 is used for the WR timebase.

During cold start-up, AD9516-4 is not initialized, therefore, there is no CLK_SYS signal. The FPGA uses CLK_SYS signal to perform the glitch-free clock switch-over after initialization.

To install clocking mode, the AD9516 uses CLK/main VCXO to synchronize the WR timebase using the internal clock dividers (internal VCO disabled).

During start-up, the BUFGMUX primitive is used to perform the glitch-free clock switch-over after initialization.
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Digital Board (eRTM14)
Front Panel LEDs
The ID is a valid EUI-48, aka IEEE MAC address. The revision number of the board can be stored in the NV memory, the unique ID is provided by an external chip. Boot0 = GND: boot from main Flash.

Note for layout: keep FLASH* traces to STM32 very short, to avoid stubs. Avoid stubs to STM32 very short. To avoid stubs to STM32 very short. To avoid stubs.