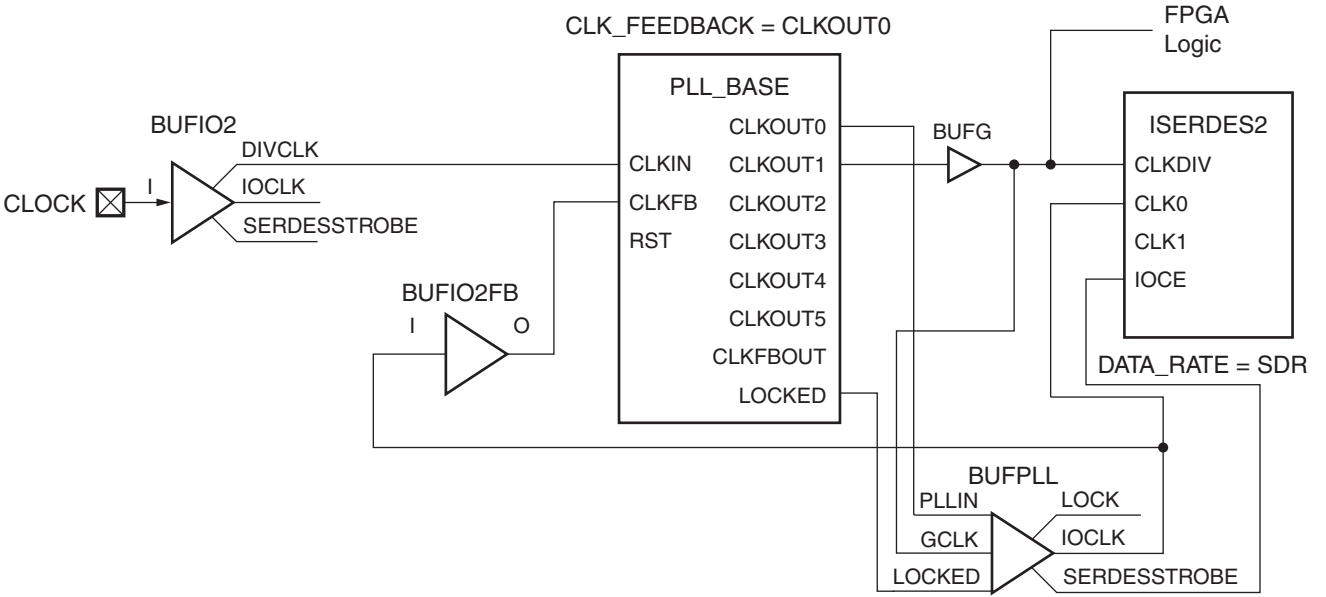
CLK_FEEDBACK = CLKOUT0
FPGA
Logic
PLL_BASE
BUFIO2
DIVCLK
CLOCK
I
IOCLK
SERDESSTROBE
CLKIN
CLKFB
RST
CLKOUT0
CLKOUT1
CLKOUT2
CLKOUT3
CLKOUT4
CLKOUT5
CLKFBOUT
LOCKED
BUFG
ISERDES2
CLKDIV
CLK0
CLK1
IOCE
BUFIO2FB
I
O
DATA_RATE = SDR
BUFPLL
PLLIN
LOCK
GCLK
IOCLK
LOCKED
SERDESSTROBE
UG382_c1_10_121709