Evaluation of Initial Proposal for FmcAdc100M14b4ch_a 27/11/09
by *The Analogue Anarchist*

Choice of components

Input Buffer THS4631

A reasonable choice (amongst the alternatives), but does have some issues that need to be looked at.

If used as a unity gain input buffer, it must have an input and output capability of ±10.24 V.
The data sheet indicates that this is outside the Input Common Mode range if the THS4631 is powered from ±12V as is suggested in the documentation. If powered from ±15V things should be OK over the 0C to 70C temperature range. This does complicate the Power Supplies strategy a bit.

Input Clamp Protection is a highly desired feature on the inputs. However I think you have been misled by the data sheet (I agree it's written in a stupid way). Regardless of how one can interpret Vs, Vs+, Vs-, ±Vs and so on, I'm 100% sure they are trying to say that the input pins cannot go outside the Power Supply rails ie +/- 15V in this case. If you connect clamp diodes directly to these supply rails then the Input can still go outside of them by a diode drop. This should be OK, but a more sophisticated clamp would have clamp diodes at, say ±12V to be sure. A series input resistor is also required between the module input and the clamped buffer input to increase the source impedance seen by the clamp diodes (they can themselves be blown up by input overloads). 50 ohms would be fine, and not really change the SNR or bandwidth of the system. The choice of diode is also important to not create too much harmonic distortion on the signal to non-linear capacitance effects.

Harmonic Distortion from the buffer itself may be an issue at higher Fullscale inputs (±10.24 V). However there are no curves for G = 1 behaviour. I imagine in Unity Gain Buffer mode the THD should be a bit better rather than worse for G = 2 where data is specified.

The Input Equivalent Noise voltage of 7nV / √Hz is too high for the desired system performance. This will be discussed in the System Issues section.

PGA THS7002

Again, a reasonable choice (given the lack of alternatives), BUT…….

Harmonic Distortion is not stated at 25MHz, but id does seem to be heading skywards in an alarming fashion above 10MHz.

The Input Equivalent Noise voltage of 10nV / √Hz adds to the problem of the Input Buffer. To be discussed below.

Crosstalk between PGA sections is specified at -77dB @ 1MHz. This is somewhat vague because we don't know how it's really measured – specifically when the two PGA channels are in very different

gain settings. Could have a “shift” of 42dB in the interpretation. I understand that space is a crucial issue in this design, but generally using dual or quadruple components is not a good idea

Diff Amp THS4524

This device would be OK for an acquisition system with lower performance, but it it definitely NOT the correct one here. A key performance parameter for any of these Diff Amps is the Harmonic Distortion at higher frequencies, and this one doesn’t make the grade. The HD at 25MHz is pretty atrocious – worse than -50dB for 2^{nd} and almost -30dB for 3^{rd}. It is possible to find another Diff Amp with a better performance.

ADC LTC2174

Looks like a pretty decent ADC with good analogue specs. The ADC is the one part of the system where I would say it’s OK to use a “Multi-Device” package, because it drastically simplifies the super-critical ADC Clock part of the layout.

Schematic Issues

I did the previous write up before I had the schematic, but now I have it I can make a few comments.

Input Buffer

As suggested before – change supplies to ±15V and add clamp diodes to ±12V directly at the THS4631 +Ve input. Suggest BAR66 diodes because they have a much lower cap than the BAV99s.
Input termination resistors (2 x 100 ohms) must be 1W devices.

Diff Amp

Running from a single +5V supply with an Output Common Mode of 0.9V for the ADC is not a good idea. I know the data sheet implies that this will (may) work, but it's right on the hairy edge. In any case the HD performance of the THS4524 is insufficient. Suggest LMH6552 running from ±5V. Lower noise and much lower distortion. LMH6552 and LMH6551 OK – THD not quite as good but lower power.

ADC

I don't think OVDD can be connected to +2.5V. - Max voltage is 2V….

LT1931

This regulator with coupled inductor seems to be hooked up in a very strange way. If it was meant to be a CUK converter architecture, it isn't ! I can highly recommend the CUK converter for this sort of positive to negative conversion because it injects much lower noise into its input and output than other types. See LT1931 data sheet for details.

System Issues

Full Scale Ranges

There seems to be an inconsistency in the specified FS ranges. Full-scale are ±40mV to ±10.24V in 6dB steps. This makes a 48dB gain range in 9 different Full-scales. The PGA only provides 42dB in 8 FS ranges. There is a 2:1 Input Range Adjustment on the ADC, but this is common to all channels with a single control. So this then requires a FS spec change, or a hardware architecture change.

Anti-Aliasing Filter.

I didn't see any on the schematic. They must be put just in front of the ADC. Putting them anywhere else would drastically decrease the channel SNR.

Channel SNR

As mentioned above, there is a channel SNR issue. We can ignore resistor noise and opamp current noise as they do not really change anything in this case. Also the first two Frontend stages dominate the result, so we only need to look at them. The key numbers are:

Input Buffer: Input Signal = ±40mV, Signal Gain = 1, EIN = 7nV / √Hz, , Noise Gain = 1
- which gives Output Signal = ±40mV,. EON = 7nV / √Hz (Equivalent Output Noise)

Combining the 7nV / √Hz with the 10nV / √Hz EIN of the PGA (when it's in 20dB gain) gives
PGA EIN = 12.2nV / √Hz, In Addition: Signal Gain = 10, Noise Gain = 10.

So PGA Output Signal = ±400mV, EON = 122nV / √Hz

The Diff Amp stage will add some more noise, but not anything significant if done properly, so we can calculate the SNR here as an "Upper Limit Value"

For a 25MHz BW, VNrms = 122nV x √25e6 = **610 uV RMS**

Max RMS Signal Power = 400mV / 1.41 = **284mV RMS**.

Comparing Signal Power to Noise Power gives an **SNR of 53.4 dB**. .

This would normally be considered pretty bad (understatement !) for a 14 bit system.

Harmonic Distortion

It's likely that the THD performance above 10MHz will be below the normal expected level for a 14 bit system. (Meaning that it is quite a bit worse than the ADC on its own)

Trigger

There are no details on this part, except the phrase “trigger the ADC”. So what does this mean ?
For these types of ADC the Clock must be running all the time and stable – hence the ADC is always producing data. Normally the trigger event is used to STOP the data memorisation process after the ADC, either immediately (Trigger at End of Acquired Trace case) or some number of data events after the trigger event (Trigger Occurs somewhere in Acquired Trace) or Acquired Trace occurs some delay time after trgger event (Delayed Acquisition). The easiest place to do this is the De-Serialiser component (probably an FPGA) receiving the ADC continuous data. Some jitter in the trigger event is generally not so important, unless you are going to use a Time Interpolator to place the trigger point within a clock period, or synchronise acquired data from multiple modules.

Clock

There are even fewer details about the Clock Source. A clean clock is vital to having a good acquisition system. It IS part of the analogue stuff, not the digital stuff. If you give some info I can look at this.

Multi Part Packages.

Multi Part packages can have hidden surprises in terms of signal crosstalk etc. It also means in this case that none of the channels will have exactly the same layout, which could give them different behaviours. In fact it guarantees that the layout of some of the analogue stuff will be non-optimal. Also any desired saving in package area will be compensated by extra track lengths, so it generally doesn’t lead to a more compact layouts. We’re not talking about Digital Layout with the Bus Drivers being 4 bits wide or 8 bits wide. As I said though – the “Multi-ADC” is a special case, being right at the end of the analogue chain.

Conclusion

If you really want an acquisition system that comes significantly closer to a 14 bit performance, with these same Full scales and bandwidths, some work is needed on the FE architecture.

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