FmcAdc100M14b4ch_a

Shortened Spec

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Abstract

FmcAdc100M14b4ch_a is a 4 channel 14 bit 100MS/s ADC board with internal/external

triggering

in FMC (FPGA Mezzanine Card) standard

1. **Project requirements**

- Electrical and mechanical characteristics fit to FMC standard
- Sample rate up to 100MS/s
- Resolution 16bit
- 4 channels, DC coupled, fixed input impedance: high, or 50Ω
- Trigger: internal, or external (logic levels)
- Clock: internal
- Digitally controlled gain – set independently for each channel. Sensitivity have to cover the range form +/- 40mV for full scale to +/- 10.24V for full scale
- 25MHz analog bandwidth, antialiasing LC filter included

2. **ADC's performance**

- Integral nonlinearity: typ. +/-1 LSB, max. +/-3.75 LSB
- Differential nonlinearity: typ. +/- 0.3 LSB, max. +/-0.9 LSB
- SNR 73.4 @ 5MHz
- Offset +/- 3mV

Shown above parameters comes from LTC2174 application note. Its performance is common for many ADCs available in the market. Overall card performance will be worse because of the noise and the nonlinearity of the analog stage foregoing the ADC.

3. **General description**

FmcAdc100M14b4ch_a is a 4 channel 100MSPS 14 bit ADC card in FMC (FPGA Mezzanine Card) standard. Gain of each channel can be set in the range of 40mV/scale to 10.24V/scale in 256 steps independently. ADC can be triggered both internally and externally.

4. **Analog inputs**

ADC board has four DC coupled high impedance or 50Ω inputs (impedance is fixed, chosen by using proper resistor). Inputs are protected against overload (caused by static electricity or attaching too high voltage – in the range of +/- 48V). Gain can be set independently for each channel.

5. **Trigger inputs**

Trigger input are single ended, dedicated to work with TTL/CMOS output driving 50Ω transmission line with load. 1V threshold voltage allow card to work with both 5V and 3.3V logic.