FmcAdc100M14b4ch_b

Technical Spec

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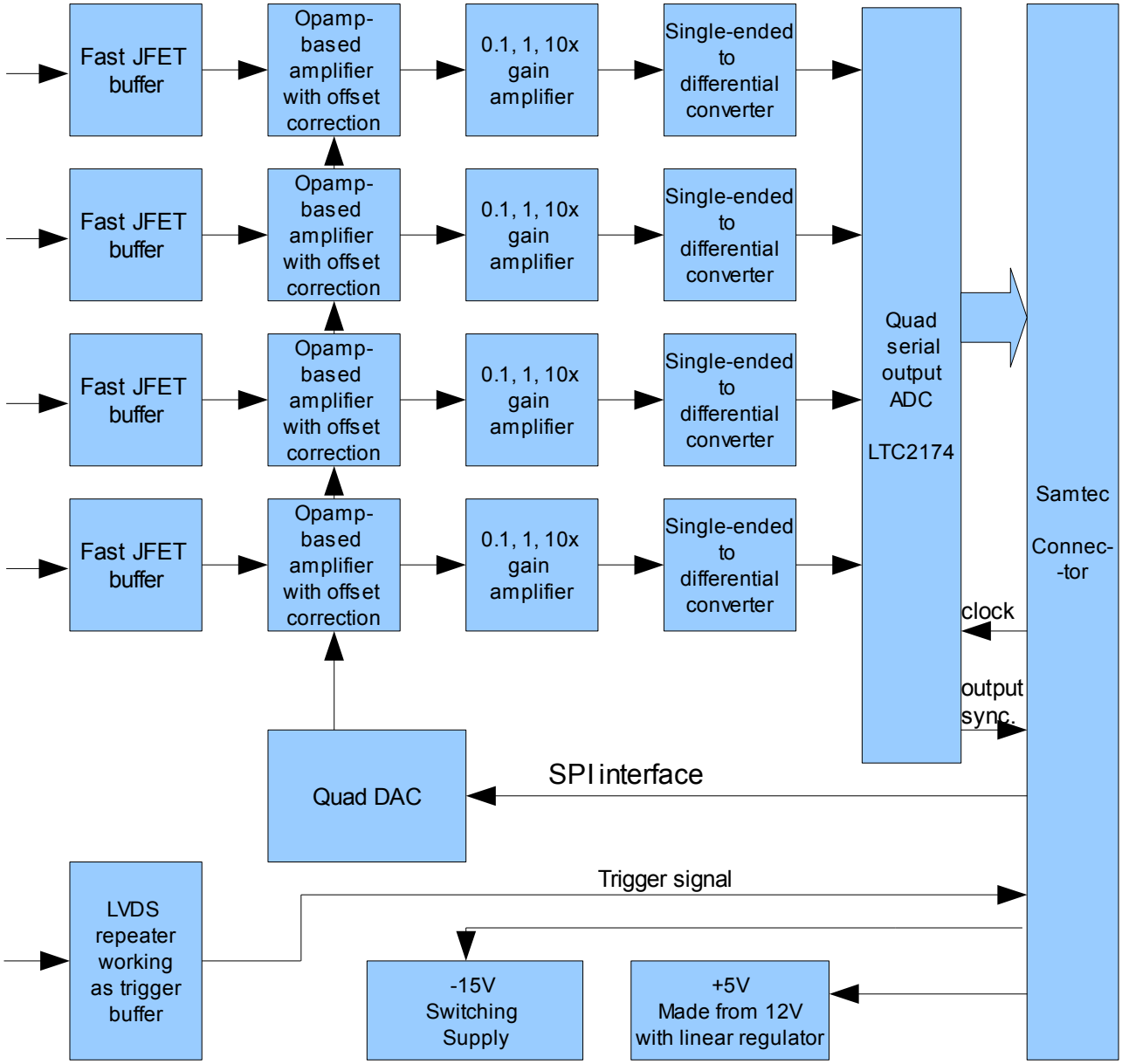
Abstract

FmcAdc100M14b4ch_b is a 4 channel 14 bit 100MS/s ADC board with internal/external triggering
in FMC (FPGA Mezzanine Card) standard

1. Block diagram



2. Description

- Fast JFET input opamp

Simple noninverting buffer with external overload protection. It was being looked for low noise bipolar amplifier, with small polarisation current. Internet research did not bring results (due to the bipolar amplifiers' large polarisation current), so it was decided to use JFET input opamp with awareness of it's larger noise level. Other important requirement is low THD factor.

JFET-based opamp is harder to break down by static electricity than opamp based on the CMOS technology. THS4631[1] type is fast enough, it is unity gain stable and can be powered from +/-12V, so no attenuator at the input is needed. Input is protected by two BAR66 diodes clamping to high signal to voltage lower (Zener diodes) than supply voltage.

- Opamp-based amplifier with offset correction

Operational amplifier in reversing configuration. Virtual ground is driven from the DAC. AD811 (with the noise level of 1.9nV/√Hz and THD of -70dBc@10MHz) will be sufficient.

- Jumper selectable gain amplifier.

Gain range is settable in three steps by changing jumper settings. Using dual jumpers allow motherboard to determine which input voltage range has been set. AD811[2] is valid choice for this application.

1 http://www.ti.com/lit/gpn/ths4631
2 http://www.analog.com/static/imported-files/data_sheets/AD811.pdf

- Anti-aliasing filter

  Simple LC Butterworth low-pass filter. Two pole filter doesn't have edges sharp enough, so 4-pole filter will be used. It will be terminated only at the end point to avoid unnecessary signal attenuating.

- Single-ended to differential converter

  LTC6404[3] is used here, because of it good noise factor and low distortion (1.8nV/√Hz, -90dBc@10MHz). Rail-to-rail input allows amplifier to work with single supply.

- ADC

  Reasons of choosing LTC2174[4]:

  - descent sampling speed (up to 105MSPS)
  - including four ADCs in one package
  - serial output interface – do not needs many pins to communicate with carrier board, low-pin-count connector can be used.

- Trigger receiver

  The MAX9180[5] is used here. This component is a LVDS repeater, but it can be used as single-ended to differential converter. It is fast enough (400Mbps) and it's added jitter is low.

3 http://cds.linear.com/docs/Datasheet/6406fc.pdf
4 http://cds.linear.com/docs/Datasheet/21754312f.pdf
5 http://datasheets.maxim-ic.com/en/ds/MAX9180.pdf

- Power supply

Power supply regulators needs to be stable, efficient, easy to use and being able to deliver proper current to the loading. Switching supply should work with high chopping frequency, therefore proper filtration is easier. Low noise LT1931[6] (CUK architecture) and LT3495[7] (boost) are used here.

A bit more attention has to be paid at the supply of ADC. This component needs 1.8V for analog and digital stage. FPGA testing boards are not fully compatible with the FMC standard, and VADJ (adjustable power supply) cannot be set – voltage is fixed to 2.5V. For make first-run simpler, it is decided to use additional LDO linear regulator, making 1.8V from 2.5V. Another advantage of this solution (even for target design) is no need of using level converter for communication with DAC (it "one" level voltage is at least 2V). LT1763[8] has been chosen.

6 http://cds.linear.com/docs/Datasheet/1931fa.pdf
7 http://cds.linear.com/docs/Datasheet/3495b1b1fa.pdf
8 http://cds.linear.com/docs/Datasheet/1763ff.pdf