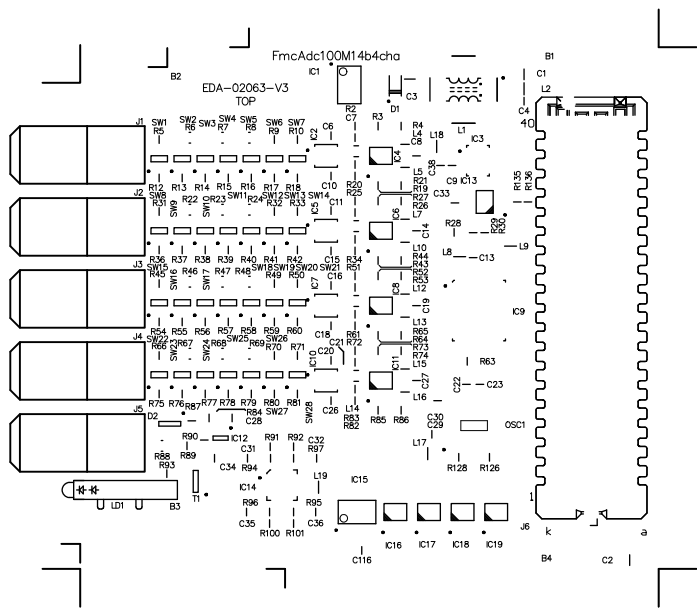


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Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

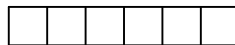
Print Date 24/06/2011 13:57:13

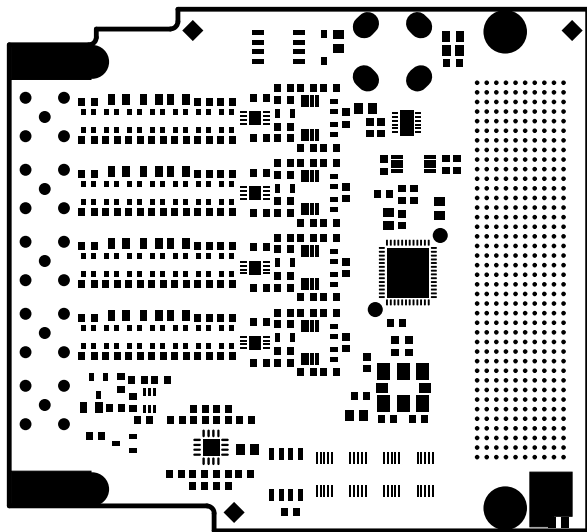


Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

Print Date 24/06/2011 13:57:14

Top Overlay

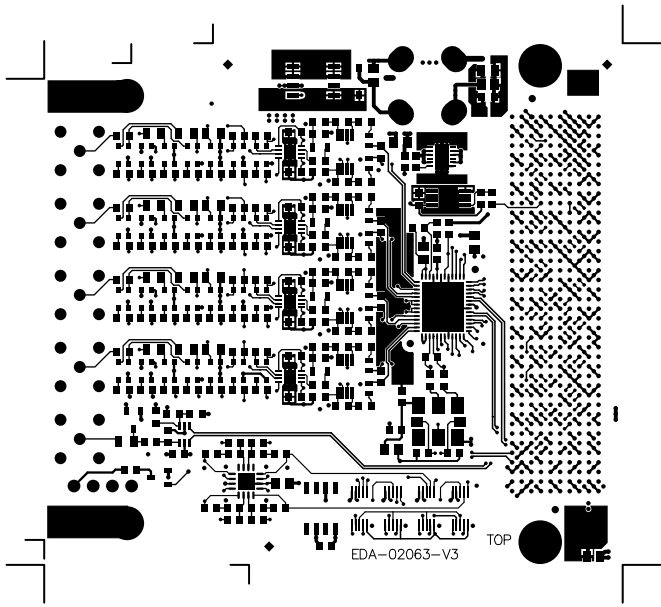




Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

Print Date 24/06/2011 13:57:15

Top Solder

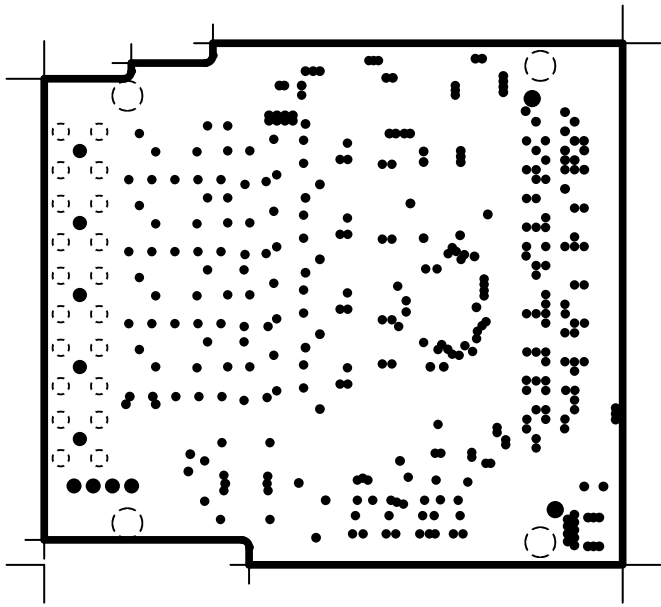


Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

Print Date 24/06/2011 13:57:14

Top Layer

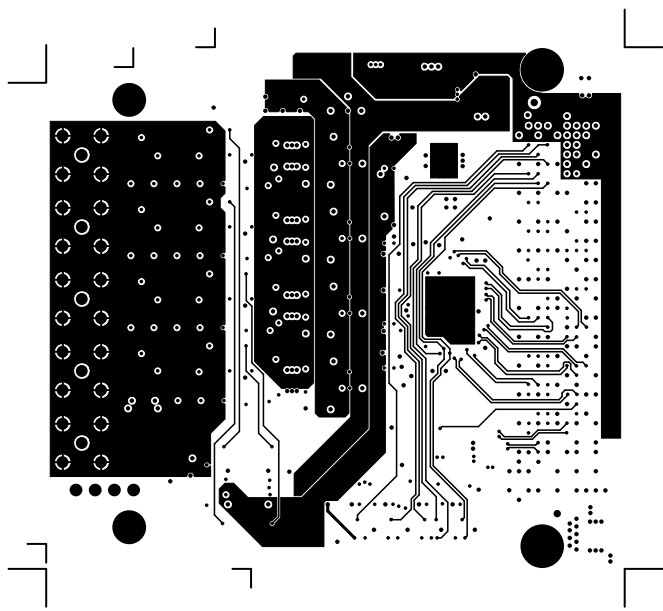
1					
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Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

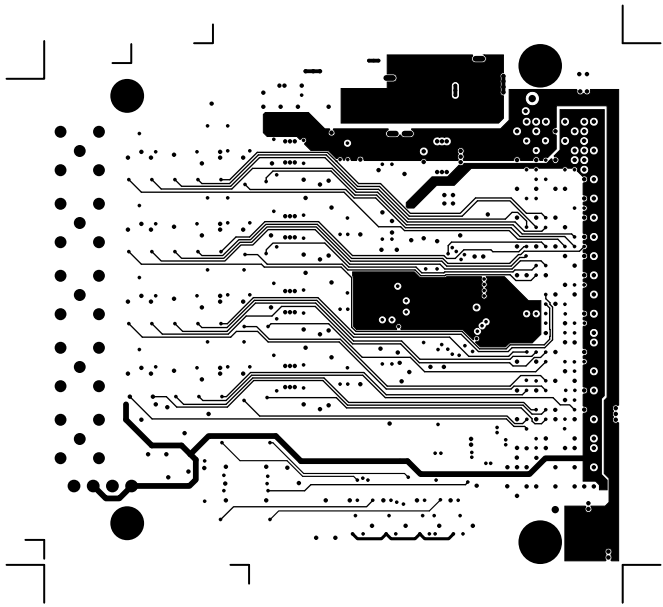
Print Date 24/06/2011 13:57:14

Plate 17 empty



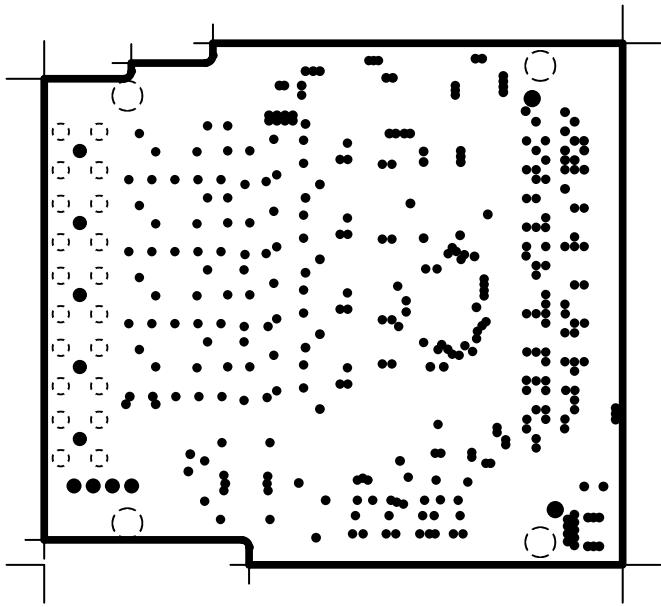
Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

Print Date 24/06/2011 13:57:14



Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

Print Date 24/06/2011 13:57:14

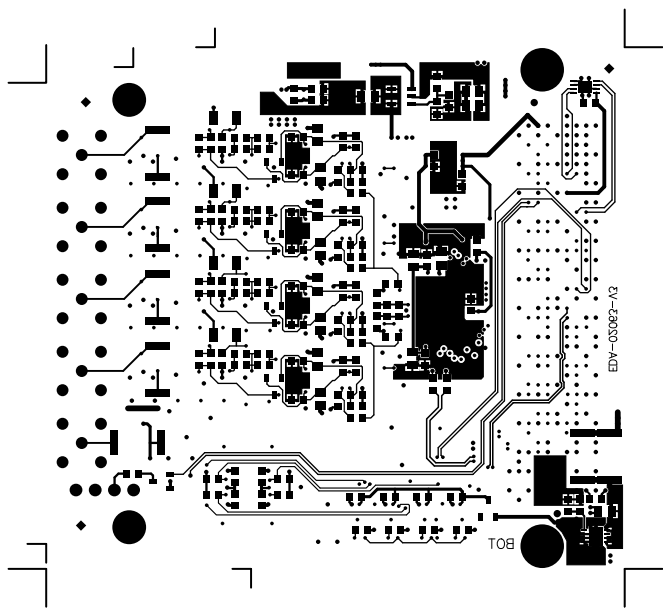


Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

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Plane L5 GND  
5

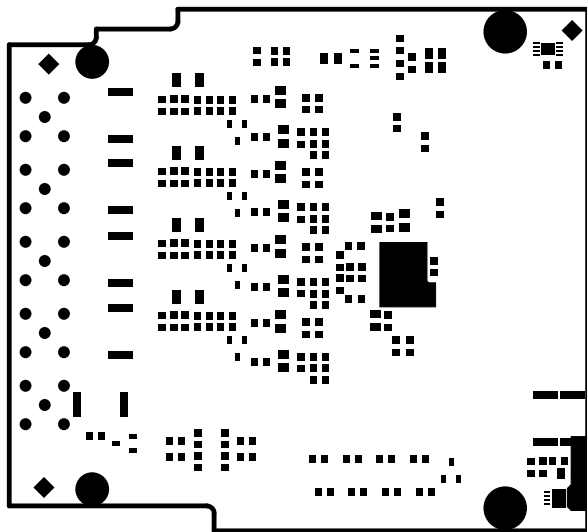




Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

Print Date 24/06/2011 13:57:14

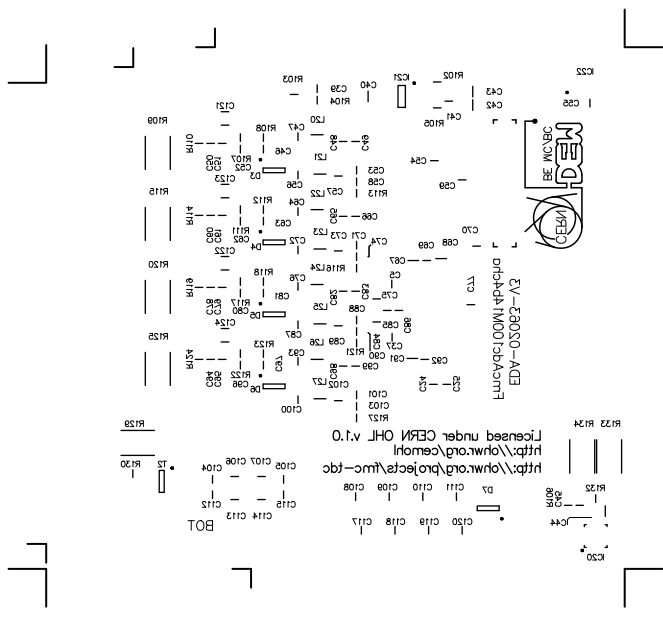
Bottom (top)



Number	EDA-02063-V3
Drawn By	CEGELEC NL
DATE	12-03-2010
MOD.	CEGELEC BC (24-06-2011)

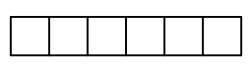
Print Date 24/06/2011 13:57:16

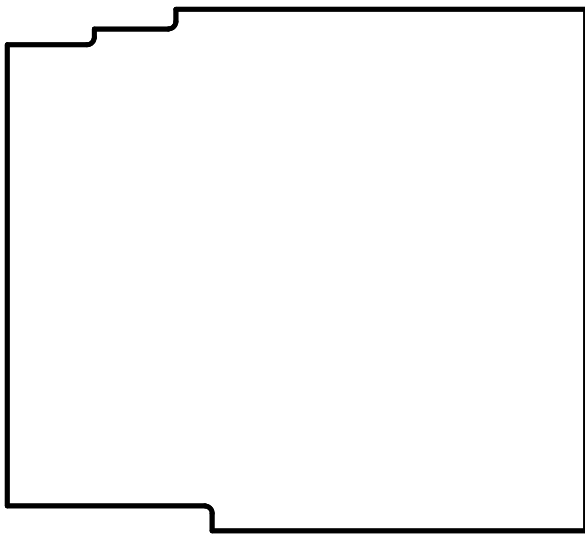
Bottom solder

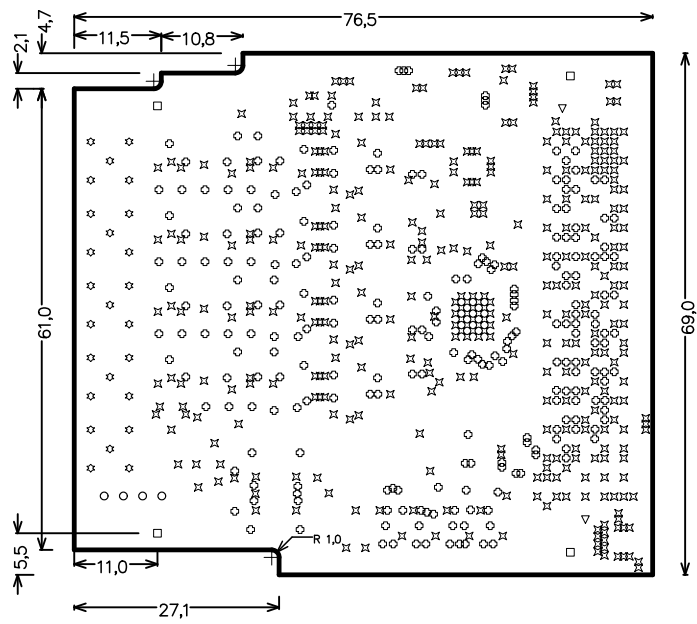


Number	EDA-02063-V3
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Bottom Overlay







Symbol	Hit Count	Tool Size	Plated	Hole Type
⊙	242	9.842mil (0.25mm)	PTH	Round
⊗	377	11.811mil (0.3mm)	PTH	Round
⊛	25	35.433mil (0.9mm)	PTH	Round
○	4	39.37mil (1mm)	PTH	Round
▽	2	51.181mil (1.3mm)	NPTH	Round
□	4	106.299mil (2.7mm)	PTH	Round
	654 Total			

Layer Stack Up Detail for: EDA-02063-V3\_pcb.PcbDoc

LAYER IDENTIFICATION	LINE WIDTH/GAP (mm)	FINISHED COPPER THICKNESS	CONTROLLED IMPEDANCE +/-10%	DIELECTRIC THICKNESS *CRITICAL
TOP LAYER	SIGNAL LAYER	0.208/0.127	35 um	50/*100 Ohms
LAYER 2	GND PLANE	-	35 um	-
LAYER 3	Signals	0.208/0.127	35 um	50/*100 Ohms
LAYER 4	Signals	-	35 um	xx Ohms
LAYER 5	GND PLANE	-	35 um	-
BOTTOM LAYER	SIGNAL LAYER	0.208/0.127	35 um	50/*100 Ohms
FINISHED BOARD THICKNESS +/-10%				1.36mm

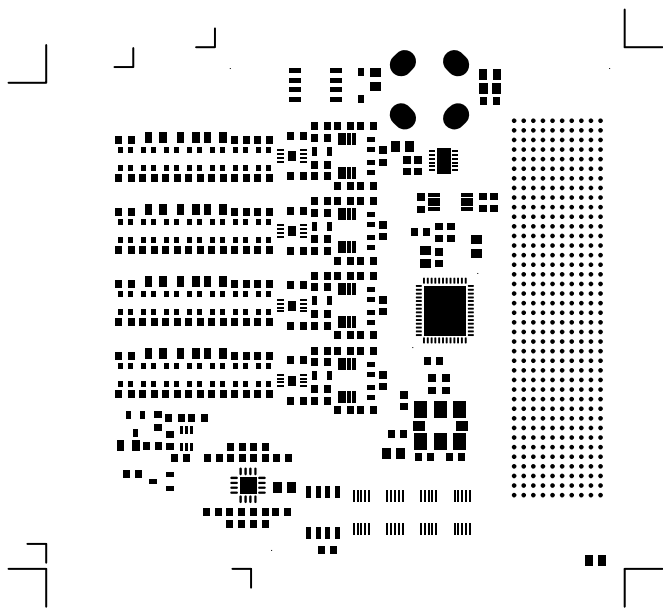
\*100 Ohms = Differential Impedance



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Components 360  
Pins 1403  
Vias 619  
Holes 654  
Nets 272

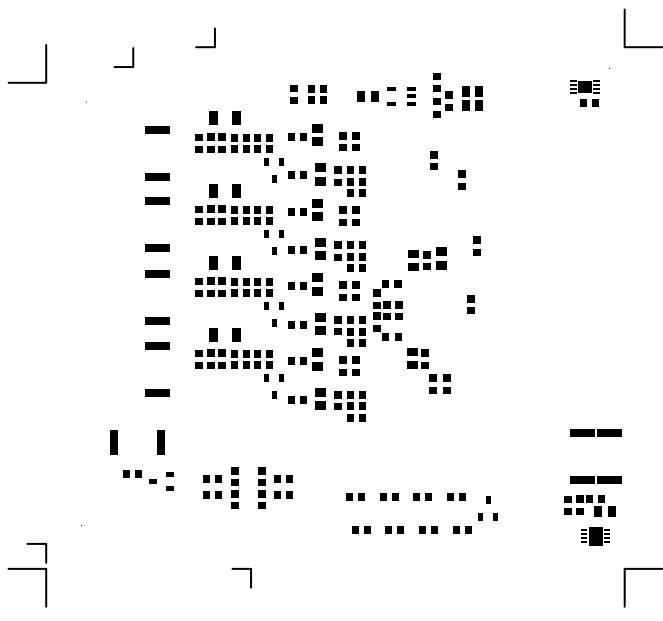


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Top Paste





Number	EDA-02063-V3
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Bottom Paste

