CNPEM
Brazilian Center for Research
in Energy and Materials

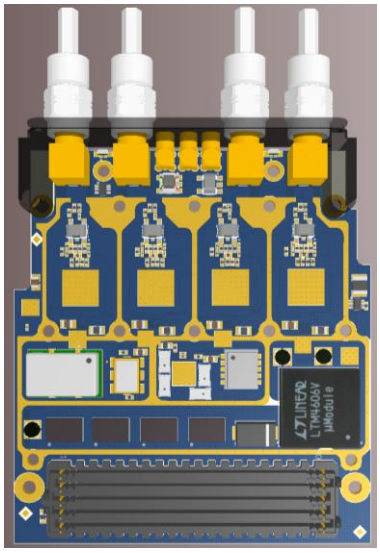
FMC-ADC-130MSps hardware manual

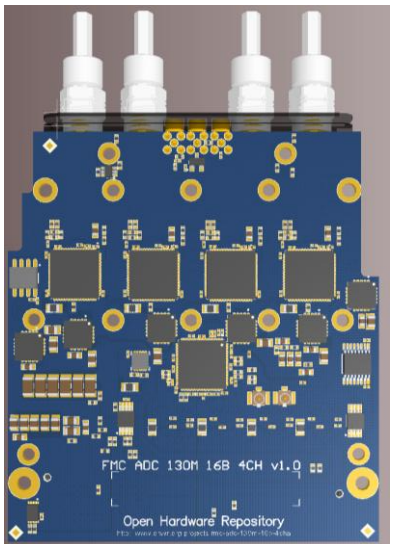
April 2014

Brazilian Synchrotron Light Laboratory
Beam Diagnostics Group (DIG)

Centro Nacional de Pesquisa em Energia e Materiais (CNPEM)
Laboratório Nacional de Luz Síncrotron (LNLS)
Rua Giuseppe Maximo Scolfaro, 10000, Polo II de Alta Tecnologia
Campinas, São Paulo, Brazil
CEP 13083-970 – Caixa Postal 6192

- Design reference name: FMC_ADC130M_v1, FMC_ADC130M_v2, FMC_ADC130M_v3
- Last production: Beam Diagnostics Group, Brazilian Synchrotron Light Source, 15 units, jan/2014.





Beam Diagnostics Group
Brazilian Synchrotron Light Laboratory
Tel.: +55 19 3512-5071
Email: dig@lnls.br

Date	Revision	Description	Authors
07/01/2015	0.1	Initial draft.	Rafael A. Baron,

Table of Contents

1. General information

- **About the manual:** This manual is intended to describe about the FMC_ADC130M_vX hardware designed for the BPM electronics of the Brazilian Synchrotron Light Source, Sirius Project. There are information about the specific schemes that are implemented on the board, about the devices chosen (when necessary), and about manufacturing process.
- **If some part of the text is important it will be noted with the signals that are described in what follows.**

Conventions

DANGER

Indicates that death or severe personal injury will result if proper precaution are not taken.

Warning

Indicates that death or severe personal injury may result if proper precautions are not taken.

Caution

Indicates that minor personal injury can result if proper precautions are not taken.

Notice

Indicates that damage to equipment can result if proper precautions are not taken.

Information

Indicates information that we think you should have read to save your time by avoiding common problems. Important suggestions that should be followed will also be marked with this sign.

2. Introduction

The FMC_ADC130Msps electronics is composed by one board based on the HPC (High Pin Count) FMC standard.

Follows the FMC_ADC130Msps specifications.

Table 1: Specifications of the FMC_ADC130Msps electronics[1].

Parameter	Value
ADC resolution	16 bits
Bandwidth (3dB)	20 – 500 MHz
Crosstalk @ 500 MHz	>40 dB
Full scale range	1.5 or 2.25 Volts p-p
ENOB @ 500 MHz, 0 dBm	9 bits
SFDR @ 500 MHz, 0 dBm	58 dBFS
SINAD @ 500 MHz, 0 dBm	58 dBFS
SNR @ 500 MHz, 0 dBm	73 dBFS
Noise Floor, 0 dBm input[2]	-123 dBFS

Temperature operation: -20 ºC to 50 ºC

2.1 Hardware Characteristics:

- Four ADC 130 Msps sampling channels
- Two clock sampling schemes, selectable between internal clock generation or external sampling clock[3].
- Passive clock distribution network for the external clock sampling scheme.
- Input reference for the internal clock generation. The internal clock generation is locked to the external reference and is based on COTS VCXO and PLL circuits.
- VCXO selectable between ultra low Phase Noise and lower pulling range or Low Phase Noise, higher pulling range.
- Input reference clock digitally selected between front panel MMCX connector or FMC connector.
- Low insertion loss Single Ended input RF stage. SMA connectors on the RF input channels
- Two on-board semiconductor-based temperature sensor.
- Output trigger signal via the MMCX connector
- UFL RF connector for ADC clock test probe

[1] All the measurements have been performed using a sampling clock of 115 MSps
[2] Noise Floor measured considering a 100k points FFT resulting in a process gain of $10.\log_{10}(M/2)$~47 dB
[3] The selection between internal or external clock generation is done before the manufacturing process. The clock signal path is selected by soldering capacitors in order to avoid additive Phase Noise.

2.2 Safety Instructions

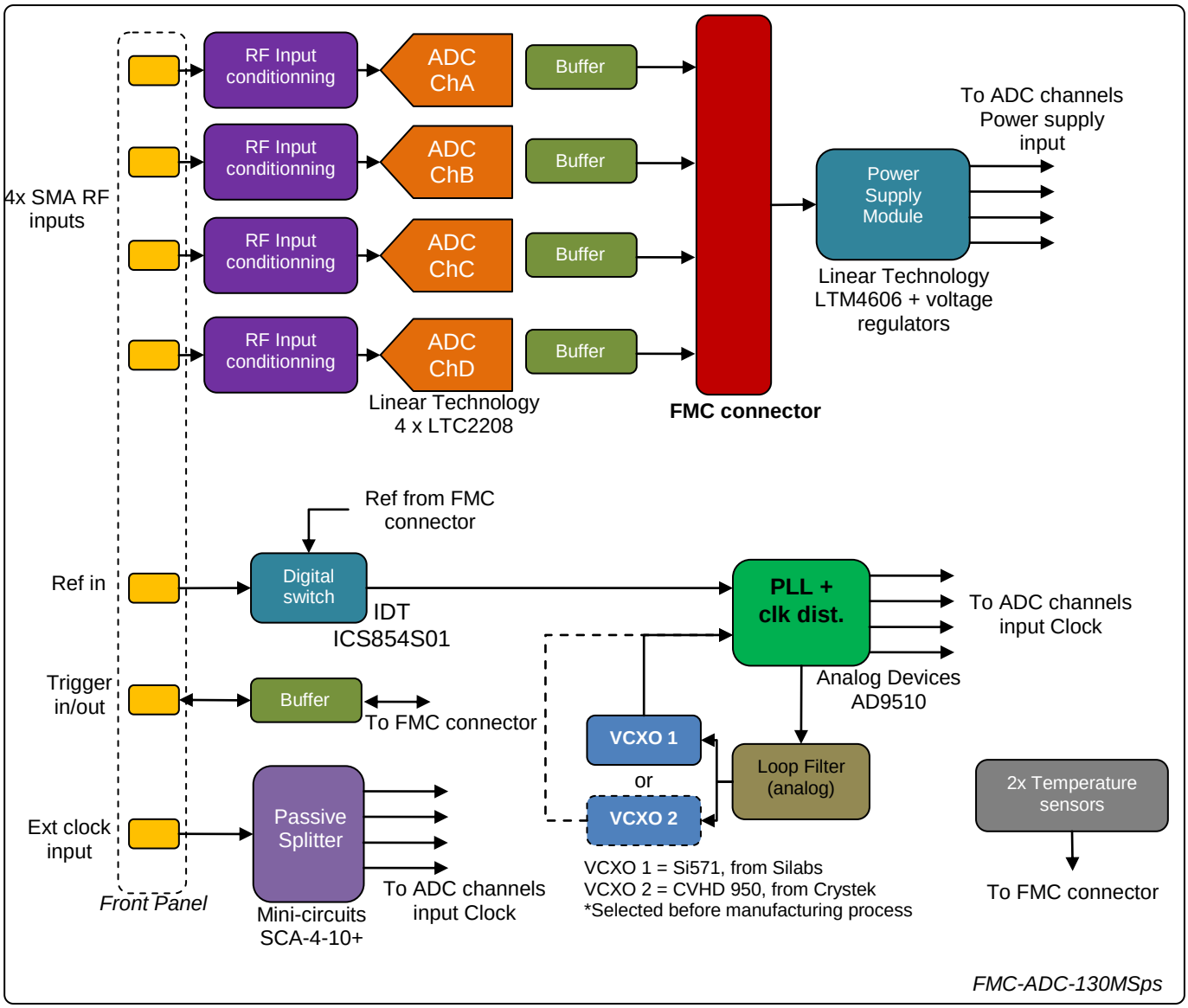
DANGER

Do not operate this electronics in potentially explosive atmosphere

3. Technical Overview

On this section it will be described about the hardware characteristics and detailed schematic description

3.1 Block Diagram



- Analog Loop Filter
  - The loop filter can be selected by soldering capacitors and resistors on the board.
- Digital Switch for reference selection
  - The reference can be selected between the MMCX connector on the front panel and the FMC connector.

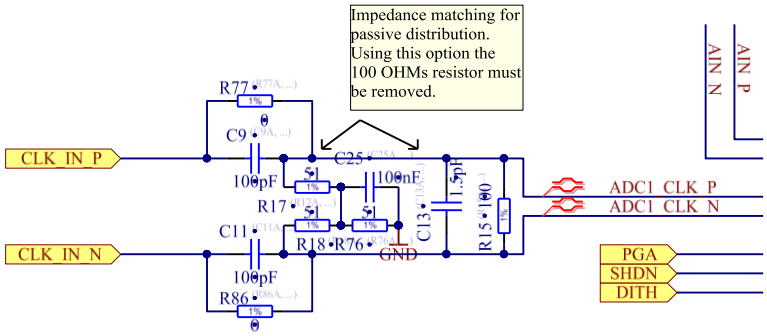
- Passive Splitter
  - This option is used to avoid adding Phase Noise to the sampling clock. This input is directly connected via a differential circuit to the ADC inputs.

Notice

- Do not exceed the Max input Power of 14 dBm on the RF inputs and 10 dBm on the clock inputs. It can permanently damage the devices.

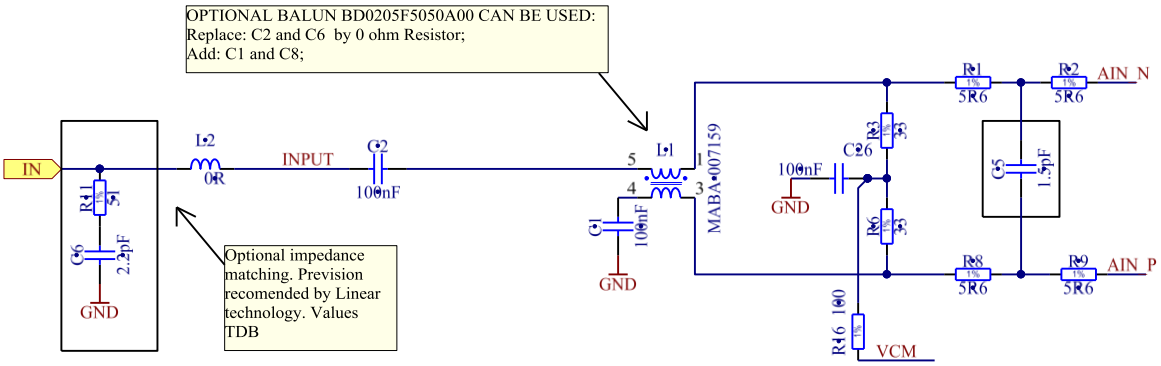
3.2 Schematics

3.2.1 Clock matching network – FMC_ADC130M_v3



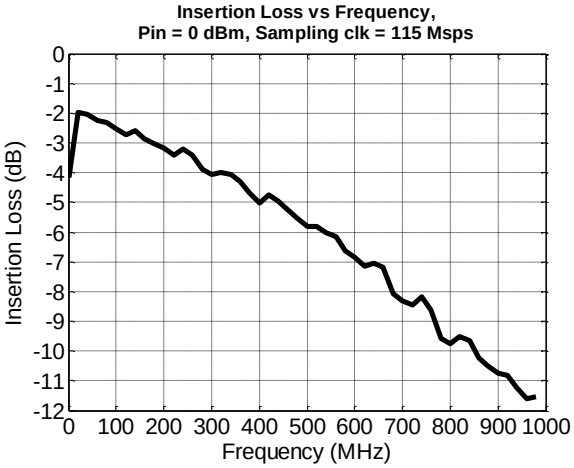
- On the external clk version, R76, R77 e R86 are not soldered.
- On the internal clk version, C9, C11, C13 e R15 are not soldered.

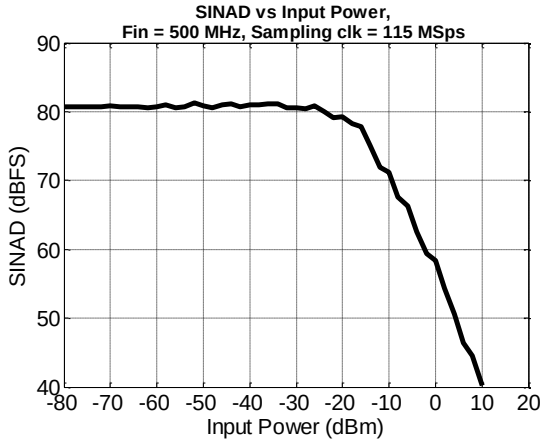
3.2.2 RF conditioning Schematic – FMC_ADC130M_v3

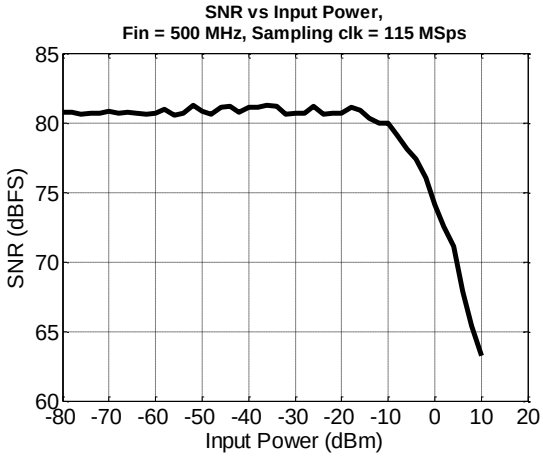


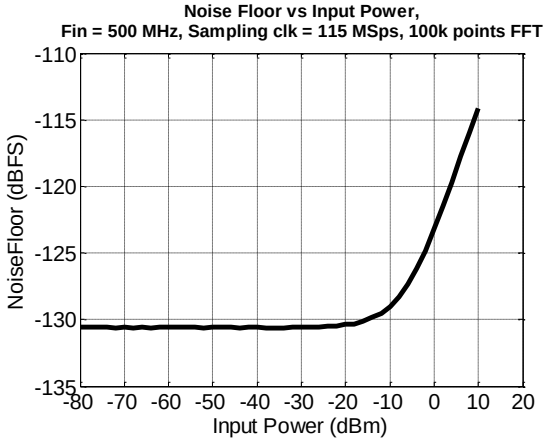
3.3 Typical Performance Characteristics[4]

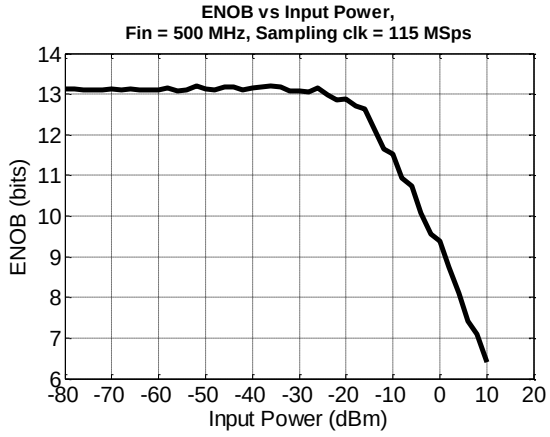
The results presented on this section show the typical characteristics for a sampling channel of the FMC-ADC-130M_v3 electronics[5].

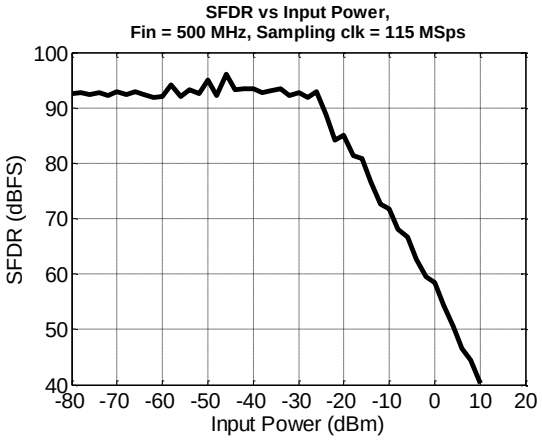




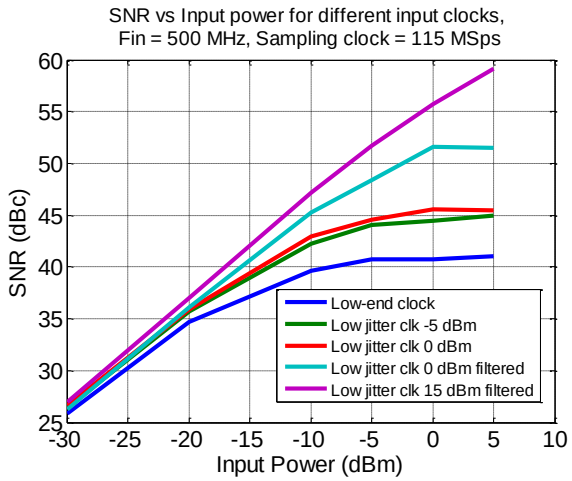


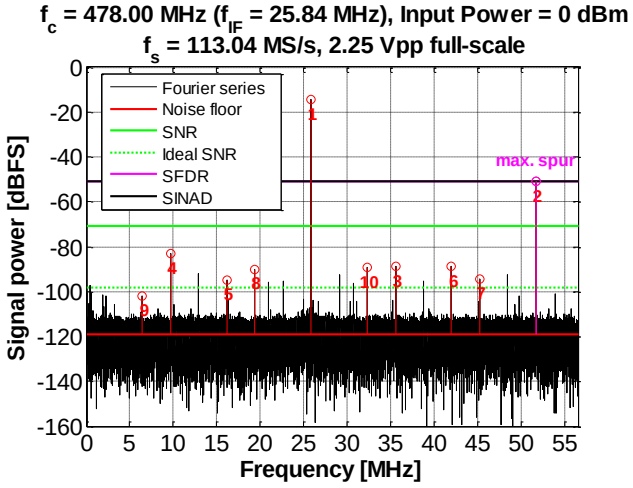




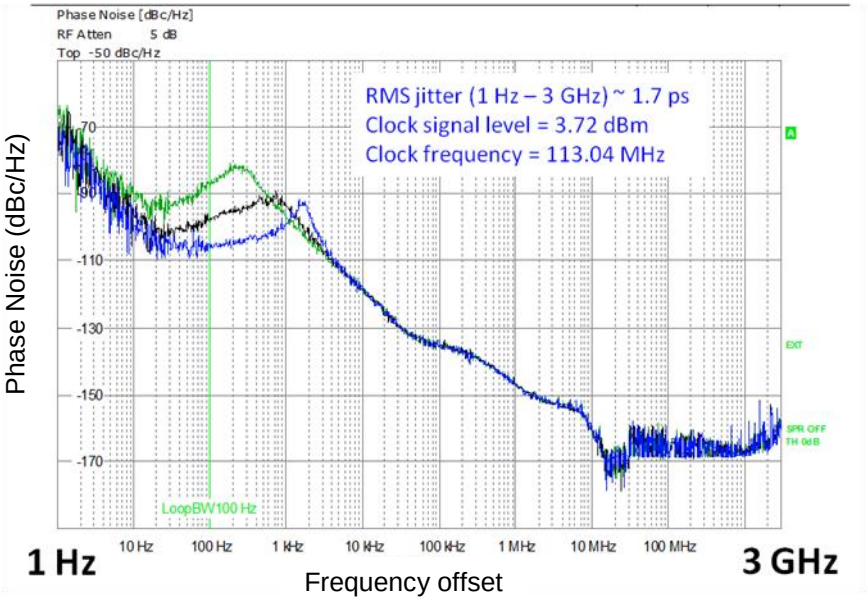


[4] The plots were taken considering 100k points FFT, which a means a process gain of $10.log_{10}(M/2) \sim 47$ dB.
[5] All the measurements were performed using Rohde & Schwarz SMA100A RF signal generator on clock and RF inputs (external clock option on the ADC boards).





- Clock performance for the internal clock generator option and the si571 VCXO, reference input from SMA100A. Phase noise and jitter characteristics in a 3 GHz bandwidth considering three different loop filter bandwidths.



3.4 PCB Design

- Symmetric RC channels
- Designed with FR4 substrate
- Improved grounding schemes
- Enclosure as shielding and thermal dissipator
- SMA connectors fixed by the shielding
- 6-layers, FMC form factor

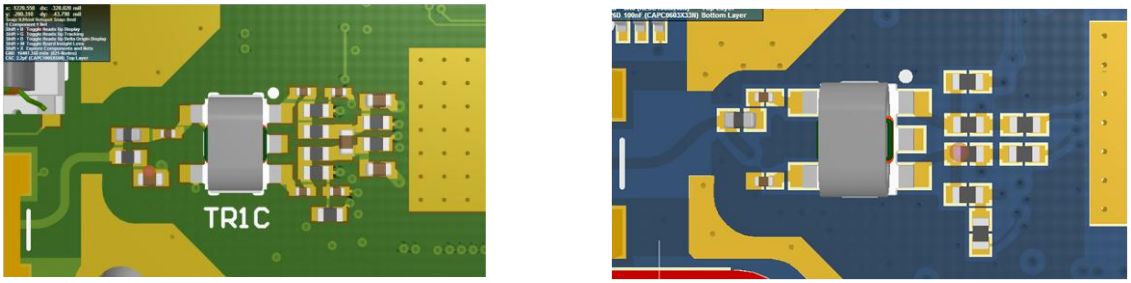


Figure: RF input layout for version 1 on left and version 3, on right.

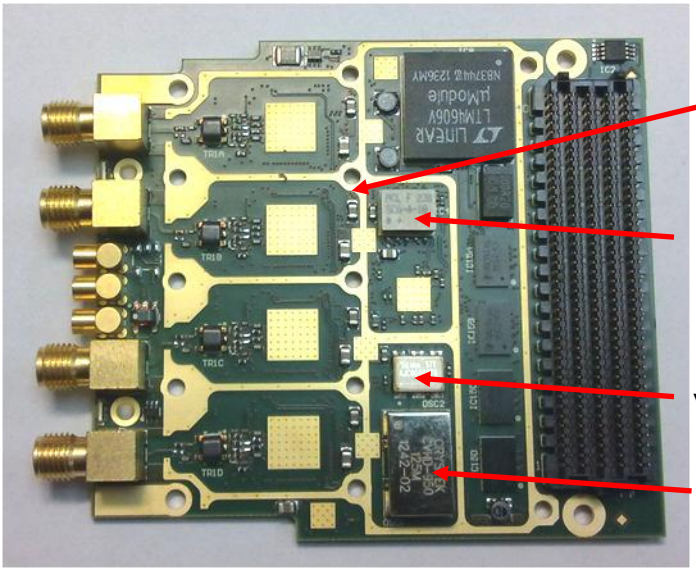


Figure: ADC board with some comments.

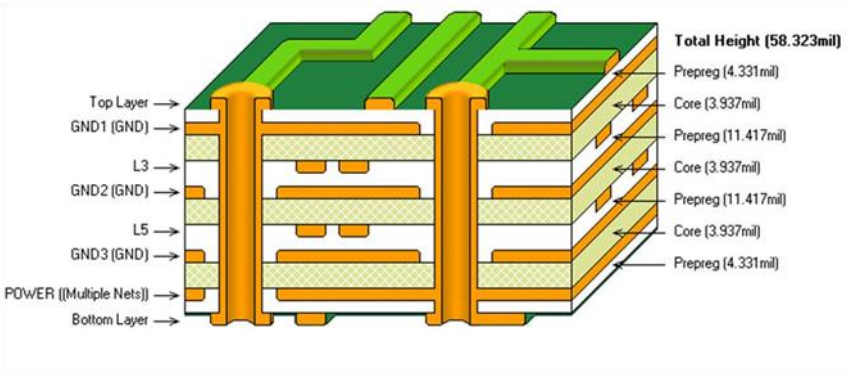
4. PCB Fabrication Requirements

Design references			
Name	FMC_ADC130M_v3		
File name(s)	FMC_ADC130M_v3		
Designer	Beam Diagnostics Group, LNLS		
E-mail	dig@lnls.br		
Fone	+55 19 3512-5071	Date	07/01/2014

Mechanical characteristics	
External size (mm)	FMC standard
Thickness (mm)	1.6 mm
Multilayers	8 layers
Min track width (mm/mils)	
Min Hole size (mm/mils)	
Laminate	FR-4
Pre-preg	FR-4
Finish Copper	
External layers (µm)	35 µm
Holes walls (µm)	25 µm
Internal Layers-Planes (µm)	35 µm
Internal Layers-Signals (µm)	35 µm
Board finishing requirements	
Silkscreen on top layer (color)	Green
Silkscreen on bottom layer (color)	Green
Surface Finishing	ENIG – Electroless Nickel / Immersion Gold according to IPC-4552
Thickness	Ni: 3 µm min, 6 µm máx. Au: 0.05 µm min, 0.125 µm máx

Additional Information	
Impedance test	No
Packaging requirements	No
Documentation to be delivered	No
Additional control quality requirements	No

Board Stackup Information			
		Laminate/pre-preg	Thickness (mm/mils)
Layer 1	RF signals	FR4	Refer to figure
Layer 2	RF Ground Plane	FR4	Refer to figure
Layer 3	Digital signaling	FR4	Refer to figure
Layer 4	Ground Plane	FR4	Refer to figure
Layer 5	Digital signaling	FR4	Refer to figure
Layer 6	Ground Plane	FR4	Refer to figure
Layer 7	Digital signaling	FR4	Refer to figure
Layer 8	Ground Plane	FR4	Refer to figure



5. References

[1] "Military Handbook - Reliability Prediction of Electronic Equipment," Department of Defense - United States of America, 1990.