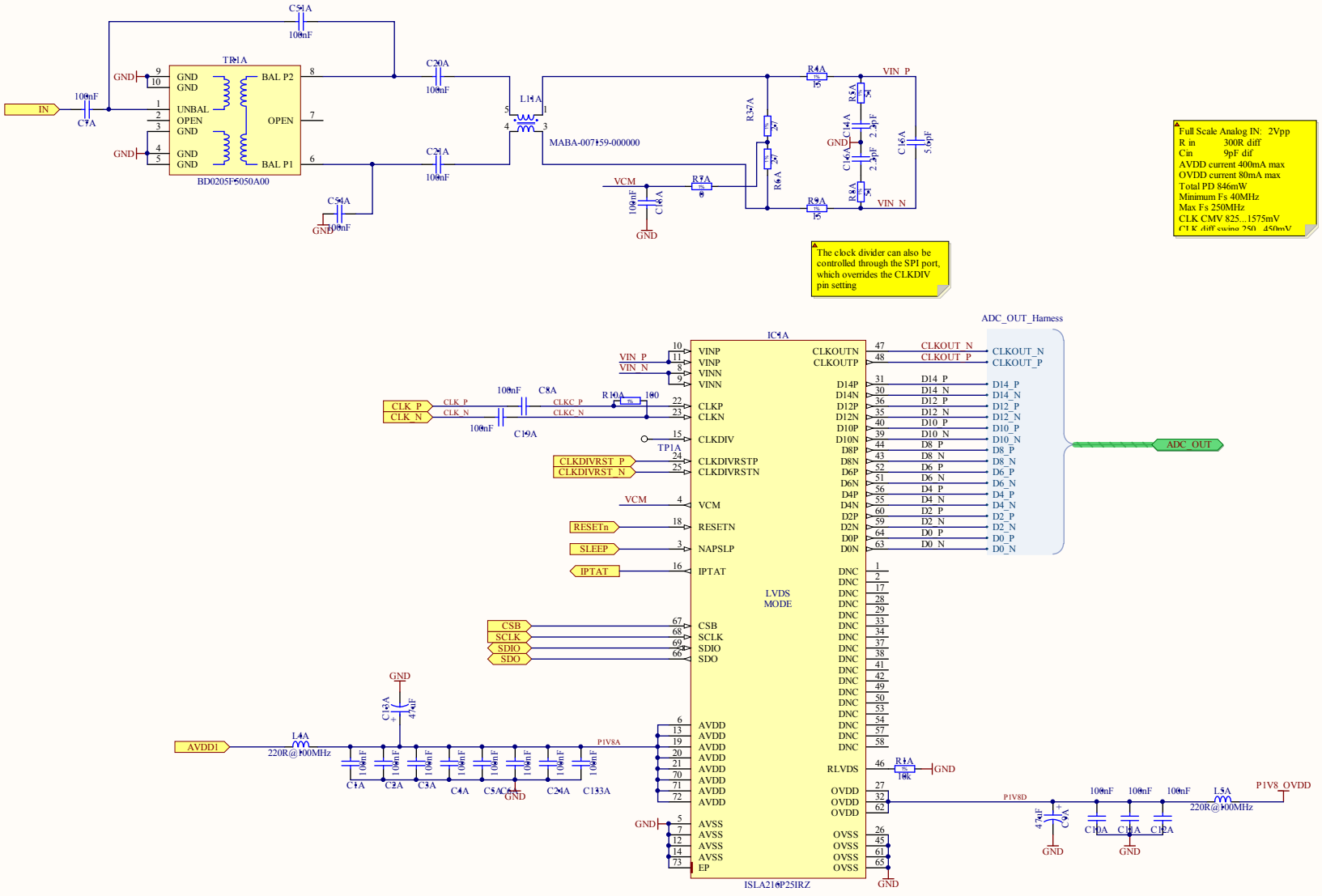

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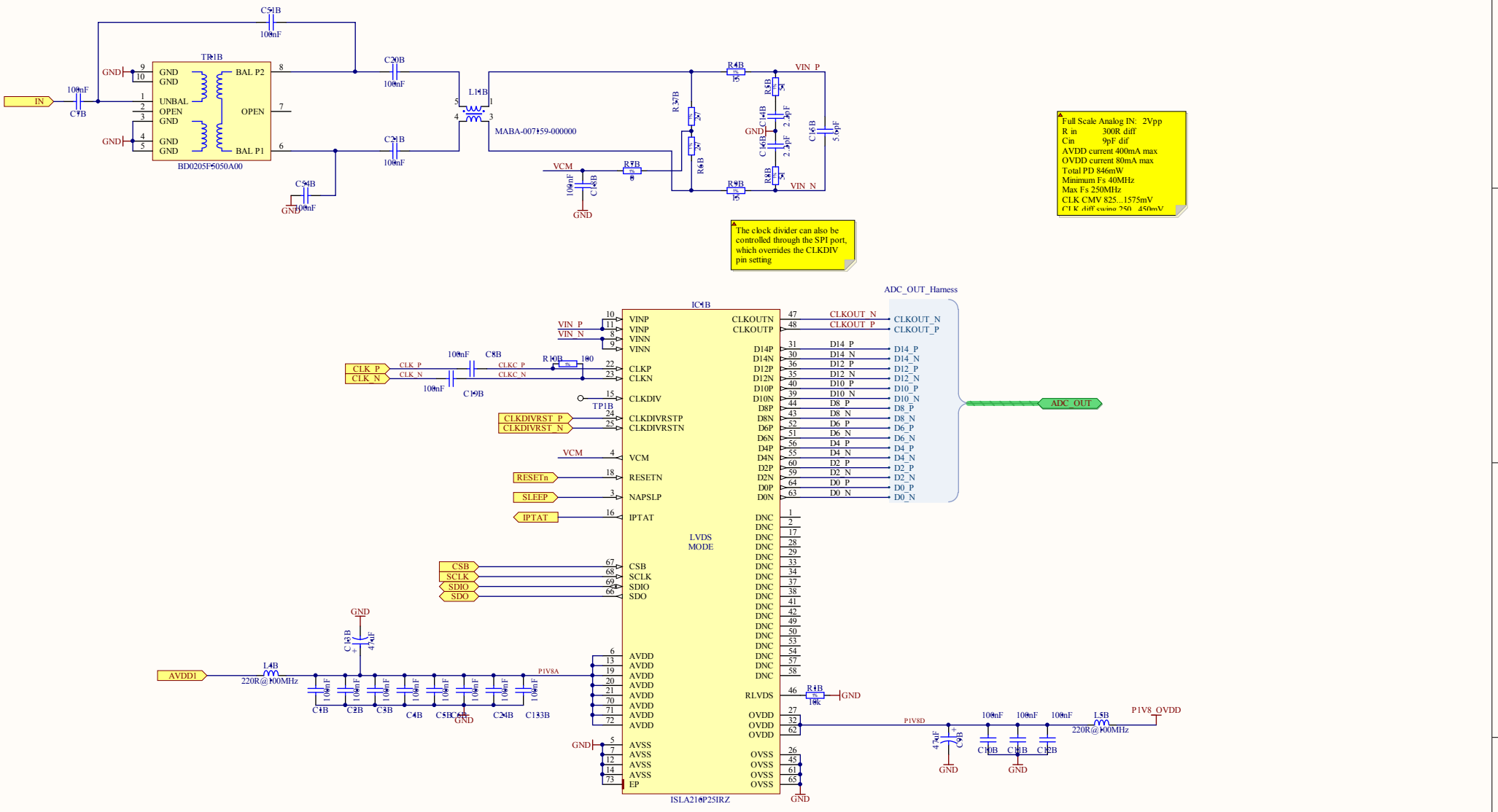
File: C:\Users\...\ADC.SchDoc		Drawn By:



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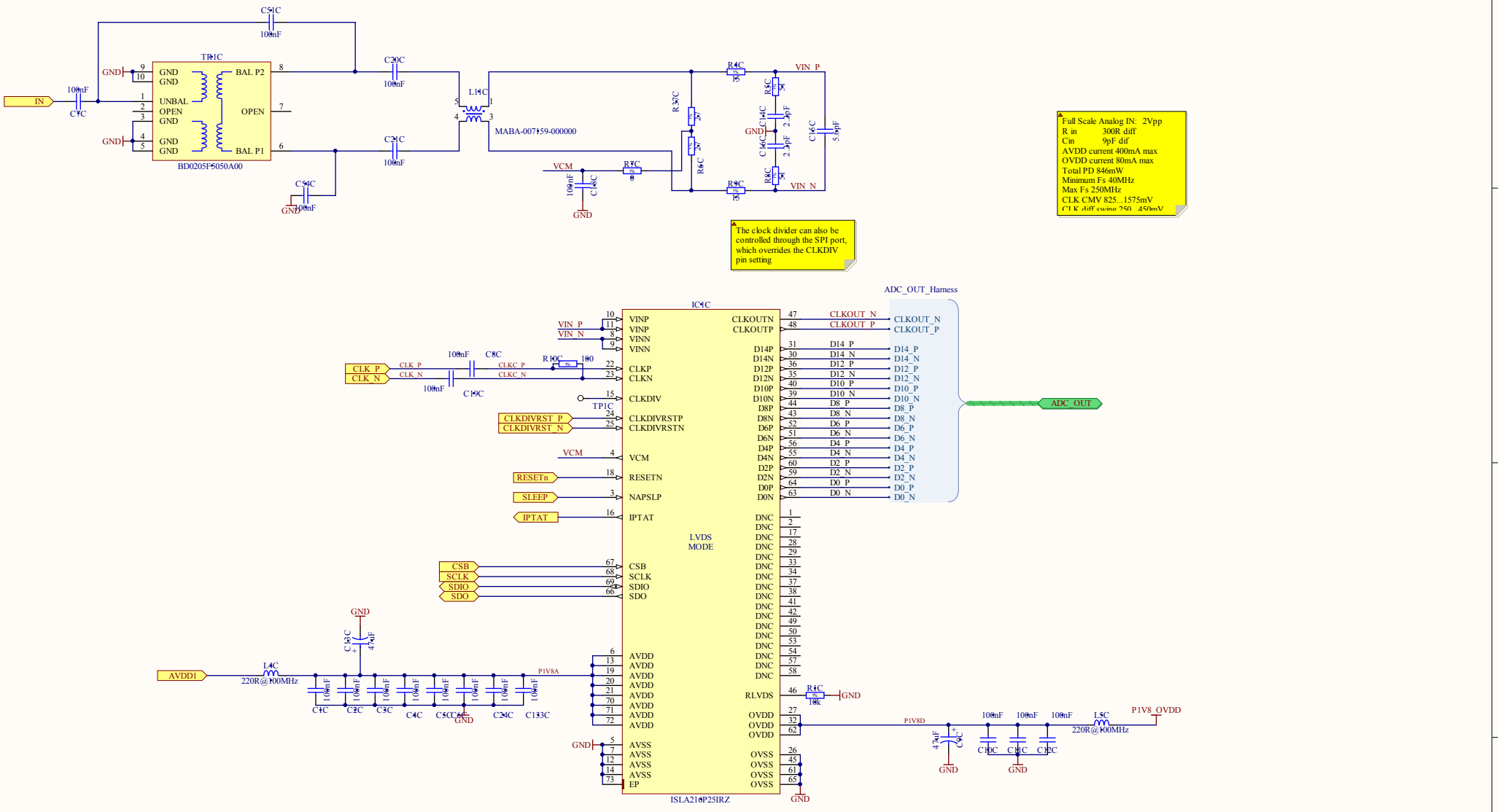

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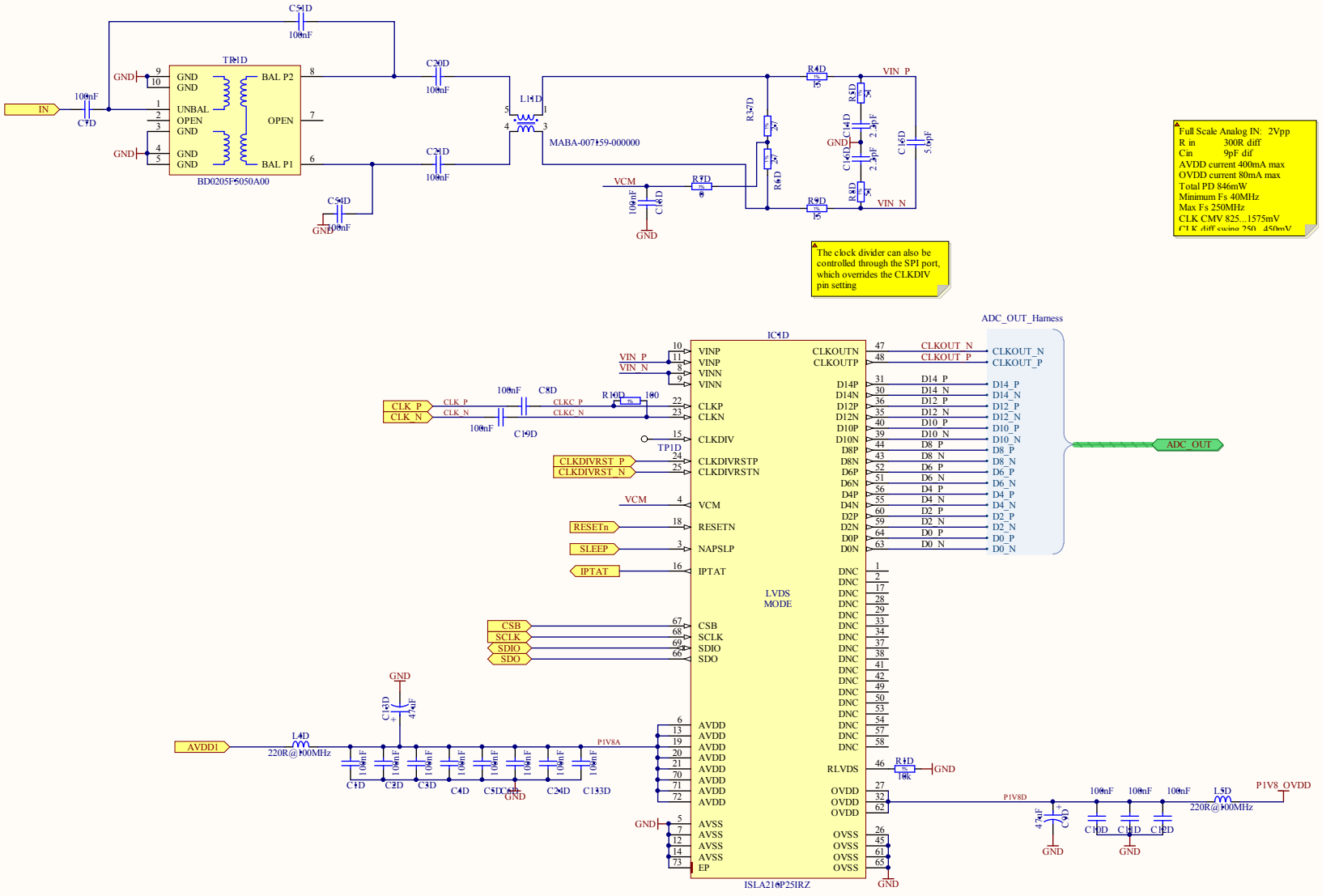

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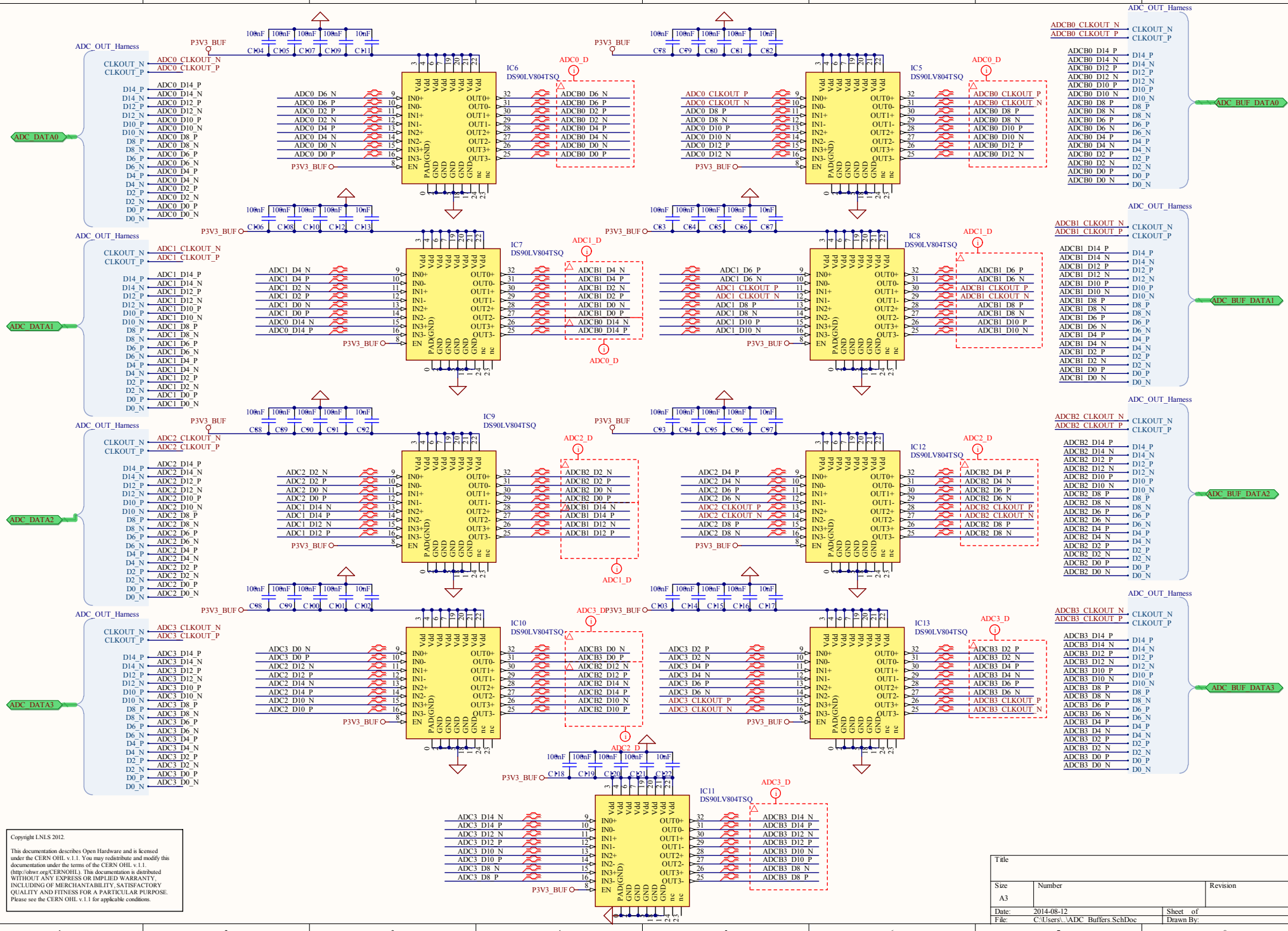
ADC_OUT_Harness
ADC_DATA0
ADC_DATA1
ADC_DATA2
ADC_DATA3
ADC_BUF_DATA0
ADC_BUF_DATA1
ADC_BUF_DATA2
ADC_BUF_DATA3
P3V3_BUF
IC6 DS90LV804TSQ
IC5 DS90LV804TSQ
IC7 DS90LV804TSQ
IC8 DS90LV804TSQ
IC9 DS90LV804TSQ
IC12 DS90LV804TSQ
IC10 DS90LV804TSQ
IC13 DS90LV804TSQ
IC11 DS90LV804TSQ
ADC0_D
ADC1_D
ADC2_D
ADC3_D
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ADC clock IN

Si570 I2C signalling:
Hi 0.75xVdd = 2.475
Lo 0.5V

The exact ADC clock frequency will be defined in the future, hence the frequency must be confirmed with LNLS before the board layout design. At present LNLS is considering:
- Reference signal: ((499.796/864)*N) MHz
- ADC clock frequency: Reference signal*384/N
Where N is an integer number ranging from 1 to 40.

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IPTAT

Temp=(I-K)/m
or
Temp=(V-RK)/Rm

m=9uV/160C
R=49.9K
K=15uV
Temp=(I-K)/m

Trigger threshold voltage: 1V

Input voltage range for normal operation:
min. 1.65V (3.3V with 50ohm termination on both ends of the cable, so divided by 2)
max. 5V with termination on both ends of the cable

Input is +/- 7.5V tolerant for continous overload and +/-10V tolerant for short term overload.

When inserted to HPC there exist an eeprom with address 1010_100

GA0 = GND on ML605

GA1 = 3.3V on LPC
GA1 = GND on HPC

A2 is GND. GOOD

24AA64T = b"10100 GA0 GA1"

Warning!
Following the VITA 57.1 standard:
GA0 goes to A1
GA1 goes to A0

IC22
24AA64T-I/MC
SDA
SCL
A2
A1
A0
WP
VCC
EP
VSS
GND
3P3VAUX
C85 100nF

Trigger indicating LED
Acquisition indicating LED
LD1
P3V3D
R2 200 1%
R41 200 1%
R27 200 1%
Q1A PMGD280UN
Q1B PMGD280UN
Q2A PMGD280UN
LED1
LED2
LED3

IC15
AMC7823IRTAT
EXT_REF_IN
ISET_RES
PREC_I_OUT
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
DAC 0_OUT
DAC 1_OUT
DAC 2_OUT
DAC 3_OUT
DAC 4_OUT
DAC 5_OUT
DAC 6_OUT
DAC 7_OUT
AVDD
AGND
EP
SGND
SCLK
MOSI
MISO
SS
RESET
GPIO-5
GPIO-4
GPIO-3/ALR3
GPIO-2/ALR2
GPIO-1/ALR1
GPIO-0/ALR0
DAV
GALR
CONVERT
ELDAC
BVDD
DVDD
DGND
MON_SCLK
MON_MOSI
MON_MISO
MON_SSn
MON_DAVn
R46 200 1%
R47 200 1%
IPTAT1
IPTAT2
IPTAT3
IPTAT4
R82 200 1%
R83 200 1%
R84 200 1%
R85 200 1%
C22 100nF
C23 100nF

FTG1 ... FTG6
Reference points for the component mounting machine.

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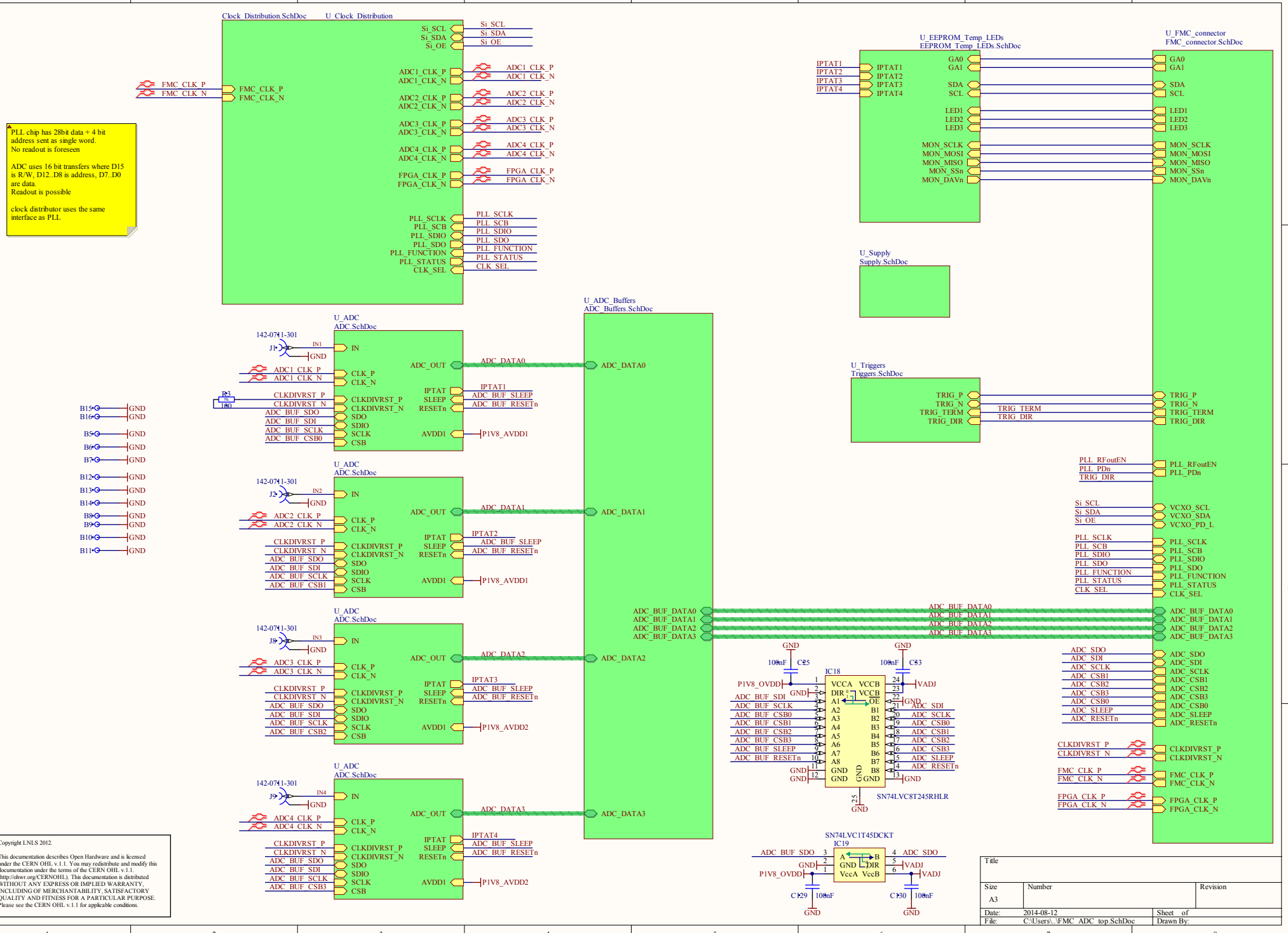
File: C:\Users\...\EEPROM_Temp_LEDs.SchDoc	Drawn By:	


Clock_Distribution.SchDoc
U_Clock_Distribution
PLL chip has 28bit data + 4 bit address sent as single word.
No readout is foreseen
ADC uses 16 bit transfers where D15 is R/W, D12..D8 is address, D7..D0 are data.
Readout is possible
clock distributor uses the same interface as PLL
U_EEPROM_Temp_LEDs
EEPROM_Temp_LEDs.SchDoc
U_FMC_connector
FMC_connector.SchDoc
U_Supply
Supply.SchDoc
U_ADC_Buffers
ADC_Buffers.SchDoc
U_ADC
ADC.SchDoc
U_Triggers
Triggers.SchDoc
IC18
SN74LVC8T245RHLR
IC19
SN74LVC1T45DCKT
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ADC_OUT_Harness

ADC_BUF_DATA0

D0_N D0_P D2_N D2_P D4_N D4_P D6_N D6_P D8_N D8_P D10_N D10_P D12_N D12_P D14_N D14_P CLKOUT_P CLKOUT_N

HA01_CC_N HA01_CC_P HA04_N HA04_P HA05_N HA05_P HA09_N HA09_P HA03_N HA03_P HA02_N HA02_P HA07_N HA07_P HA06_N HA06_P HA00_CC_P HA00_CC_N

ADC_BUF_DATA1

LA04_N LA04_P LA03_N LA03_P LA08_N LA08_P LA07_N LA07_P LA12_N LA12_P LA13_N LA13_P LA11_N LA11_P LA16_N LA16_P LA01_CC_P LA01_CC_N

ADC_BUF_DATA2

LA17_CC_N LA17_CC_P LA20_N LA20_P LA23_N LA23_P LA19_N LA19_P LA22_N LA22_P LA21_N LA21_P LA25_N LA25_P LA26_N LA26_P LA18_CC_P LA18_CC_N

ADC_BUF_DATA3

HB00_CC_N HB00_CC_P HB11_N HB11_P HB12_N HB12_P HB10_N HB10_P HB15_N HB15_P HB14_N HB14_P HB18_N HB18_P HB17_CC_N HB17_CC_P HB06_CC_P HB06_CC_N

HA12_N LA28_N LA30_N LA31_P LA30_P LA31_N LA32_P LA32_N LA29_P LA24_N LA24_P LA33_P LA33_N LA06_P LA06_N LA05_P HA13_P LA10_N LA09_N LA10_P LA09_P HA21_P HA21_N HA22_P HA22_N HA18_P HA18_N HA23_P HA23_N HA14_P LA27_P LA27_N LA05_N LA14_P LA14_N

ADC_SLEEP MON_DAVn MON_SSn MON_SCLK MON_MISO MON_MOSI CLKDIVRST_P CLKDIVRST_N LED1 LED2 LED3 TRIG_P TRIG_N VCXO_SCL VCXO_SDA VCXO_PD_L ADC_RESETn ADC_CSB0 ADC_CSB1 ADC_CSB2 ADC_CSB3 PLL_SCB PLL_SDIO PLL_SCLK CLK_SEL PLL_STATUS PLL_FUNCTION PLL_SDO PLL_PDn PLL_RFoutEN TRIG_DIR TRIG_TERM ADC_SDO ADC_SCLK ADC_SDI

FMC_CLK_P FMC_CLK_N FPGA_CLK_P FPGA_CLK_N

CLK3_BIDIR_P CLK3_BIDIR_N CLK0_M2C_P CLK0_M2C_N

J6A

GND DP1_M2C_P DP1_M2C_N DP2_M2C_P DP2_M2C_N DP3_M2C_P DP3_M2C_N DP4_M2C_P DP4_M2C_N DP5_M2C_P DP5_M2C_N DP1_C2M_P DP1_C2M_N DP2_C2M_P DP2_C2M_N DP3_C2M_P DP3_C2M_N DP4_C2M_P DP4_C2M_N DP5_C2M_P DP5_C2M_N

P3V3D R32 4k7 CLK_DIR

J6B

CLK_DIR DP9_M2C_P DP9_M2C_N DP8_M2C_P DP8_M2C_N DP7_M2C_P DP7_M2C_N DP6_M2C_P DP6_M2C_N GBTCLK1_M2C_P GBTCLK1_M2C_N DP9_C2M_P DP9_C2M_N DP8_C2M_P DP8_C2M_N DP7_C2M_P DP7_C2M_N DP6_C2M_P DP6_C2M_N RES0

J6C

DPO_C2M_P DPO_C2M_N DPO_M2C_P DPO_M2C_N LA06_P LA06_N LA10_P LA10_N LA14_P LA14_N LA18_CC_P LA18_CC_N LA27_P LA27_N SCL SDA GA0 P12V0 P12V0 P3V3 P3V3

J6D

PG_C2M DP0_C2M_P DP0_C2M_N GBTCLK0_M2C_P GBTCLK0_M2C_N DP0_M2C_P DP0_M2C_N LA01_CC_P LA01_CC_N LA05_P LA05_N LA09_P LA09_N LA13_P LA13_N LA17_CC_P LA17_CC_N LA23_P LA23_N LA26_P LA26_N TCK TDI TDO 3P3VAUX TMS TRST_L GA1 3P3V 3P3V 3P3V

J6E

HA01_CC_P HA01_CC_N HA05_P HA05_N HA09_P HA09_N HA13_P HA13_N HA16_P HA16_N HA20_P HA20_N HB03_P HB03_N HB05_P HB05_N HB09_P HB09_N HB13_P HB13_N HB19_P HB19_N HB21_P HB21_N VADJ

J6F

PG_M2C HA00_CC_P HA00_CC_N HA04_P HA04_N HA08_P HA08_N HA12_P HA12_N HA15_P HA15_N HA19_P HA19_N HB02_P HB02_N HB04_P HB04_N HB08_P HB08_N HB12_P HB12_N HB16_P HB16_N HB20_P HB20_N VADJ

J6G

CLK1_M2C_P CLK1_M2C_N LA00_CC_P LA00_CC_N LA03_P LA03_N LA08_P LA08_N LA12_P LA12_N LA16_P LA16_N LA20_P LA20_N LA22_P LA22_N LA25_P LA25_N LA29_P LA29_N LA31_P LA31_N LA33_P LA33_N VADJ

J6H

VREF_A_M2C PRSNT_M2C_L CLK0_M2C_P CLK0_M2C_N LA02_P LA02_N LA04_P LA04_N LA07_P LA07_N LA11_P LA11_N LA15_P LA15_N LA19_P LA19_N LA21_P LA21_N LA24_P LA24_N LA28_P LA28_N LA30_P LA30_N LA32_P LA32_N VADJ

J6I

CLK3_BIDIR_P CLK3_BIDIR_N HA03_P HA03_N HA07_P HA07_N HA11_P HA11_N HA14_P HA14_N HA18_P HA18_N HA22_P HA22_N HB01_P HB01_N HB07_P HB07_N HB11_P HB11_N HB15_P HB15_N HB18_P HB18_N VIO_B_M2C

J6J

VREF_B_M2C CLK2_BIDIR_P CLK2_BIDIR_N HA02_P HA02_N HA06_P HA06_N HA10_P HA10_N HA17_CC_P HA17_CC_N HA21_P HA21_N HA23_P HA23_N HB00_CC_P HB00_CC_N HB06_CC_P HB06_CC_N HB10_P HB10_N HB14_P HB14_N HB17_CC_P HB17_CC_N VIO_B_M2C

B1 B3 B2 B4 GND GND

B1 ... B4
screw holes for mounting the FmcAdc to the carrier board.

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.

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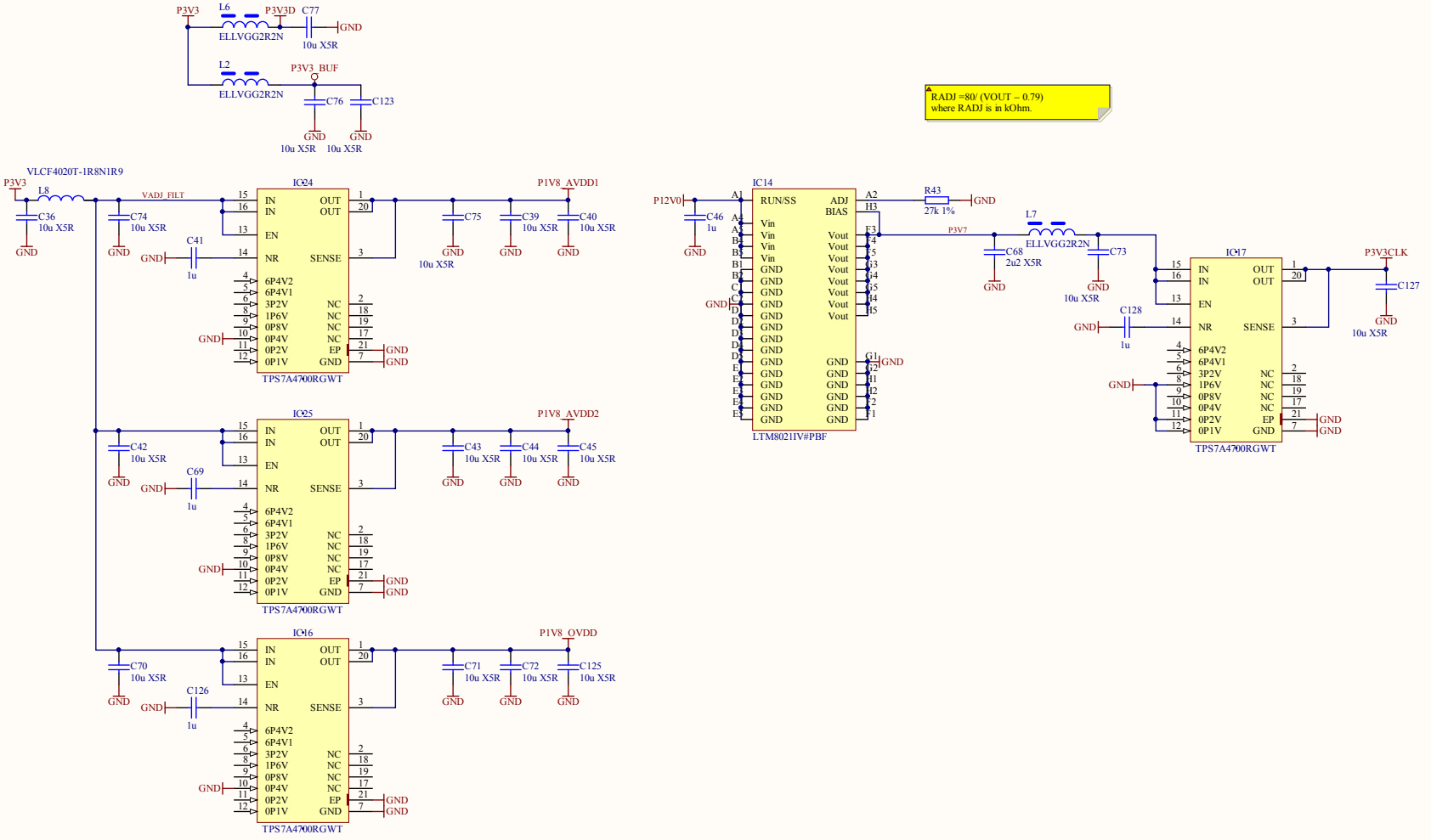

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Date:	2014-08-12	Sheet of	
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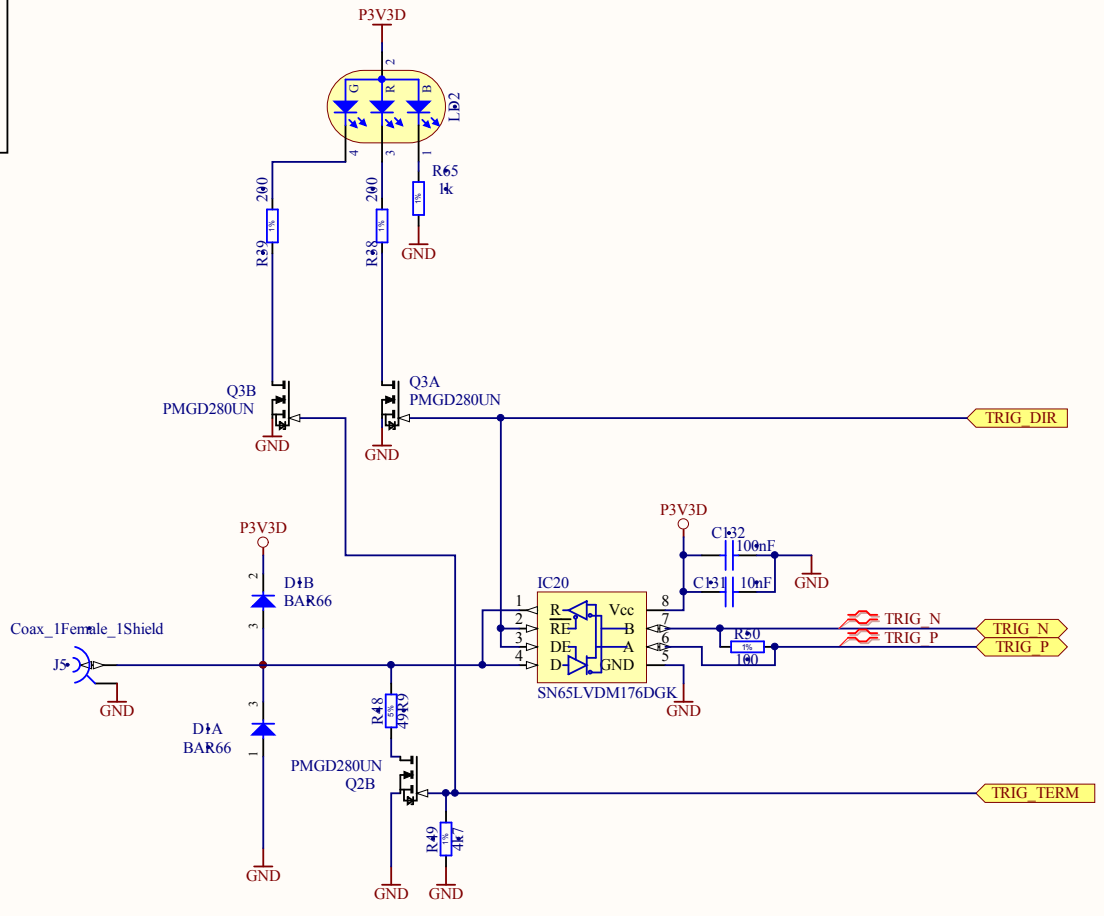

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Date: 2014-08-12		Sheet of
File: C:\Users\..\Triggers.SchDoc		Drawn By: