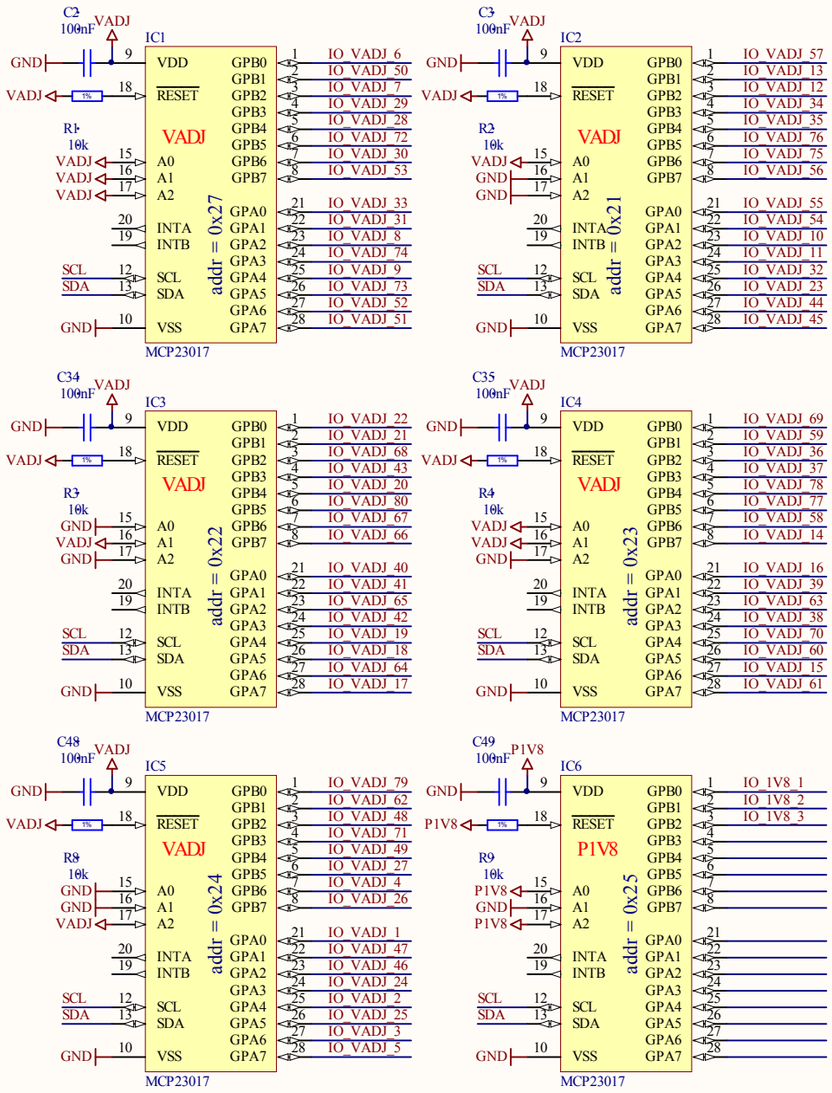
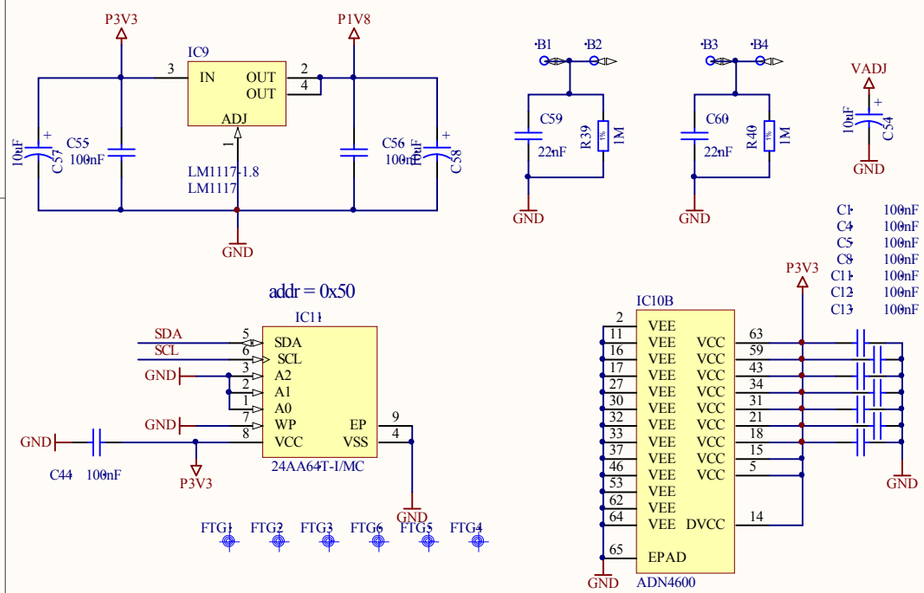
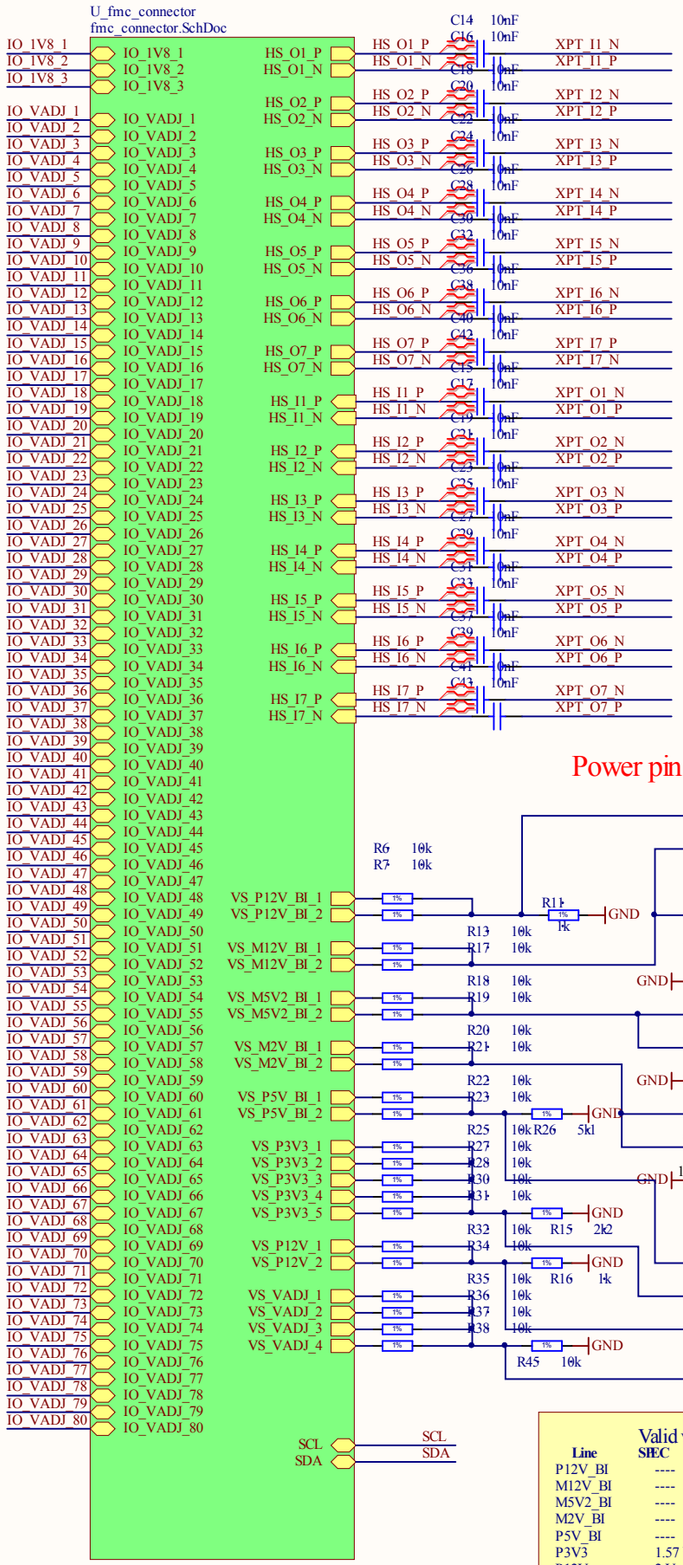
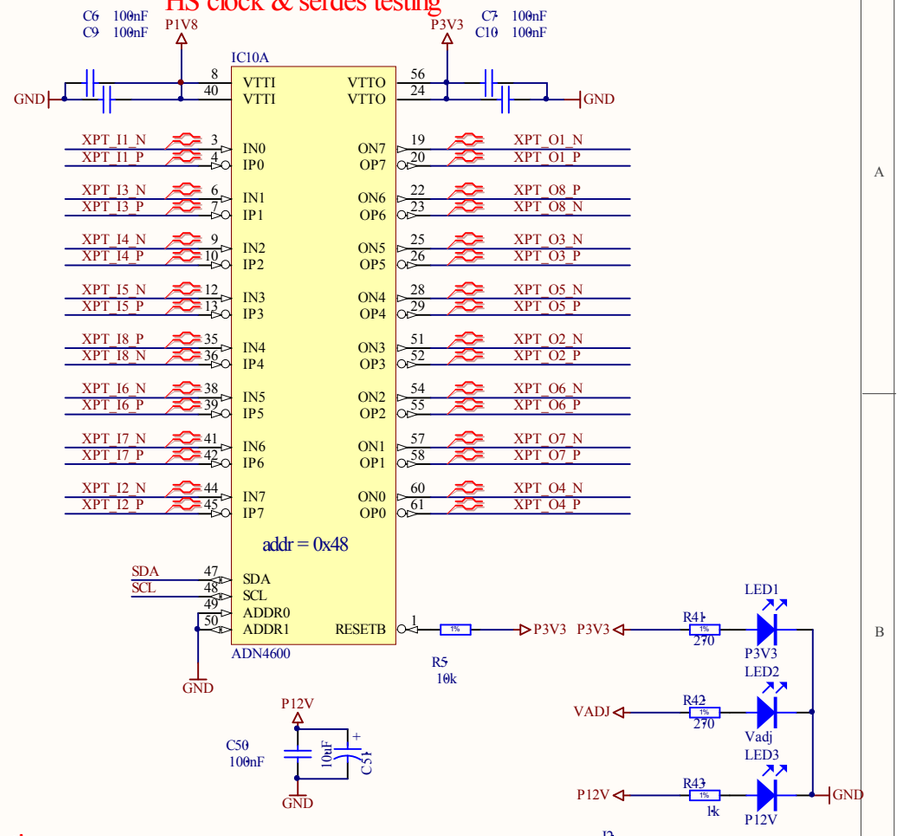
I/O Line testing

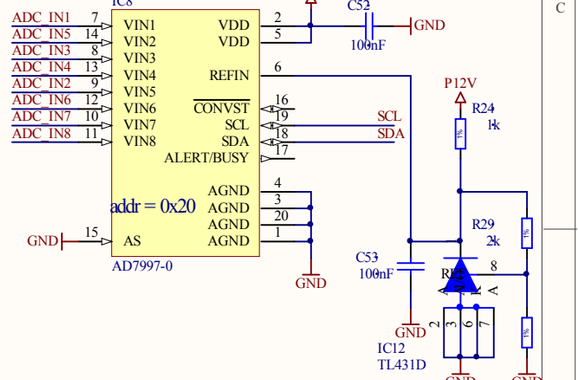






HS clock & serdes testing





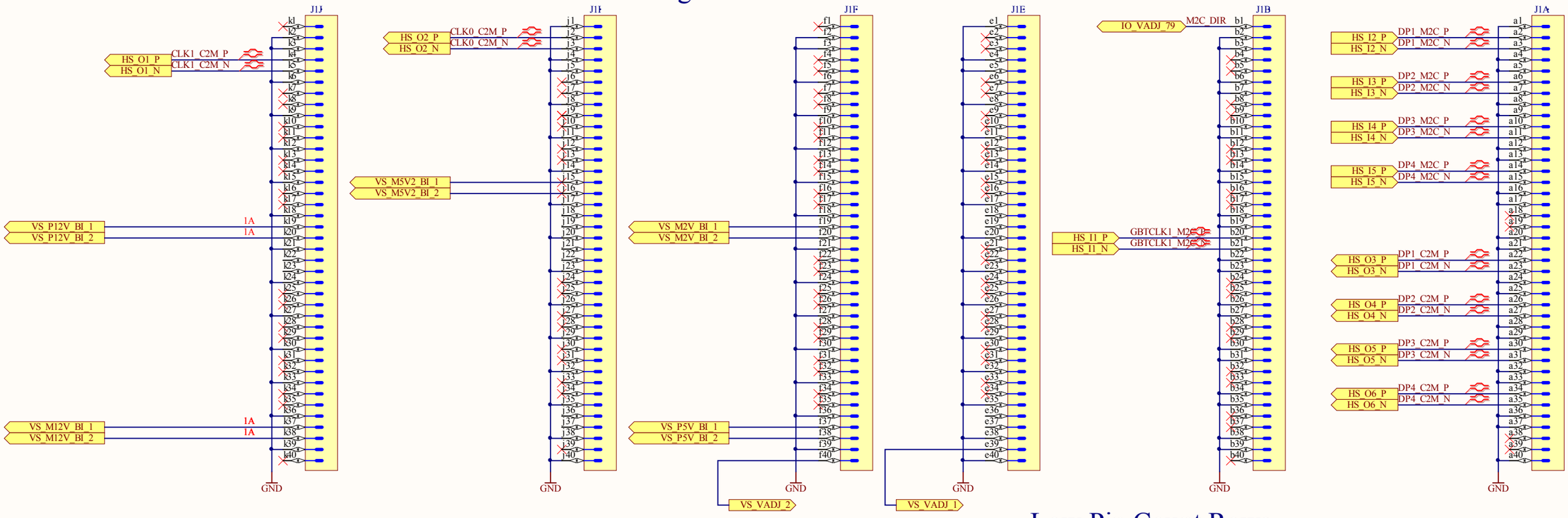
Power pin testing

Valid voltage values

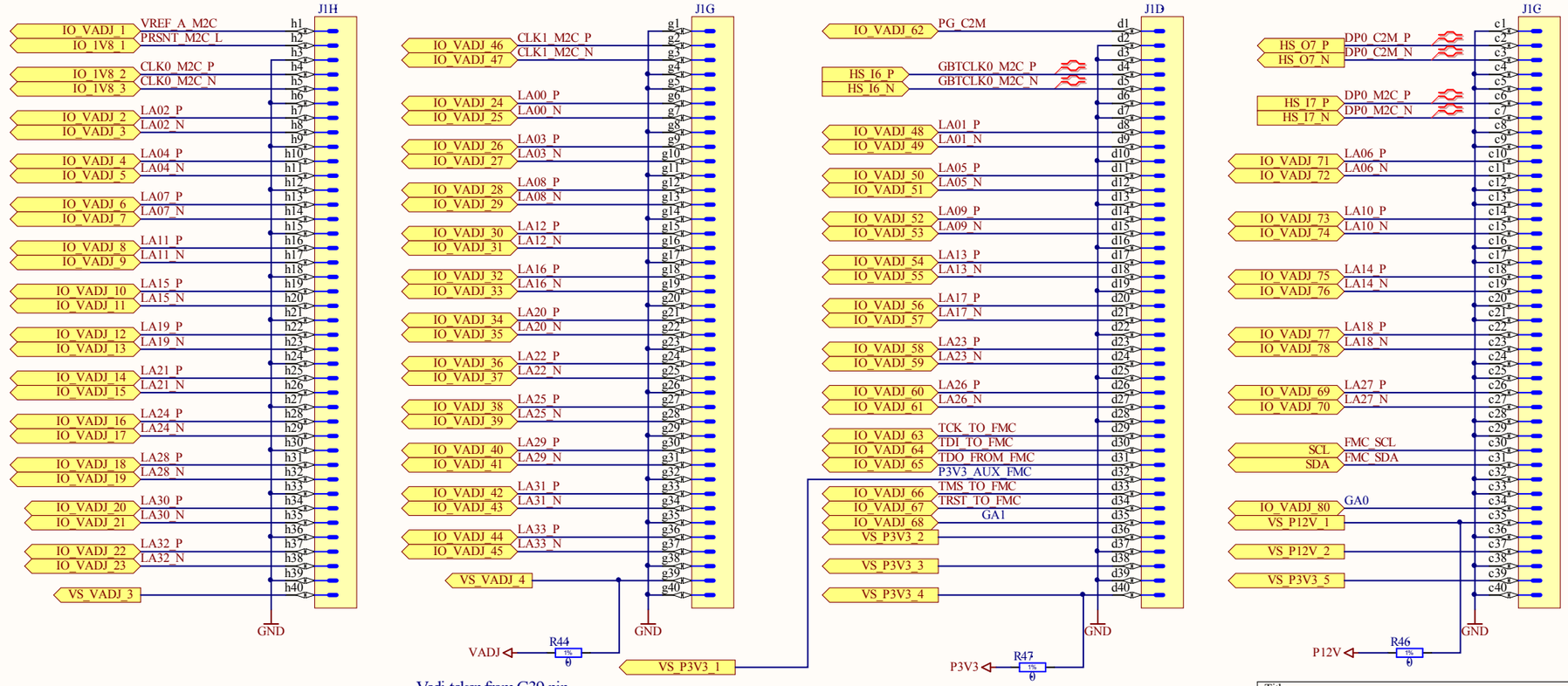
Line	SPEC	HC/VIC	Failure if...
P12V_BI	----	2 V	less
M12V_BI	----	2.4 V	less
M5V2_BI	----	2.28 V	less
M2V_BI	----	2 V	less
P5V_BI	----	2.52 V	less
P3V3	1.57 V	1.57 V	less
P12V	2 V	2 V	less
Vadj (2.5V)	2 V	2 V	less

Title	FMC Carrier testboard - main schematic		
Size: A3	Number:		Revision: 1.0
Date: 1/10/2011		Sheet of	
File: C:\altium-projects\..\fmc_carrier_tester.SchDoc		Drawn By:	

High Pin Count Rows



Low Pin Count Rows



Vadj taken from G39 pin

P3V3 taken from D40 pin

P12V taken from C35 pin

Title: FMC Carrier testboard - HPC FMC connector		
Size: A3	Number:	Revision: 1.0
Date: 1/10/2011		Sheet of
File: C:\altium-projects\..\fmc_connector.SchDoc		Drawn By:

Number	?
Drawn By	TW
DATE	06-01-2010
MOD.	-

Print Date 1/10/2011 5:47:02 PM

Mechanical 11