FMC3 Functional Specification

Matthieu Cattin

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Abstract

FMC3 is a 4-channel 16-bit 10Ms/s DAC card in FMC (FPGA Mezzanine Card [1]) form-factor. This document describes the hardware only. Another functional specification is dedicated to the HDL related to the FMC3 card (see *FMC3 HDL functional specification*).

1   Features

- 4 single-ended analog output channels

- Output voltage range : +/-10V (50 ohms)

- 16-bit DACs

- Up to 10MS/s

- 1 external clock input (single-ended)

- 1 start input (TTL)

- 1 pause input (TTL)

- 1 abort input (TTL)

- Each channel can store up to 32 waveform.

- Memory/channel is determined by FMC carrier.

- Analog outputs auto-calibration.

- I^2C EEPROM to store IPMI information and DACs calibration factors

- 2 modes (vectors and points)

2   General description

An FMC3 is a mezzanine card in FMC format, containing four identical analog output channels. Each channel has a 10MS/s 16-bit DAC with an output range of +/-10V. In addition, the card has three trigger inputs (start, pause and abort) and one external clock input. Those inputs are common to the four analog channels.

3   Clock input

The FMC3 card has an external clock input. It is compatible with many different electrical standards, like TTL, LVTTL, PECL, sine-wave, etc...

External clock input features:

- 50 ohms terminated

- 100Hz to 10MHz

- 0.6Vpp to 1Vpp (max. 10Vpp)

Nevertheless, the external clock input doesn't have to be used, as DACs clock can be provided by the FMC carrier card.

4   Trigger inputs

The FMC3 has 3 trigger inputs. A start, a pause and an abort input. They can be used in many different ways. For further information see the *FMC3 HDL functional specification.*

All trigger inputs are TTL compliant with an internal 50 ohms termination. Trigger inputs polarity is selectable via a register (TTL or $\overline{TTL}$).

5   Analog outputs

Table 1 lists expected FMC3 analog outputs characteristics. Those are taken from an National Instruments PCI analog output card [2].

Table 1: Analog outputs characteristics

Range	$\pm$10V
INL[1]	$\pm$2.2 LSB max.
DNL[1]	$\pm$1.0 LSB max.
Monotonicity[1]	16 bits
Offset error[1]	$\pm$168uV max
Gain error[1]	$\pm$30ppm of output max
Offset temperature coefficient	$\pm$35μV/$^\circ$C
Gain temperature coefficient	$\pm$6.5ppm/$^\circ$C
Onboard calibration reference	
Level	5.000V
Temperature coefficient	$\pm$0.6ppm/$^\circ$C
Long-term stability	$\pm$15ppm/$\sqrt{1000h}$
Slew rate	>15V/μ
Noise	80μV, DC to 10MHz
Channel crosstalk	-95dB
Settling time	25ns to $\pm$1 LSB accuracy
Total harmonic distortion	-90dB typ
	(generating a 10V, 1000 points,
	7.5kHz sinewave, summing 9 harmonics)

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[1]Measured after calibration

6   Auto-calibration

Analog output channels can be auto-calibrated via an on-board ADC. Calibration information is then stored in the on-board EEPROM.

7   Physical description

Figure 1 shows the standard single width FMC board shape. The FMC3 card is connected to its carrier through a high-pin count connector from Samtec (see FMC standard [1] for further details), also visible in figure 1.
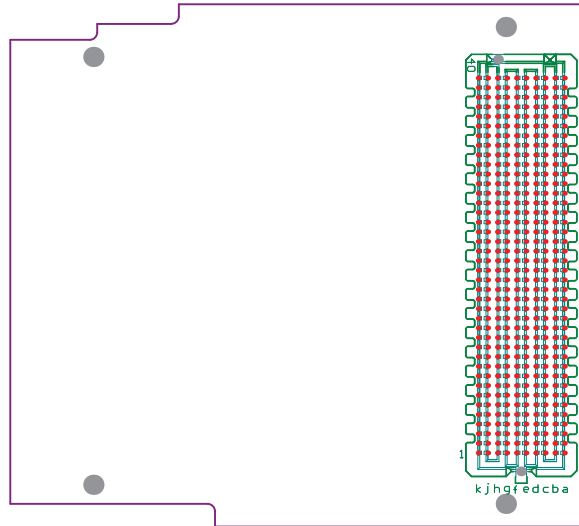

Figure 1: FMC single width board shape (scale 1:1)

Due to the small amount of space on the front panel, it has been decided to use only one MDR[1] multi-pin connector on the FMC. This connector will carry all I/O signals to a 19 inches 1U patch panel. Several FMC3 can be connected to the same patch panel. The final number has to be decided. Timing inputs and analog outputs can be connected to the patch panel via SMA coaxial connectors. Next to each SMA connector, the indicate that a signal is present either at an input, or at an output.

In addition to the MDR connector, two LEDs are present on the FMC3. One is to indicate that the FPGA is correctly configured for FMC3 card. The second one is to indicate that the patch panel is correctly connected.

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[1]Mini Delta Ribbon (available from 3M, AMPHENOL, HARTING)

References

[1] ANSI/VITA. American national standard for fpga mezzanine card (fmc) standard ansi/vita 57.1-2008, 2008.

[2] National Instruments. NI 6731/6733 Specifications, 2007.