FMC3 HDL Functional Specification

Matthieu Cattin

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Abstract

FMC3 is a 4-channel 16-bit 10Ms/s DAC board in FMC (FPGA Mezzanine Card [1]) form-factor. This document describes the HDL related to the FMC3 card. For more information on hardware related specification, see *FMC3 functional specification*.

History of versions

Version	Date	Author(s)	Changes
1.0	10-20-2009	mcattin	First draft of functional specifications.
1.1	10-21-2009	mcattin	Minor corrections after internal cern review.
1.2	10-22-2009	mcattin	Remove ”abort” trigger input from functional specifications.
1.3	10-26-2009	mcattin	Add a revision history.

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1 Features

- 4 single-ended analog output channels
- Output voltage range : +/-10V (50 ohms)
- 16-bit DACs
- Up to 10MS/s
- 1 external clock input (single-ended)
- 1 start input (TTL)
- 1 pause input (TTL)
- Each channel can store up to 32 waveform.
- Memory/channel is determined by FMC carrier [3] [2].
- Analog outputs auto-calibration.
- I^2C EEPROM to store IPMI information and DACs calibration factors
- 2 modes (vectors and points)

2 General description

An FMC3 is a mezzanine card in FMC format, containing four identical analog output channels. Each channel has a 10MS/s 16-bit DAC with an output range of +/-10V. In addition, the card has two trigger inputs (start and pause) and one external clock input. Those inputs are common to the four analog channels.

3 Modes

3.1 Vector mode

The vector mode principle works as follows: a waveform stored in memory contains only a set of vectors (intermediate values to be sent to the DAC are computed on-board). A vector is made of 3 parts, one for the amplitude and two for the time :

- amplitude value (next amplitude to reach)
- step size (number of sampling clock period for a step)
- number of steps

The first 3 values of a waveform are different from the above vector type.

- total number of vectors
- repeat number (0=infinite)
- first amplitude value

Memory can store up to 32 different waveforms per channel. Each waveform will have a fixed maximum length depending on the FMC carrier card capacity [3] [2]. The carrier should provide enough memory for at least 8000 vectors per waveform.

Each channel has a register allowing users to select the waveform to be played on next start pulse.

One mask register per channel allows to selectively enable the 32 waveforms. If a waveform is selected but disabled in the mask, the start trigger is ignored.

In vector mode, the sampling frequency is fixed (10MS/s).

All digital values sent to the DACs are computed inside the FMC carrier from the vectors in memory.

3.2 Point mode

In addition to the vector mode, a point mode will also be implemented. In this case, all values to be sent to the DAC will be stored in memory.

A table describes a set of waveforms. Each waveform is defined by:

- An address pointer.
- The waveform size.
- A repetition number.
- The next waveform to play (if any).

The maximum number of waveform is 20 (to be confirmed). Waveforms can be chained using the "Next waveform to play" field.

In point mode, sampling clock can be internal or external. In case of an internal clock, the frequency can be selected over a wide range. It will depend on the carrier clock distribution scheme [3] [2].

4 Triggers

The FMC3 has two trigger inputs. A start and a pause input. They can be used in many different ways.

The first and simplest case uses only the start input. The selected waveform is generated when a start pulse arrives. Generation continues until the end of the waveform.

The "pause" trigger input is used to suspend the waveform generation. After a pause pulse, a new start pulse is needed in order to continue waveform generation.

Moreover, in vector mode, it is possible to program a pause inside a waveform. This is done by means of a special vector called "internal pause". To continue the waveform generation a start pulse is needed, as for the pause trigger input.

For test purposes, all the trigger inputs are also emulated in software by writing in a register.

Trigger inputs polarity is selectable via a register (TTL or $\overline{TTL}$).

5 Test

Some test features will be implemented to easily test hardware during development and installation. The two test features are:

- Test waveform generation (saw-tooth).
- Direct digital value to DAC.

References

[1] ANSI/VITA. American national standard for fpga mezzanine card (fmc) standard ansi/vita 57.1-2008, 2008.

[2] CERN. PCIe FMC carrier OHR project, 2009.

[3] CERN. VME FMC carrier OHR project, 2009.