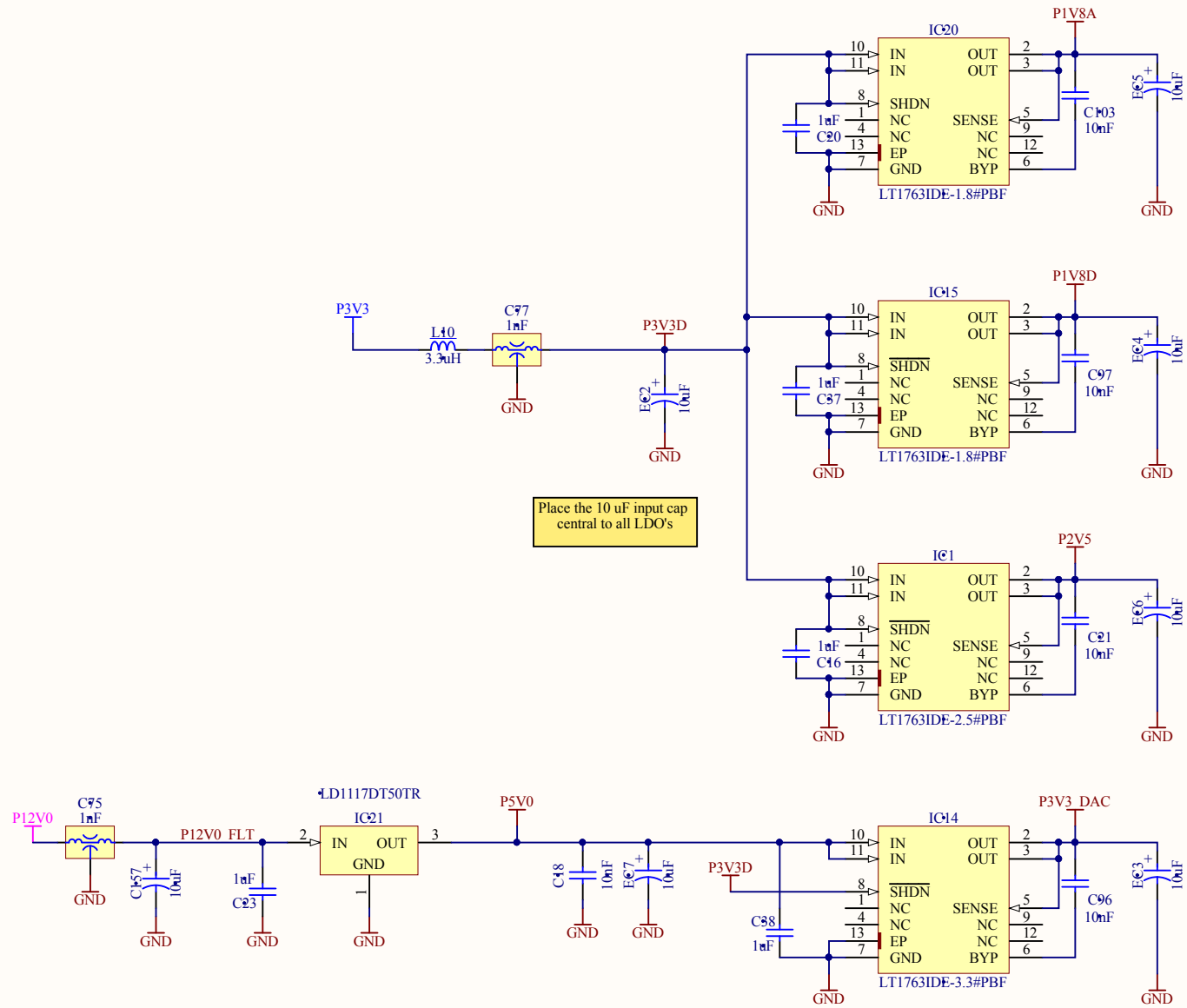


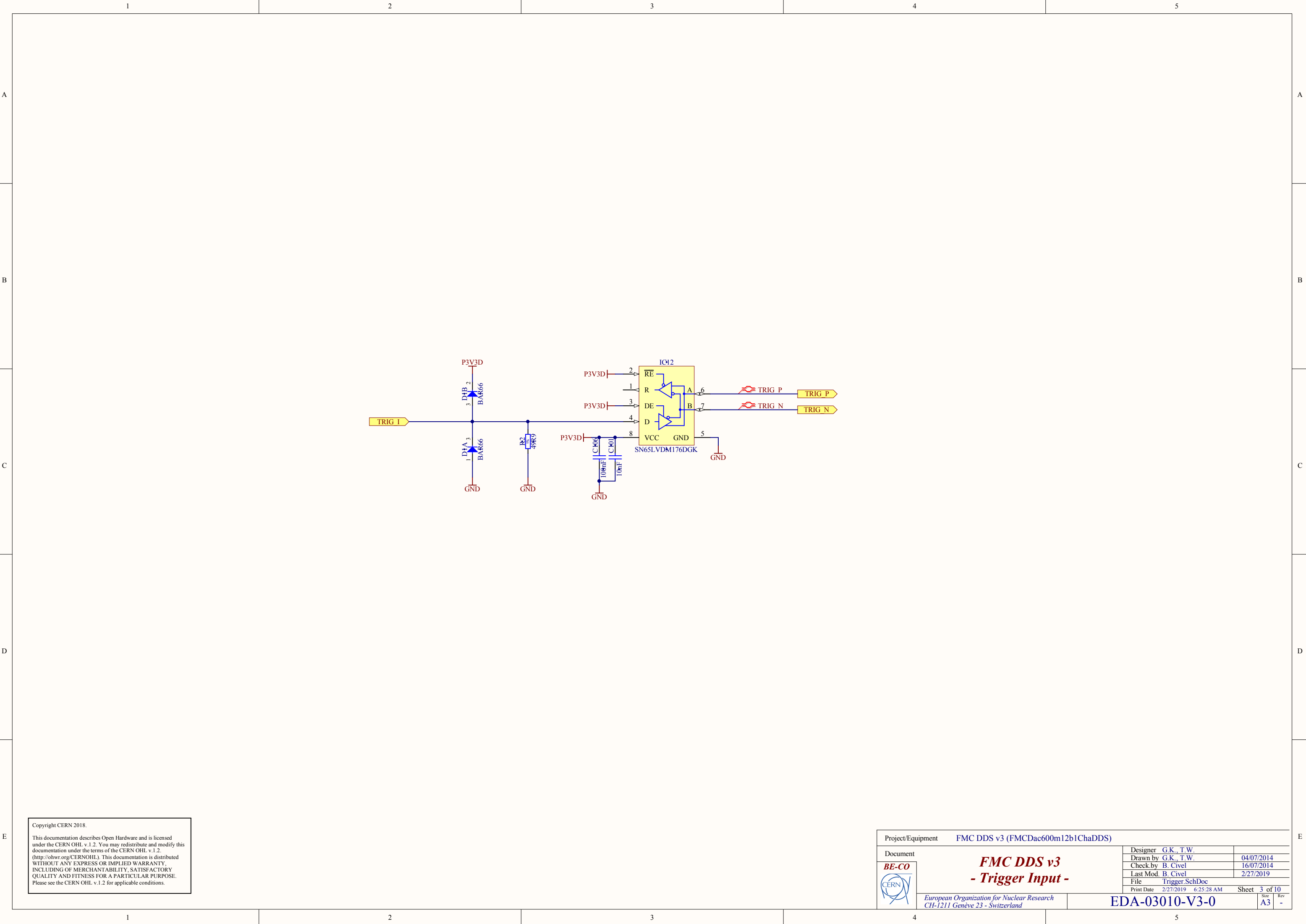
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Place all LT1763's on 100 mm^2 (min) pour. Device pad should have multiple (>6) 0.5 mm vias connecting to all ground planes, and be soldered to pour

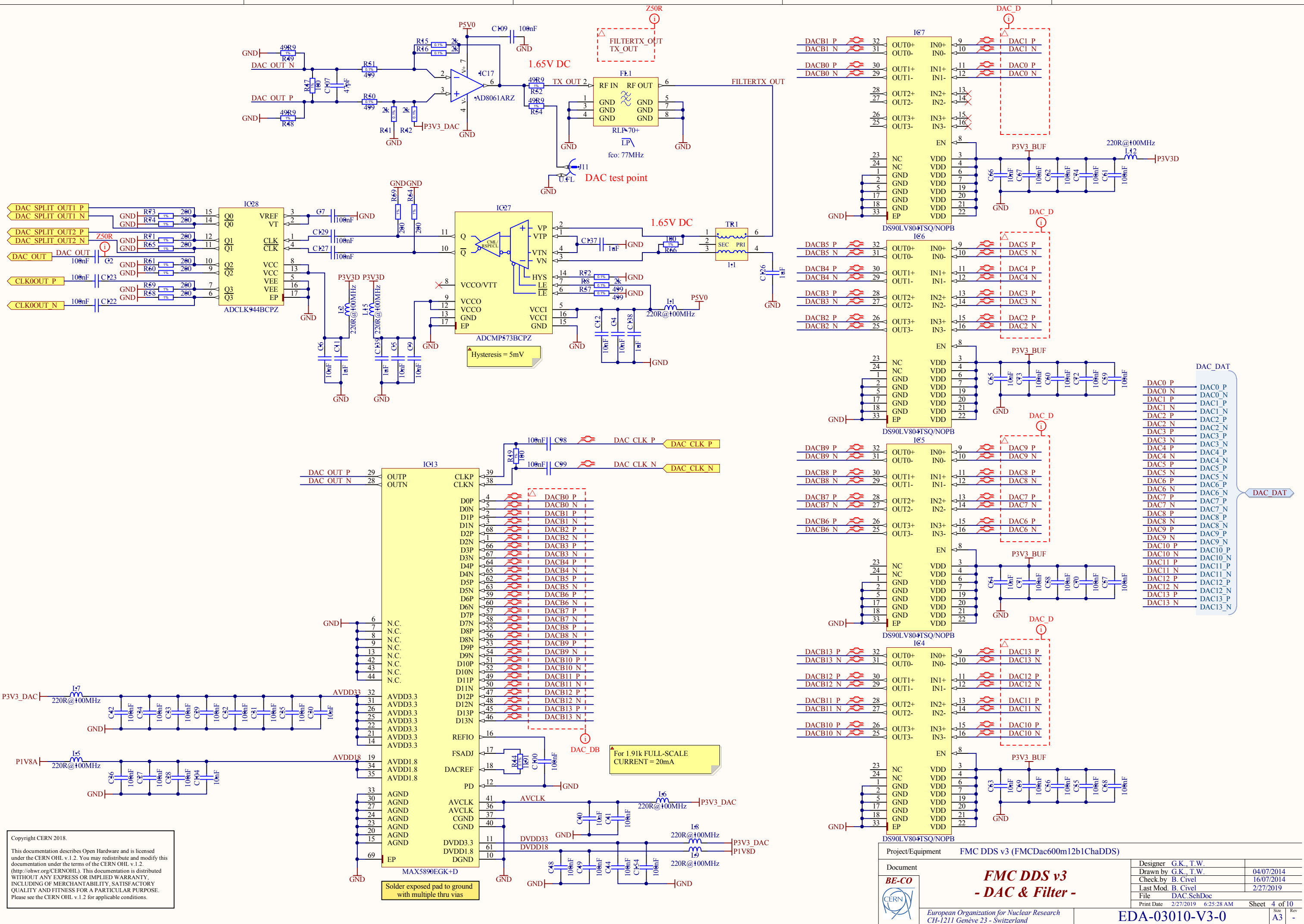
Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)			
Document	<div>BE-CO</div> <div>CERN</div> <div>European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland</div>	Designer	G.K., T.W.		
		Drawn by	G.K., T.W.	04/07/2014	
		Check by	B. Civel	16/07/2014	
		Last Mod.	B. Civel	2/27/2019	
File		Power.SchDoc			
Print Date		2/27/2019	6:25:27 AM	Sheet 2 of 10	
Size		A3	Rev -		
		EDA-03010-V3-0			



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Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
<div>Document</div> <div></div>	Designer		G.K., T.W.
	Drawn by		G.K., T.W.
	Check by		B. Civel
	Last Mod.		B. Civel
	File		Trigger.SchDoc
Print Date		2/27/2019 6:25:28 AM	Sheet 3 of 10
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-03010-V3-0	
Size		A3	Rev -





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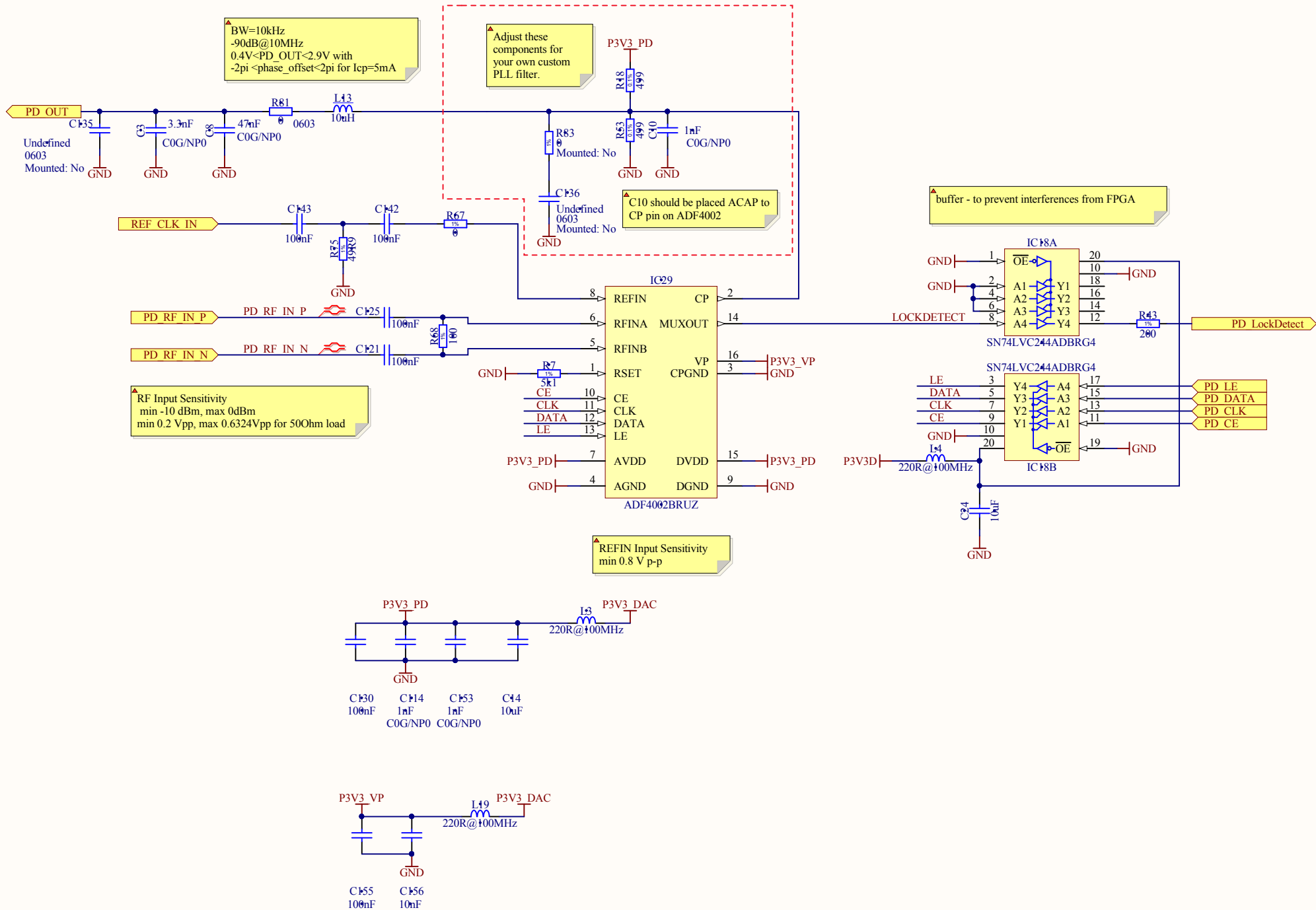
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Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
Document		Designer	G.K., T.W.
<div>BE-CO</div> <div>CERN</div>		Drawn by	G.K., T.W.
		Check by	B. Civel
		Last Mod.	B. Civel
		File	Phase detector.SchDoc
		Print Date	2/27/2019 6:25:28 AM
		Sheet	6 of 10
		Size	A3
		Rev	-

FMC DDS v3
- Phase Detector -

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-03010-V3-0

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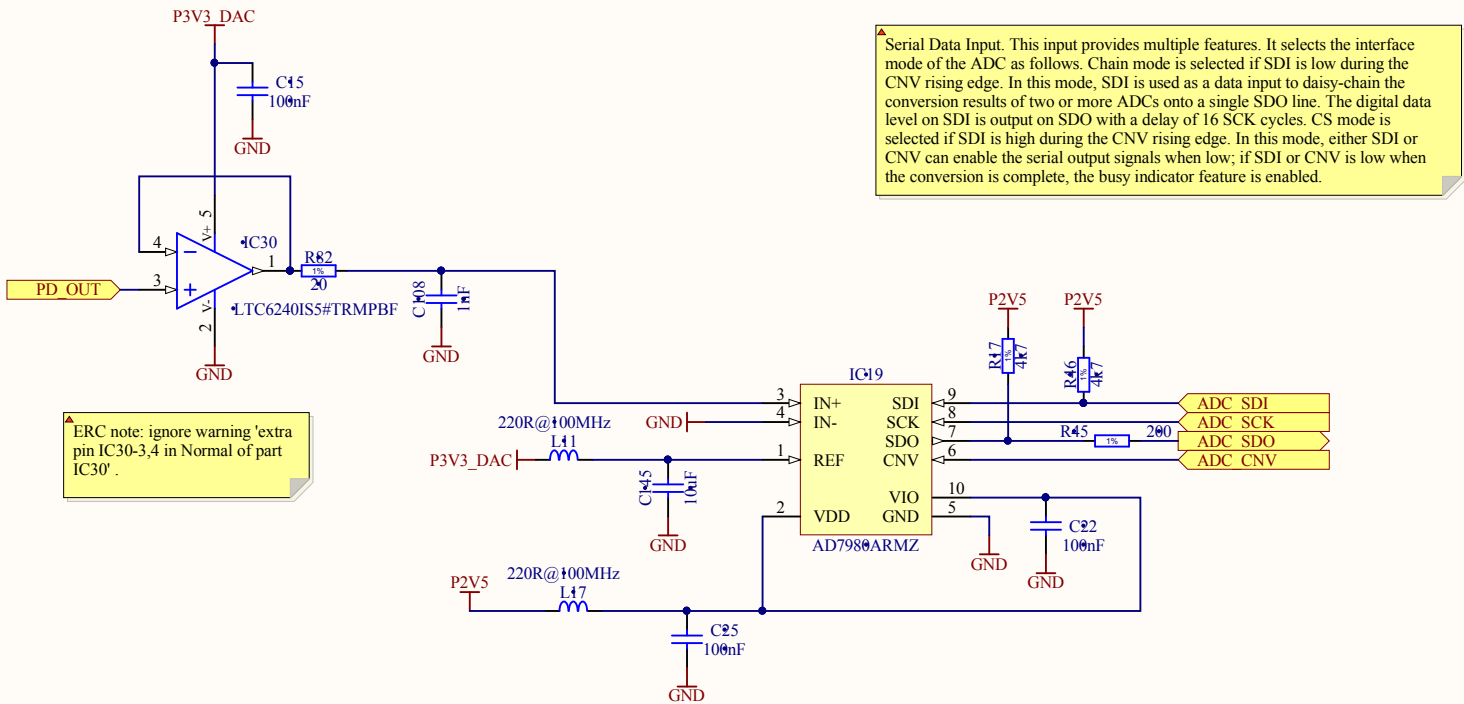
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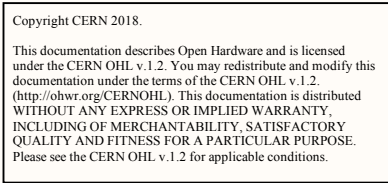
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



Project/Equipment		FMC DDS v3(FMCDac600m12b1ChaDDS)	
Document		Designer	G.K., T.W.
<div>BE-CO</div> <div></div> <div><i>European Organization for Nuclear Research</i> CH-1211 Genève 23 - Switzerland</div>		Drawn by	G.K., T.W.
		Check by	B. Civel
		Last Mod.	B. Civel
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		Sheet	7 of 10
		Size	A3
		Rev	-

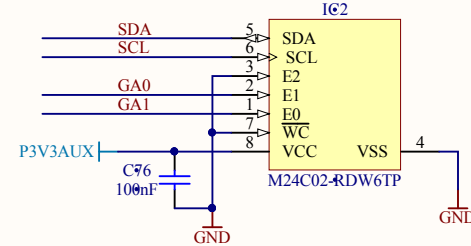
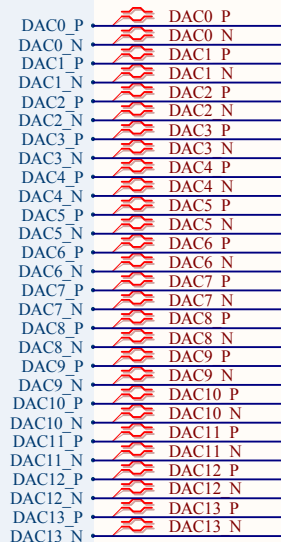
FMC DDS v3
- ADC -

EDA-03010-V3-0

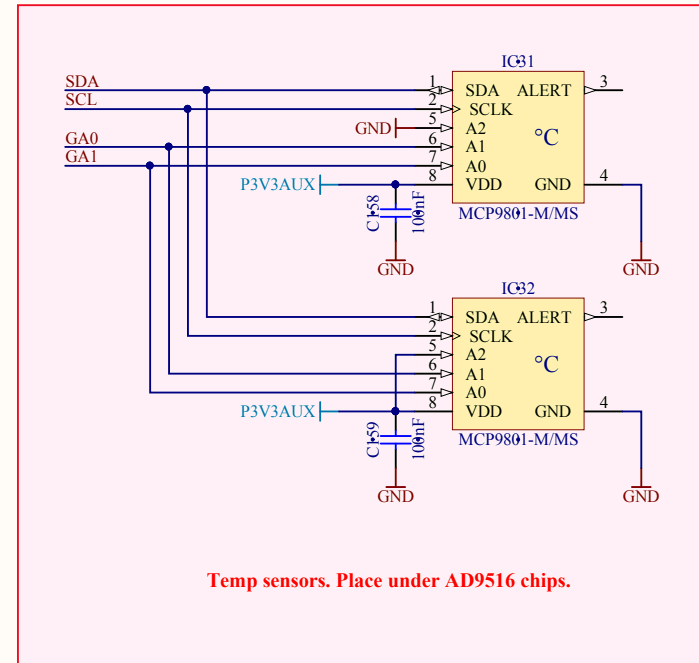


Project/Equipment		FMC DDS v3 (FMCDDac600m12b1ChaDDS)	
Document		Designer	G.K., T.W.
 <div style="text-align: center;"> <p>FMC DDS v3</p> <p>- VCXO & PLL, WR Clock -</p> </div>		Drawn by	G.K., T.W.
		Check by	B. Civel
		Last Mod.	B. Civel
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		Print Date	2/27/2019 6:25:29 AM
 <p>European Organization for Nuclear Research CH-1211, Genève 23 - Switzerland</p>		Sheet	8 of 10
		Size	A3
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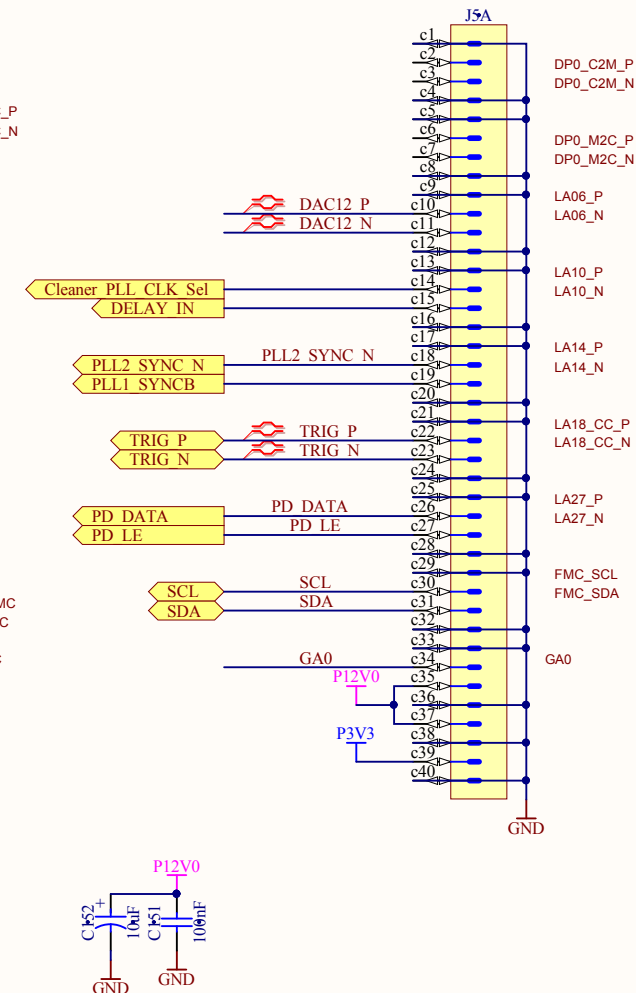
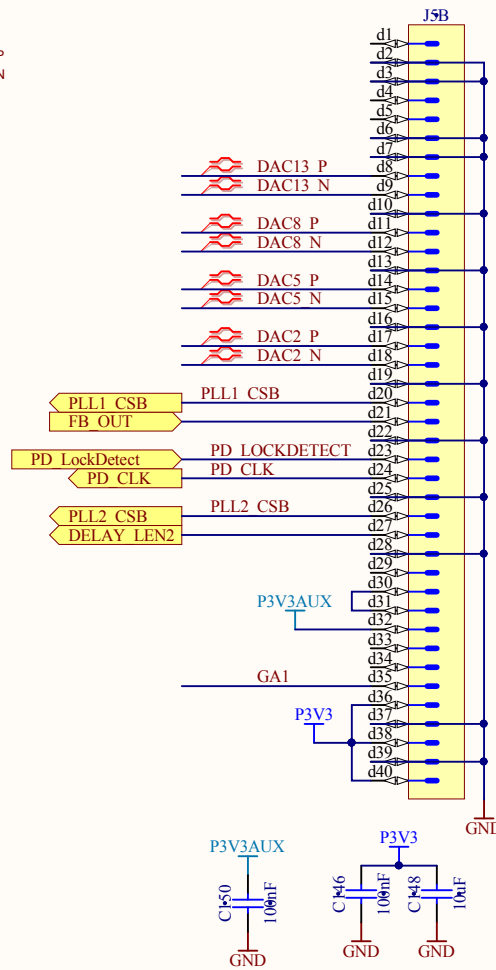
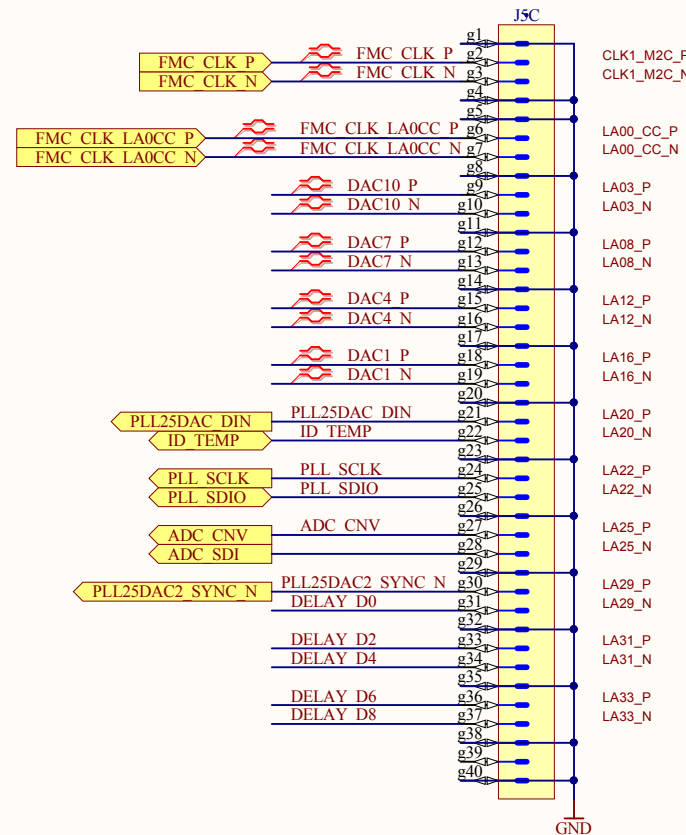
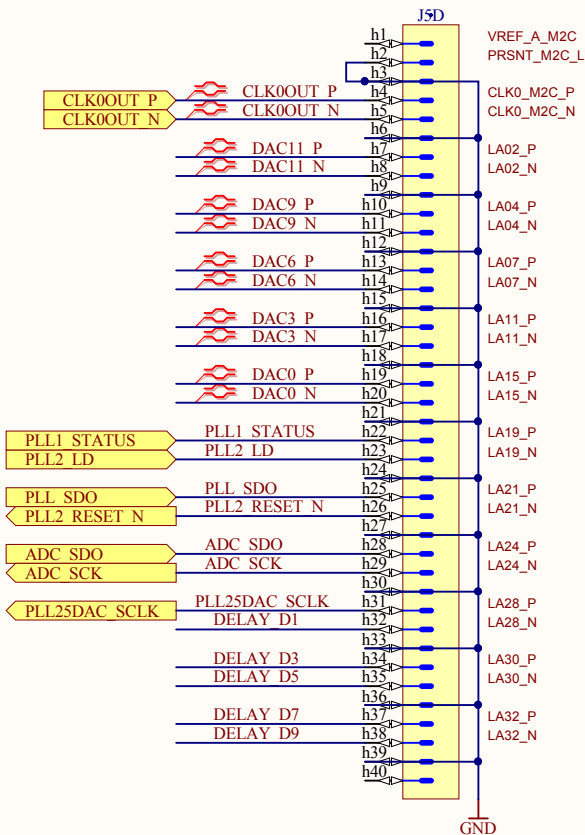
DAC_DAT



Note on GA0, GA1 pins; they are connected IN REVERSE to the EEPROM address pins:
GA0~>A1/E1
GA1~>A0/E0.
This looks awkward, but so says the VITA FMC standard.



Temp sensors. Place under AD9516 chips.



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Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
Document		FMC DDS v3 - FMC Connector & EEPROM -	
Designer		G.K., T.W.	04/07/2014
Check by		B. Civel	16/07/2014
Last Mod.		B. Civel	2/27/2019
File		FMC_SchDoc	
Print Date		2/27/2019 6:25:29 AM	Sheet 9 of 10
Size		A3	Rev -

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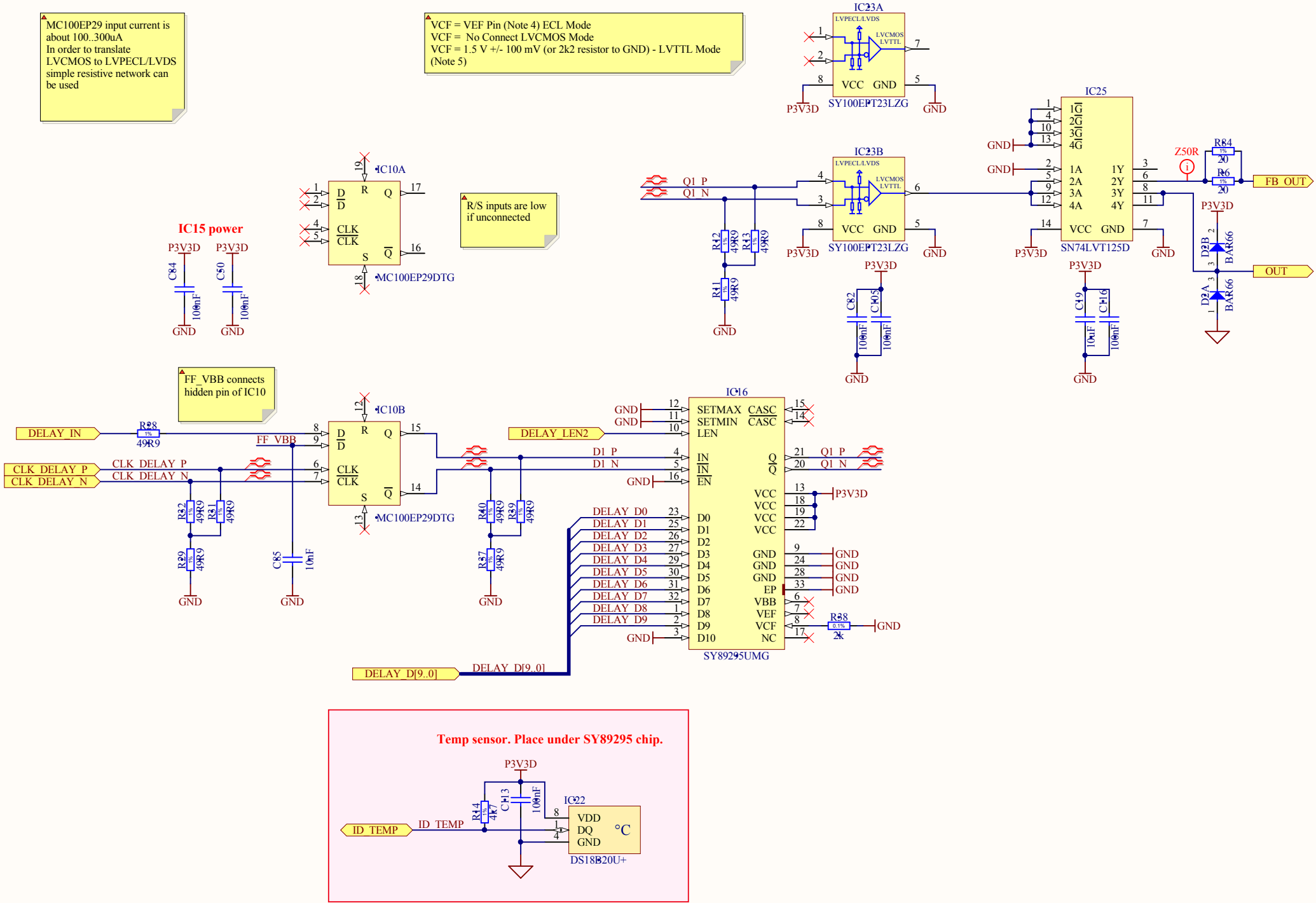
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▲ MC100EP29 input current is about 100...300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used

▲ VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV (or 2k2 resistor to GND) - LVTTTL Mode (Note 5)



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Project/Equipment		FMC DDS v3 (FMCDac600m12b1ChaDDS)	
Document		Designer G.K., T.W.	
<div>BE-CO</div> <div></div>		Drawn by G.K., T.W.	04/07/2014
		Check by B. Civel	16/07/2014
		Last Mod. B. Civel	2/27/2019
		File delay.SchDoc	
Print Date 2/27/2019 6:25:29 AM		Sheet 10 of 10	Size A3 Rev -
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-03010-V3-0	