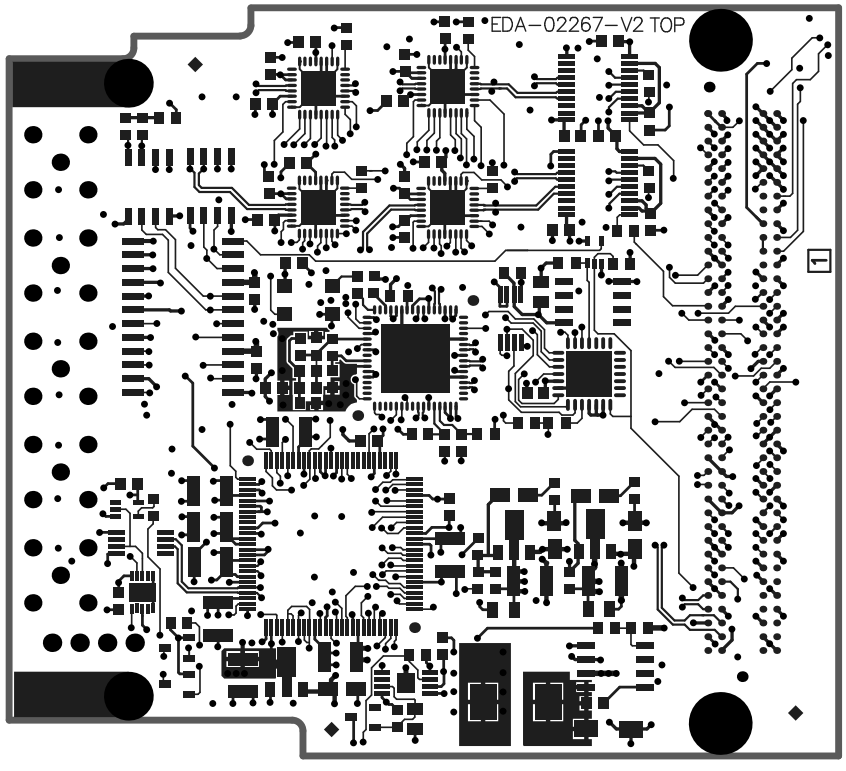


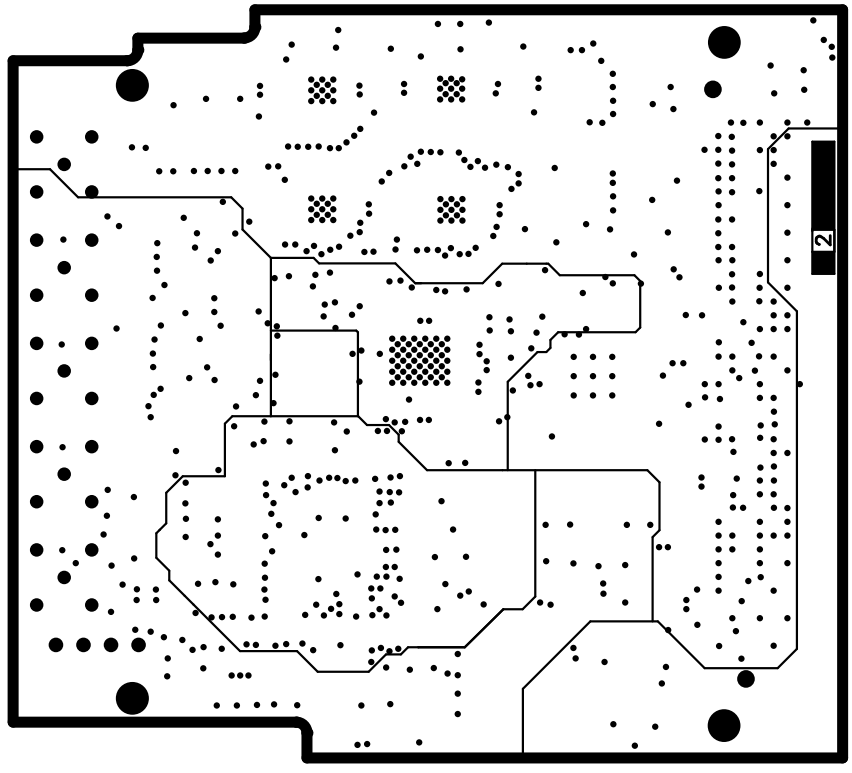
CERN

Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:42 PM

Top Layer

1

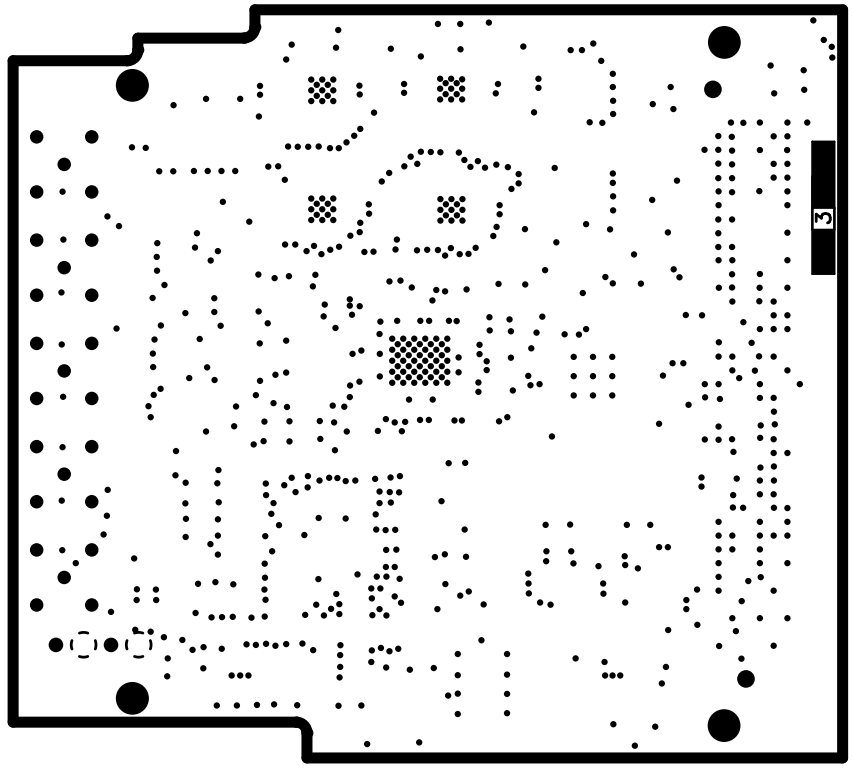


Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:42 PM

plane L2 PWR

[redacted] 2 [redacted]

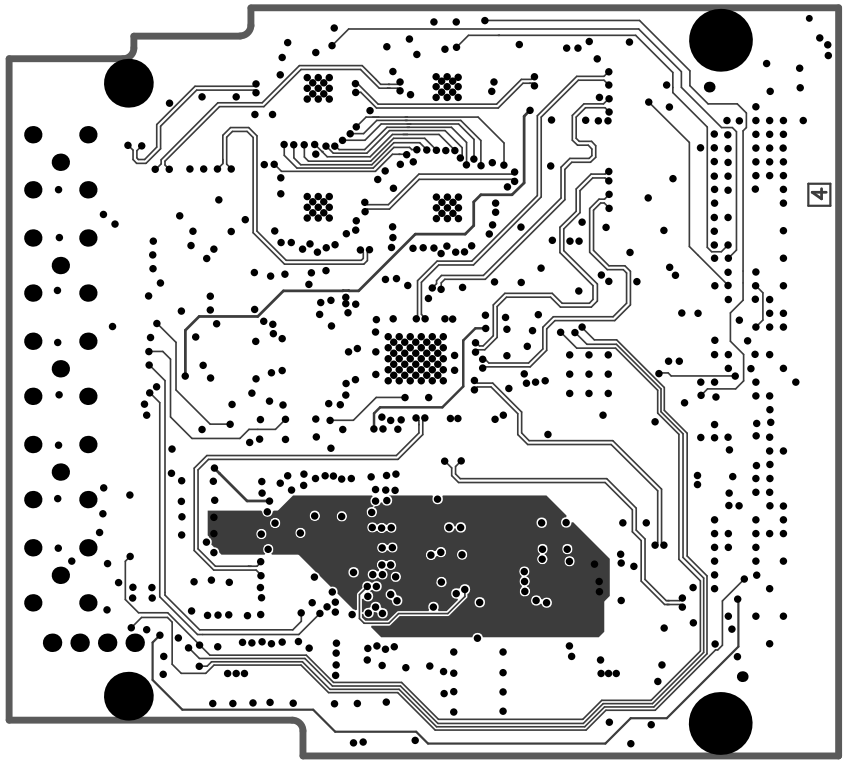


Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:42 PM

Plane L3 3P3V / 3P3V_TDC

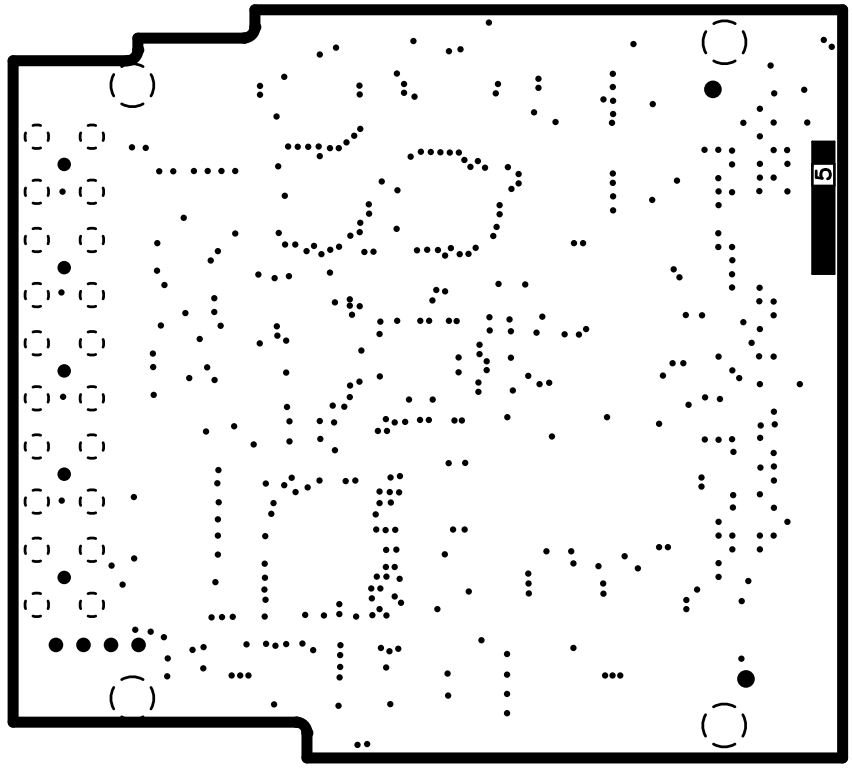
3



Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:42 PM

4



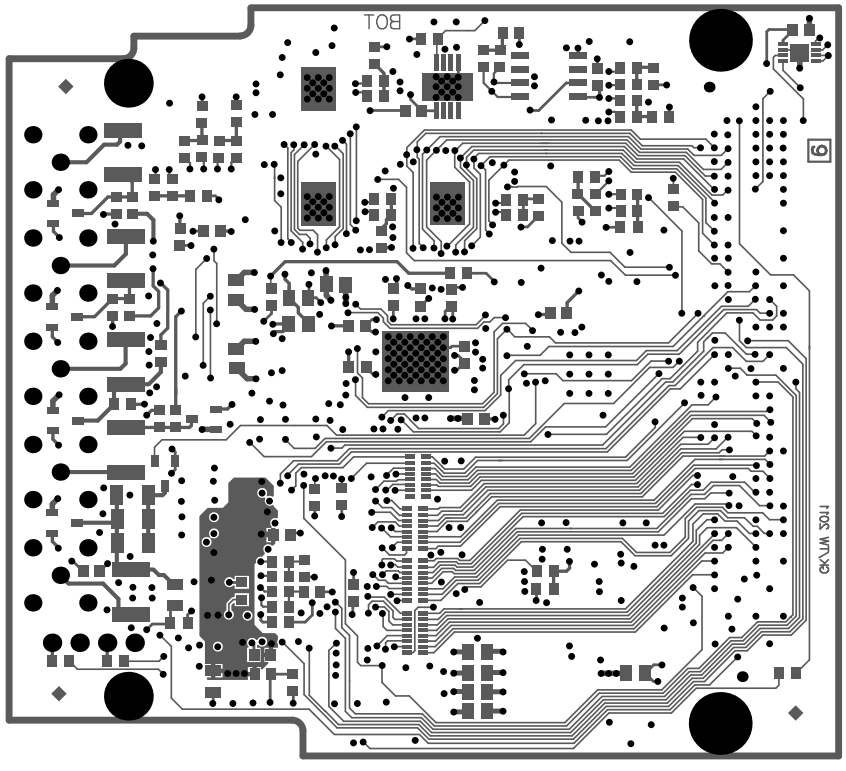
CERN

Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:42 PM

Plane L5 GND

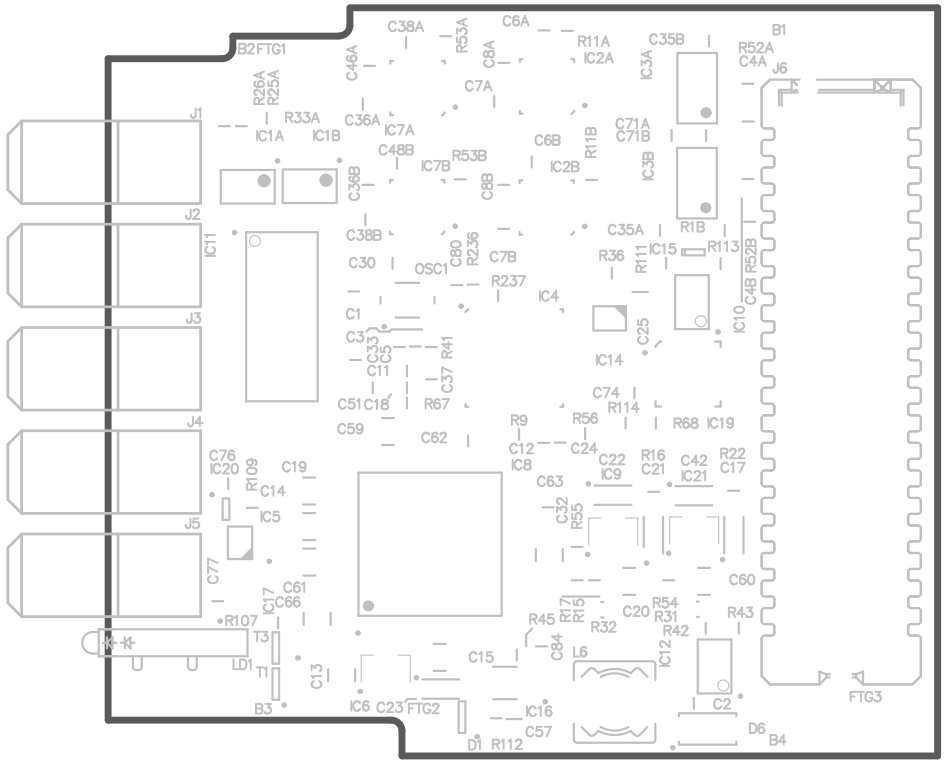
5



Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:43 PM

Bottom Layer



Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

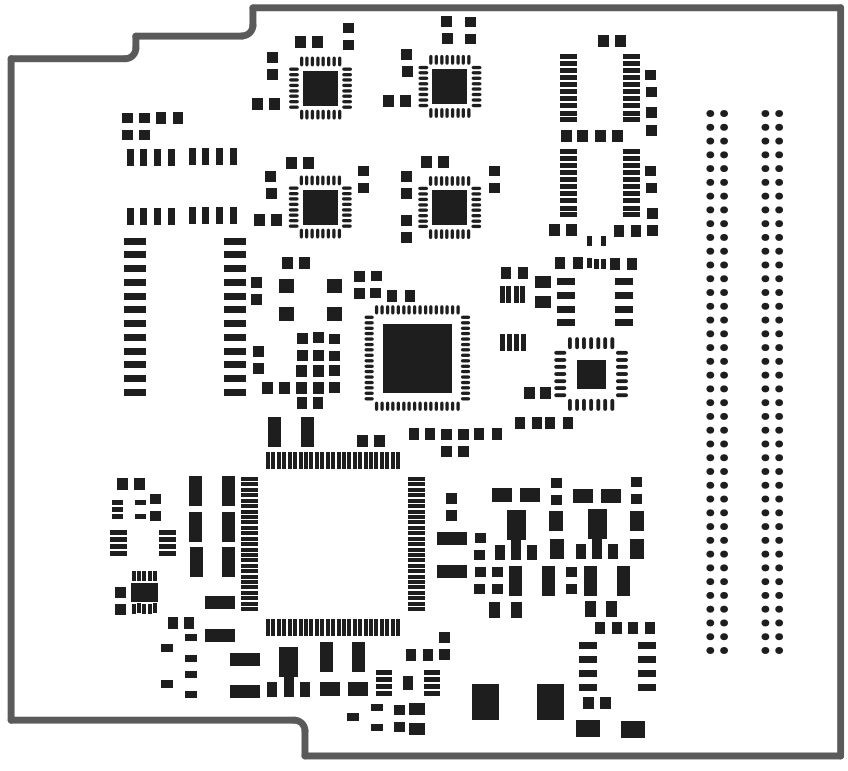
Print Date 5/5/2011 2:37:43 PM

Top Overlay

Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:43 PM

Bottom Overlay



CERN

Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:43 PM

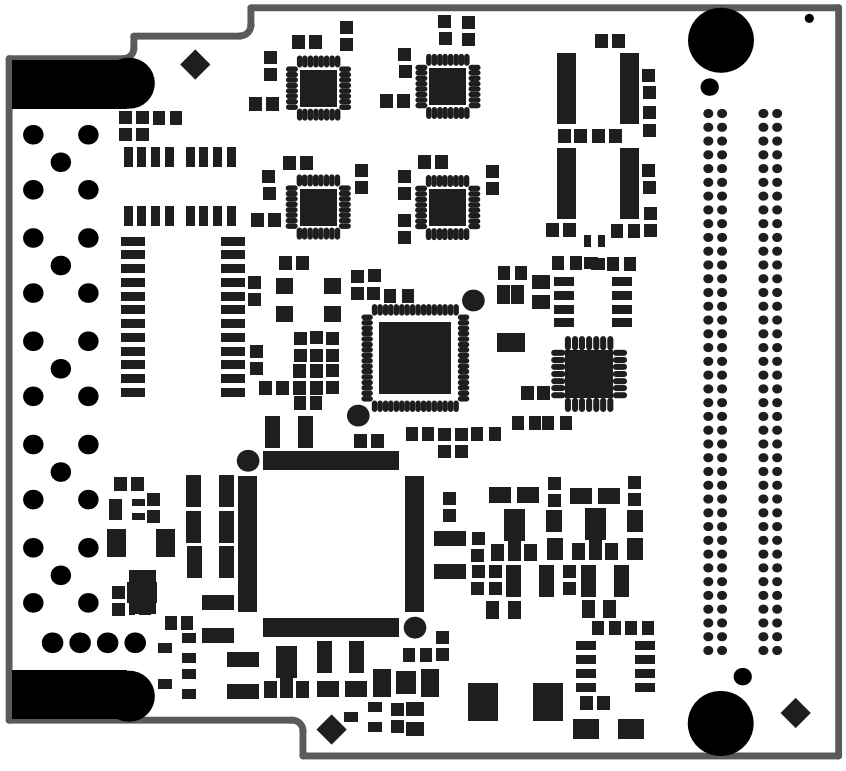
Top Paste

CERN

Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:43 PM

Bottom Paste

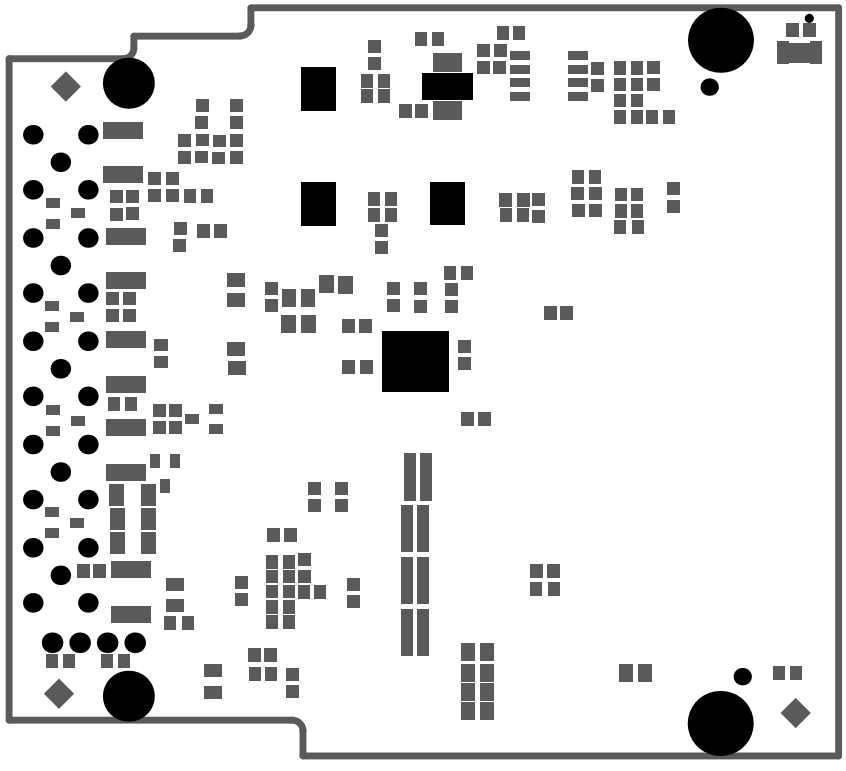


CERN

Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:43 PM

Top Solder



Number	EDA-02267-V1
Drawn By	T. WLOSTOWSKI
DATE	12-03-2010
MOD.	-

Print Date 5/5/2011 2:37:43 PM

Bottom Solder

U_power_supply
power_supply.SchDoc
RESETn

P3V3
C74 100nF 0603
C84 100nF 0603
GND

16-bit I/O Port Expander With Serial Interface
IC19
MCP23S17-E/ML
EXT_CSn
SCLK
SDI
SDO
R68 100 0603 1%
RESETn
P3V3
GND
CS
SCK
SI
SO
A2
A1
A0
RESET
INTB
INTA
VDD
VSS
EP
GPA7
GPA6
GPA5
GPA4
GPA3
GPA2
GPA1
GPA0
GPB7
GPB6
GPB5
GPB4
GPB3
GPB2
GPB1
GPB0
TERM_ENABLE
PLL_STATUS
PLL_LD
PLL_REFMON
TRIG_SEL
LED1
LED2
OUTPUT_ENABLE

U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
DELAY_D[9..0]
DELAY_LEN1
DELAY_LEN2
DIN1
DIN2
CLK1_P
CLK1_N
CLK2_P
CLK2_N
OUT1
OUT2
TDC_CAL_START_P
TDC_CAL_START_N

U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
DELAY_D[9..0]
DELAY_LEN3
DELAY_LEN4
DELAY_LEN1
DELAY_LEN2
DIN3
DIN4
DIN1
DIN2
CLK1_P
CLK1_N
CLK2_P
CLK2_N
TDC_CAL_START_N
TDC_CAL_START_P
OUT1
OUT2

U_OUTPUT_BUFFER
OUTPUT_BUFFER.SchDoc
RESETn
OUTPUT_ENABLE
RESET
OUTPUT_ENABLE
IN1
IN2
IN3
IN4
OUT1
OUT2
OUT3
OUT4
CALIB_OUT1
CALIB_OUT2
CALIB_OUT3
CALIB_OUT4
J1 LEMO 00 GND
J2 LEMO 00 GND
J3 LEMO 00 GND
J4 LEMO 00 GND

VREF MUST BE 2.5V or 3.3V

FMC connector.SchDoc
U_FMC connector
DELAY_D[9..0]
DIN1
DIN2
DIN3
DIN4
DELAY_LEN1
DELAY_LEN2
DELAY_LEN3
DELAY_LEN4

U_INPUT_LOGIC
INPUT_LOGIC.SchDoc
J5 LEMO 00 GND
IN
TDC_STOP_P
TDC_STOP_N
TRIG_FPGA
TRIG_SEL
TRIG_OUT_LVTTL
TERM_ENABLE

U_TDC
TDC.SchDoc
RESETn
TDC_RESETn
TDC_CAL_START_P
TDC_CAL_START_N
TDC_STOP_P
TDC_STOP_N
TDC_CAL_STOP1
TDC_CAL_STOP2
TDC_CAL_STOP3
TDC_CAL_STOP4
TDC_START_DIS
TDC_STOP_DIS
TDC_ERR
TDC_EMPTY_FLAG
TDC_ALUTRIGGER
TDC_START_P
TDC_START_N
TDC_OEN
TDC_CSN
TDC_RDN
TDC_WRN
TDC_ADR[3..0]
TDC_D[27..0]
TDC_REF_CLK

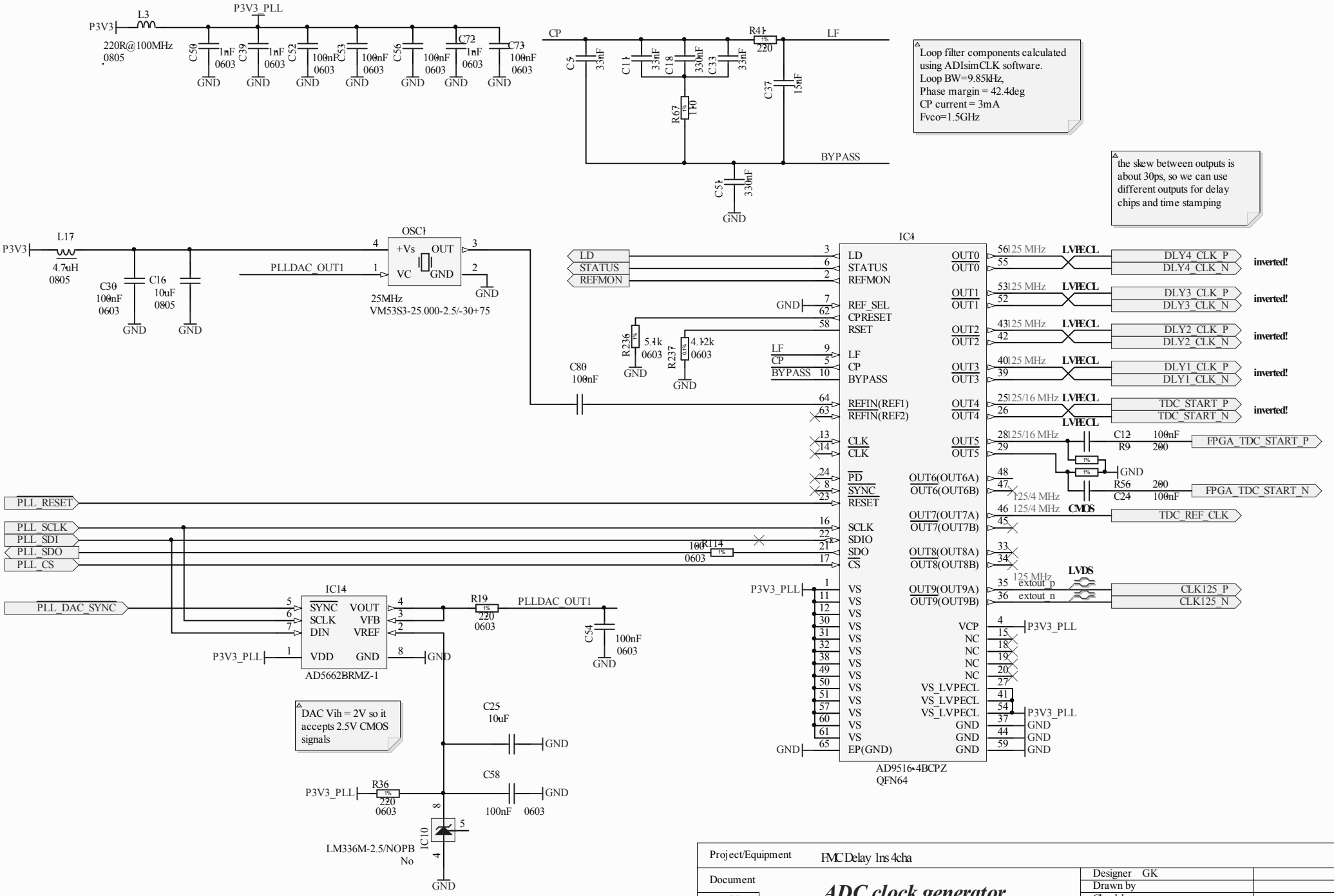
U_LED_MEM
LED_MEM.SchDoc
ONEWIRE
SDA
SCL
GA0
GA1
LED1
LED2

U_clock_generator
clock_generator.SchDoc
DLY1_CLK_P
DLY1_CLK_N
DLY2_CLK_P
DLY2_CLK_N
DLY3_CLK_P
DLY3_CLK_N
DLY4_CLK_P
DLY4_CLK_N
RESETn
PLL_RESET
TDC_START_P
TDC_START_N
TDC_REF_CLK
CLK125_P
CLK125_N
PLL_DAC_SYNC
PLL_SCLK
PLL_CS
PLL_SDO
PLL_SDI
PLL_LD
PLL_STATUS
PLL_REFMON
LD
STATUS
REFMON
SCLK
SDO
SDI
FPGA_TDC_START_P
FPGA_TDC_START_N
TRIG_OUT_LVTTL
EXT_CSn
TRIG_FPGA

Working mode:
TDC in R-Mode, 31.25 MHz reference (125 MHz / 4)
START: 7.8125 MHz (125 MHz / 16)
STOP1: trigger
27ps resolution.

Calibration mode:
TDC in I-Mode,
LVTTL inputs, 10MHz max
START: 10MHz clock delivered to TDC_CAL_START
STOP: buffer output
81ps resolution

Project/Equipment	FMC Delay 1ns 4cha
Document	**FMC delay top**
Designer	GK
Drawn by	GK
Check by	-
Last Mod.	- 5/5/2011
File	FMC_Delay_1ns_4Cha.SchDoc
Print Date	5/5/2011 2:37:47 PM Sheet 1 of 9
BE-CO	European Organization for Nuclear Research, CH-1211 Geneve 23 - Switzerland
EDA-XXXXX-VX-X	Size A3 Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	*ADC clock generator*	Designer GK	
		Drawn by	
		Check by -	-
		Last Mod. -	5/5/2011
		File clock_generator.SchDoc	
		Print Date 5/5/2011 2:37:47 PM	Sheet 2 of 9
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4	Rev -

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.

VREF MUST BE 2.5V or 3.3V

DELAY_D[9..0] DELAY_D[9..0]

TDC_ADR[3..0] TDC_ADR[3..0]
TDC_D[27..0] TDC_D[27..0]

H

J6D

	h1		
GND	h2		
GND	h3		
FPGA_TDC_START_P	h4		
FPGA_TDC_START_N	h5		
GND	h6		
TDC_D7	h7		
TDC_D6	h8		
GND	h9		
TDC_D3	h10		
TDC_D1	h11		
GND	h12		
TDC_D14	h13		
TDC_D15	h14		
GND	h15		
TDC_D22	h16		
TDC_D23	h17		
GND	h18		
TDC_ERR	h19		
ONEWIRE	h20		
GND	h21		
TDC_ADR2	h22		
TDC_ADR3	h23		
GND	h24		
DIN2	h25		
DIN1	h26		
GND	h27		
DELAY_LEN1	h28		
DELAY_LEN2	h29		
GND	h30		
DELAY_D9	h31		
DELAY_D8	h32		
GND	h33		
DELAY_D5	h34		
DELAY_D4	h35		
GND	h36		
DELAY_D1	h37		
DELAY_D0	h38		
GND	h39		
VADJ	h40		

G

J6G

		GND	g1
CLK125_P	CLK125_P		g2
CLK125_N	CLK125_N		g3
GND			g4
GND			g5
TRIG_OUT_LVTTL			g6
TRIG_FPGA			g7
GND			g8
TDC_D5			g9
TDC_D4			g10
GND			g11
TDC_D10			g12
TDC_D11			g13
GND			g14
TDC_D20			g15
TDC_D21			g16
GND			g17
TDC_ALUTRIGGER			g18
TDC_EMPTY_FLAG			g19
GND			g20
EXT_CSn			g21
TDC_CSN			g22
GND			g23
TDC_START_DIS			g24
TDC_STOP_DIS			g25
GND			g26
DIN4			g27
DIN3			g28
GND			g29
DELAY_LEN4			g30
DELAY_LEN3			g31
GND			g32
DELAY_D7			g33
DELAY_D6			g34
GND			g35
DELAY_D3			g36
DELAY_D2			g37
GND			g38
VADJ			g39
GND			g40

D

J6B

	d1		
GND	d2		
GND	d3		
	d4		
	d5		
GND	d6		
GND	d7		
TDC_D2	d8		
TDC_D0	d9		
GND	d10		
TDC_D12	d11		
TDC_D13	d12		
GND	d13		
TDC_D16	d14		
TDC_D17	d15		
GND	d16		
TDC_D24	d17		
TDC_D25	d18		
GND	d19		
TDC_WRN	d20		
TDC_RDN	d21		
GND	d22		
TDC_OEN	d23		
PLL_DAC_SYNC_N	d24		
GND	d25		
PLL_SCLK	d26		
PLL_CS	d27		
GND	d28		
TDI	d29		
TDO	d30		
P3V3_AUX	d31		
	d32		
	d33		
GA1	d34		
P3V3	d35		
GND	d36		
P3V3	d37		
GND	d38		
P3V3	d39		
	d40		

C

J6A

GND	c1		
	c2		
	c3		
GND	c4		
GND	c5		
	c6		
	c7		
GND	c8		
GND	c9		
TDC_D8	c10		
TDC_D9	c11		
GND	c12		
GND	c13		
TDC_D18	c14		
TDC_D19	c15		
GND	c16		
GND	c17		
TDC_D26	c18		
TDC_D27	c19		
GND	c20		
GND	c21		
TDC_ADR0	c22		
TDC_ADR1	c23		
GND	c24		
GND	c25		
PLL_SDI	c26		
PLL_SDO	c27		
GND	c28		
GND	c29		
SCL	c30	SCL	
SDA	c31	SDA	
GND	c32		
GND	c33		
GA0	c34	GA0	
P12V0	c35		
GND	c36		
P12V0	c37		
GND	c38		
P3V3	c39		
GND	c40		

B1 B4

GND

B1 ... B4
screw holes for mounting the FmcAdc to the carrier board.

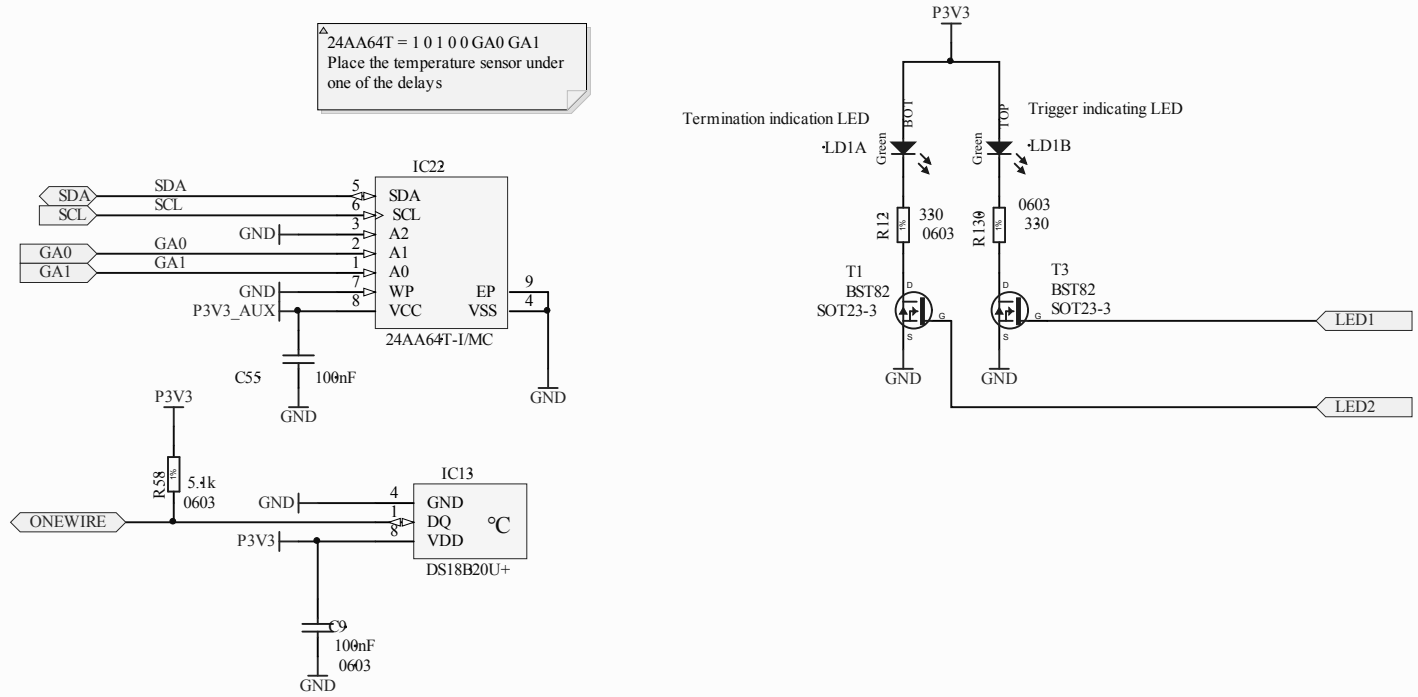
B2 B3

GND

FTG1 FTG2 FTG3 FTG6 FTG5 FTG4

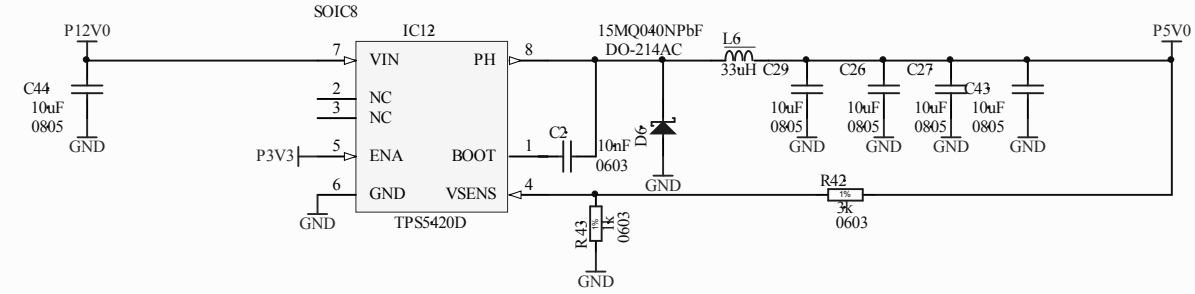
FTG1 ... FTG6
Reference points for the component mounting machine.

Project/Equipment	FMC Delay 1ns 4cha
Document	**FMC Connector**
Designer	Greg Kasprowicz,
Drawn by	Greg Kasprowicz 10/07/2010
Check by	M.C., T.W., E.B. -
Last Mod.	- 5/5/2011
File	FMC connector.SchDoc
Print Date	5/5/2011 2:37:47 PM Sheet 3 of 9
European Organization for Nuclear Research *CH-1211 Geneve 23 - SwitzerLA_Pd*	EDA-XXXXX-XX-X Size A3 Rev -



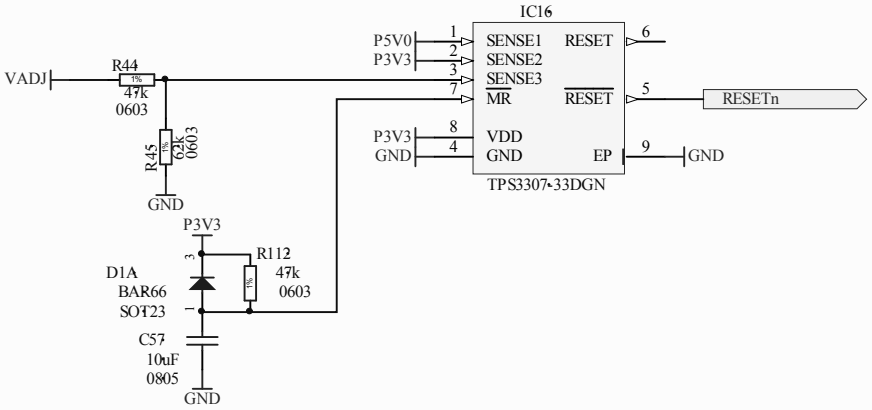
Project/Equipment	FMC Delay 1ns 4cha		
Document	***LED and MEMORY***	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check by -	-
		Last Mod. -	5/5/2011
		File LED_MEM.SchDoc	
		Print Date 5/5/2011 2:37:47 PM	Sheet 4 of 9
European Organization for Nuclear Research *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4	Rev -

P5V0 is used to power TDC chip. It is then used to supply LDO regulators, so it doesn't need to be very clean and stable

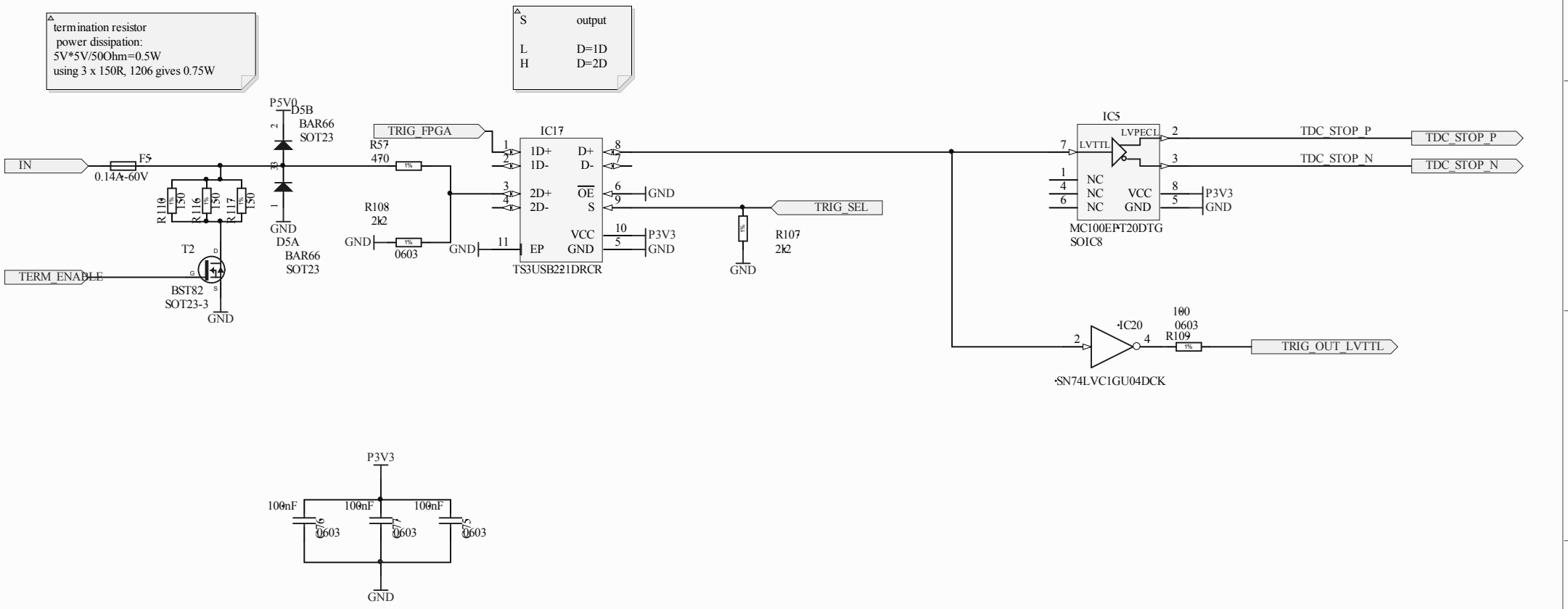


TPS3307-33D thresholds

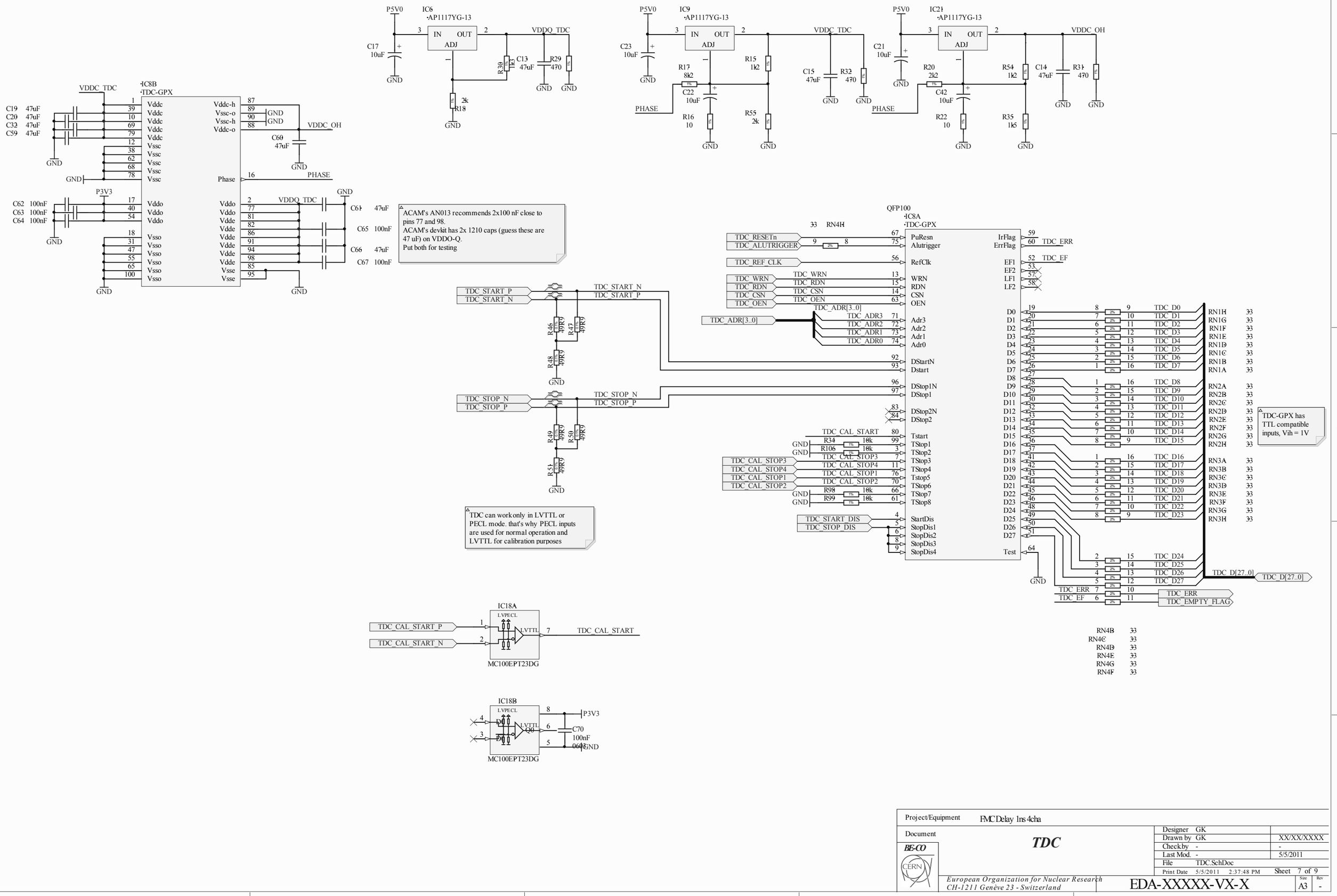
sense1	sense2	sense3
4.55V	2.93V	1.25V



Project/Equipment	FMC Delay 1ns 4cha		
Document	**Power supplies** -	Designer GK	
		Drawn by	
		Check by -	-
		Last Mod. -	5/5/2011
		File power_supply.SchDoc	
		Print Date 5/5/2011 2:37:48 PM	Sheet 5 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	**Input logic**	Designer GK	
	-	Drawn by	
		Check by -	-
		Last Mod. -	5/4/2011
		File INPUT_LOGIC.SchDoc	
		Print Date 5/5/2011 2:37:48 PM	Sheet 6 of 9
BE-CO CERN	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4 / Rev -


P5V0
IC6
AP1117YG-13
IN
OUT
ADJ
C17 10uF
R30 1k2
C13 47uF
R29 470
VDDQ_TDC
R18 2k
IC9
AP1117YG-13
C23 10uF
R17 8k2
C22 10uF
R16 10
R15 1k2
R55 2k
C15 47uF
R32 470
VDDC_TDC
PHASE
IC21
AP1117YG-13
C21 10uF
R20 2k2
C42 10uF
R22 10
R54 1k2
R35 1k5
C14 47uF
R31 470
VDDC_OH
GND
IC8B
TDC-GPX
Vddc
Vddc-h
Vssc-o
Vssc-h
Vddc-o
Vssc
Phase
Vddo
Vsso
Vsse
C19 47uF
C20 47uF
C32 47uF
C59 47uF
C60 47uF
P3V3
C62 100nF
C63 100nF
C64 100nF
C61 47uF
C65 100nF
C66 47uF
C67 100nF
ACAM's AN013 recommends 2x100 nF close to pins 77 and 98.
ACAM's devkit has 2x 1210 caps (guess these are 47 uF) on VDDO-Q.
Put both for testing
QFP100
IC8A
TDC-GPX
RN4H
33
TDC_RESETn
TDC_ALUTRIGGER
TDC_REF_CLK
TDC_WRN
TDC_RDN
TDC_CSN
TDC_OEN
TDC_ADR[3..0]
PuResn
Alutrigger
RefClk
WRN
RDN
CSN
OEN
Adr3
Adr2
Adr1
Adr0
DStartN
Dstart
DStop1N
DStop1
DStop2N
DStop2
Tstart
TStop1
TStop2
TStop3
TStop4
Tstop5
TStop6
TStop7
TStop8
StartDis
StopDis1
StopDis2
StopDis3
StopDis4
Test
IrFlag
ErrFlag
EF1
EF2
LF1
LF2
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
TDC_ERR
TDC_EF
TDC_D[27..0]
TDC_EMPTY_FLAG
RN1H
RN1G
RN1F
RN1E
RN1D
RN1C
RN1B
RN1A
RN2A
RN2B
RN2C
RN2D
RN2E
RN2F
RN2G
RN2H
RN3A
RN3B
RN3C
RN3D
RN3E
RN3F
RN3G
RN3H
RN4B
RN4C
RN4D
RN4E
RN4G
RN4F
TDC-GPX has TTL compatible inputs, Vih = 1V
TDC_START_P
TDC_START_N
R46 49R9
R47 49R9
R48 49R9
TDC_STOP_N
TDC_STOP_P
R49 49R9
R50 49R9
R51 49R9
TDC_CAL_START
TDC_CAL_STOP1
TDC_CAL_STOP2
TDC_CAL_STOP3
TDC_CAL_STOP4
R34 10k
R106 10k
R98 10k
R99 10k
TDC_START_DIS
TDC_STOP_DIS
TDC can workonly in LVTTL or PECL mode. that's why PECL inputs are used for normal operation and LVTTL for calibration purposes
IC18A
LVPECL
LVTTL
TDC_CAL_START_P
TDC_CAL_START_N
TDC_CAL_START
MC100EPT23DG
IC18B
P3V3
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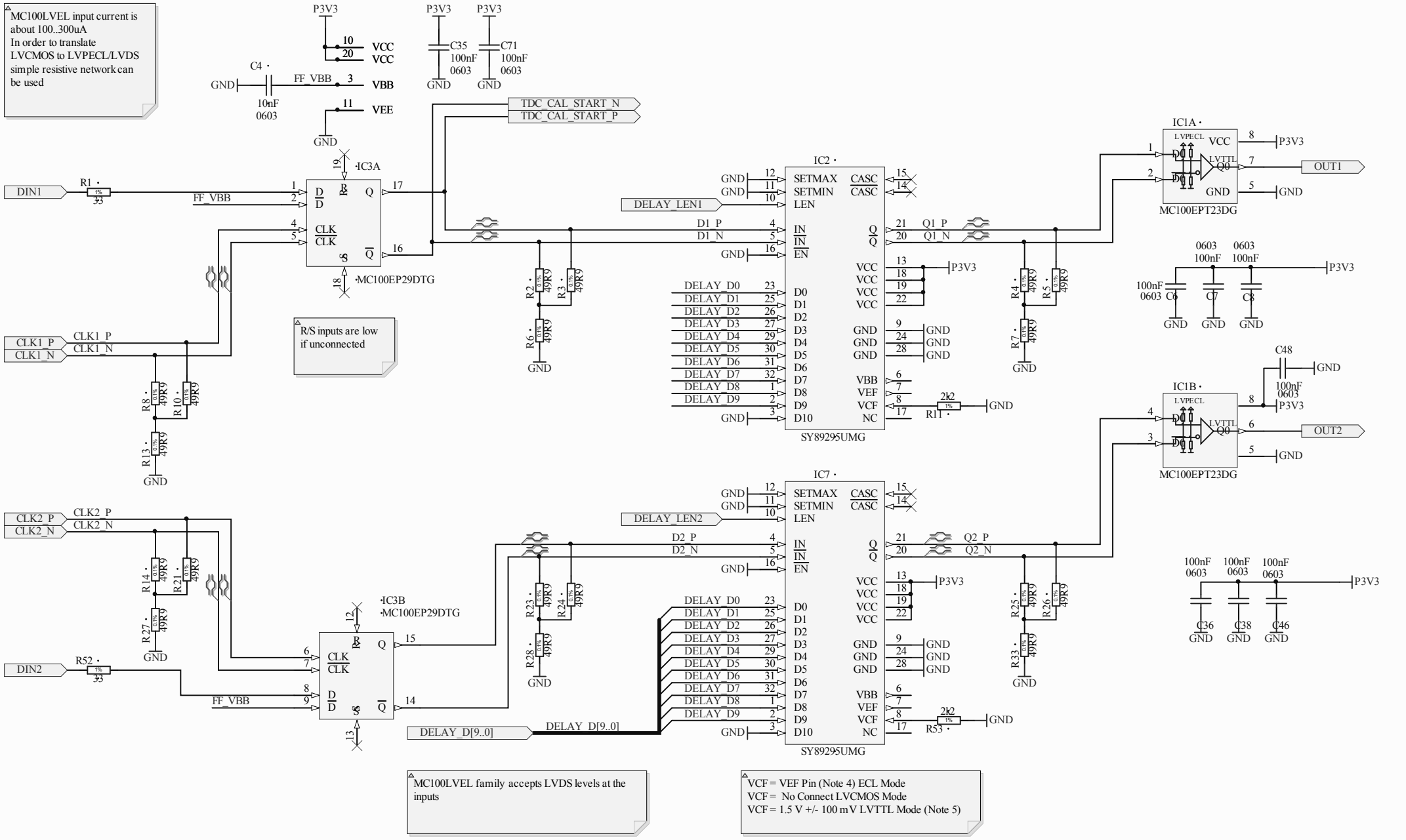

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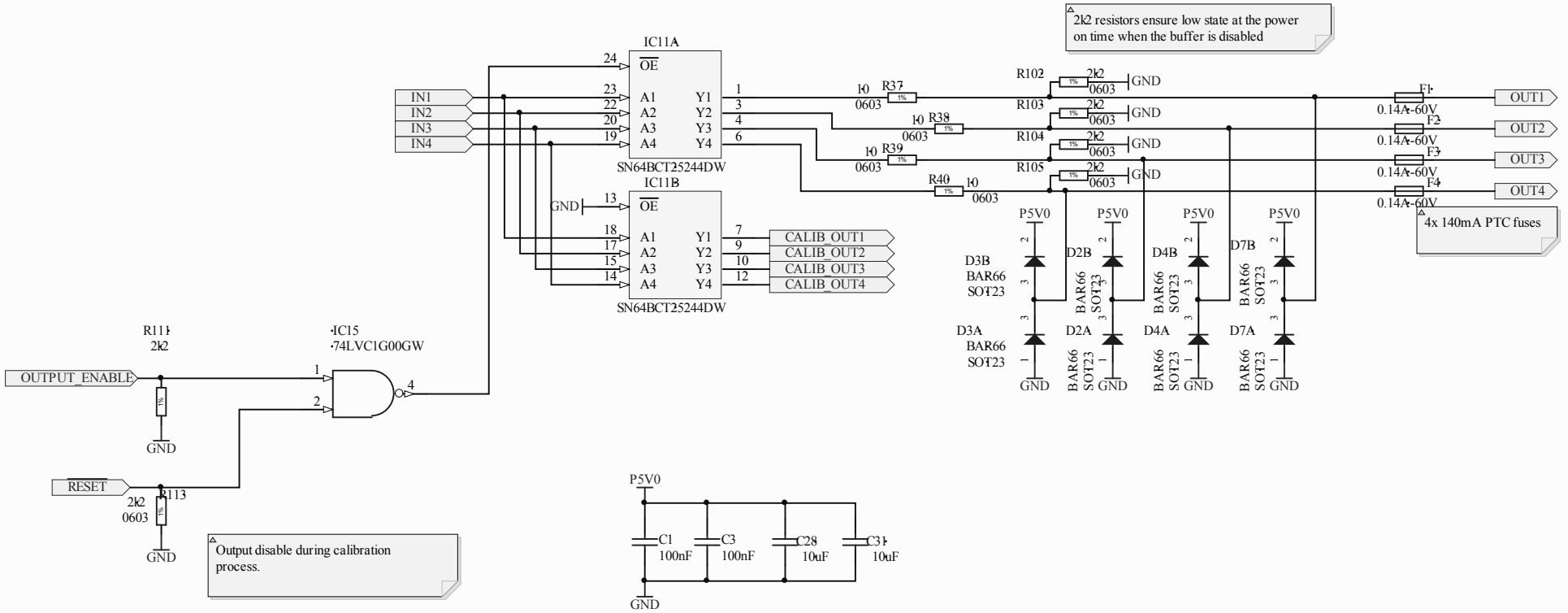

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