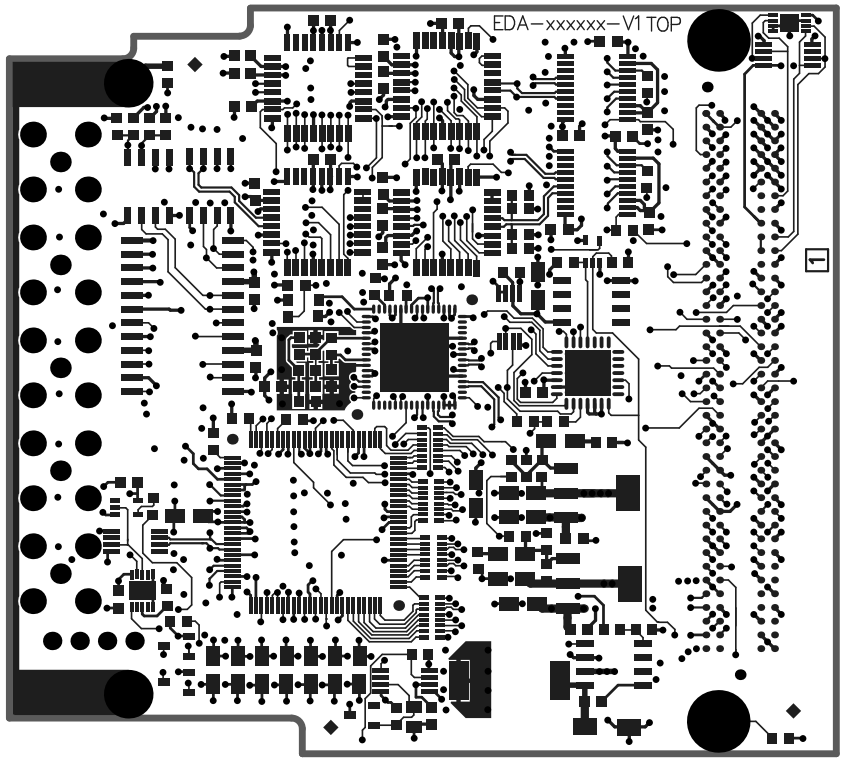
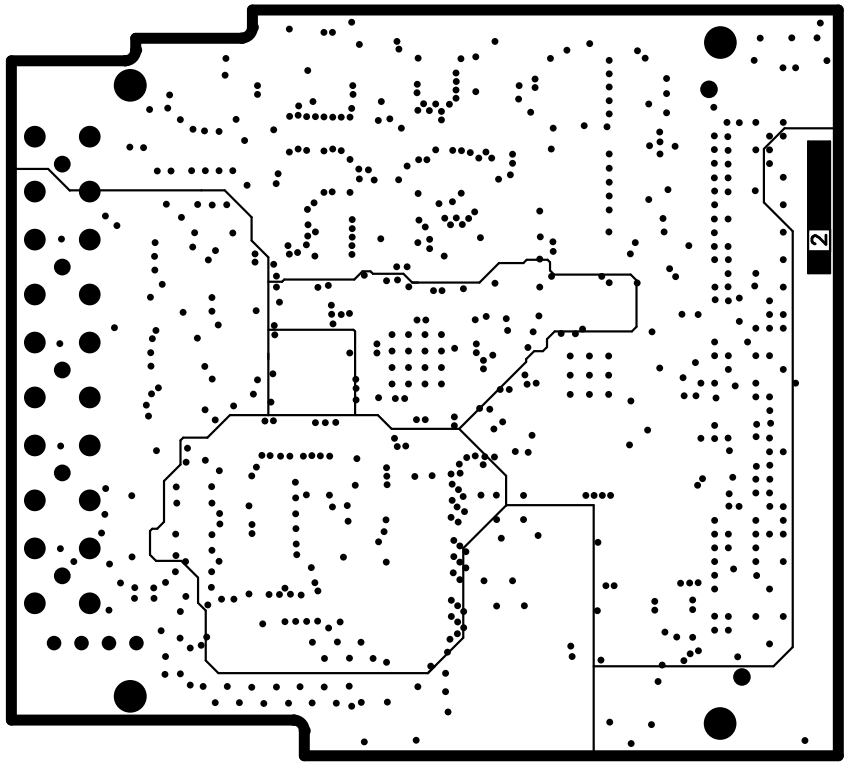


Number	EDA-XXXXX-VX
Drawn By	CREOTECH (GK)
DATE	12-03-2010
MOD.	-

Print Date 1/19/2011 2:52:32 PM

Top Layer

1

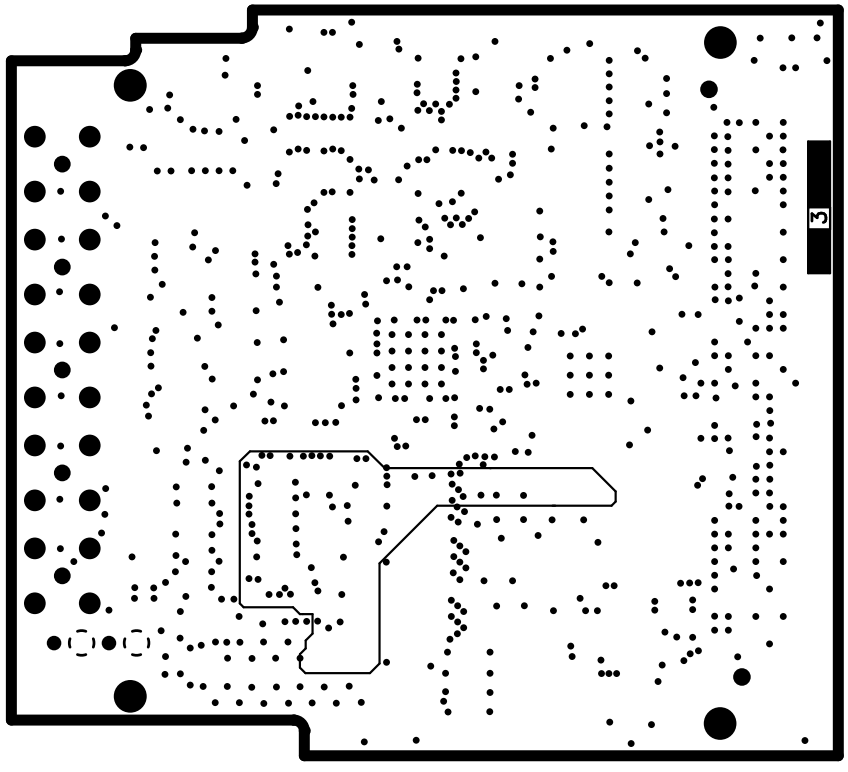


Number	EDA–XXXXX–VX
Drawn By	CREOTECH (GK)
DATE	12–03–2010
MOD.	–

Print Date 1/19/2011 2:52:32 PM

Plane L2 PWR

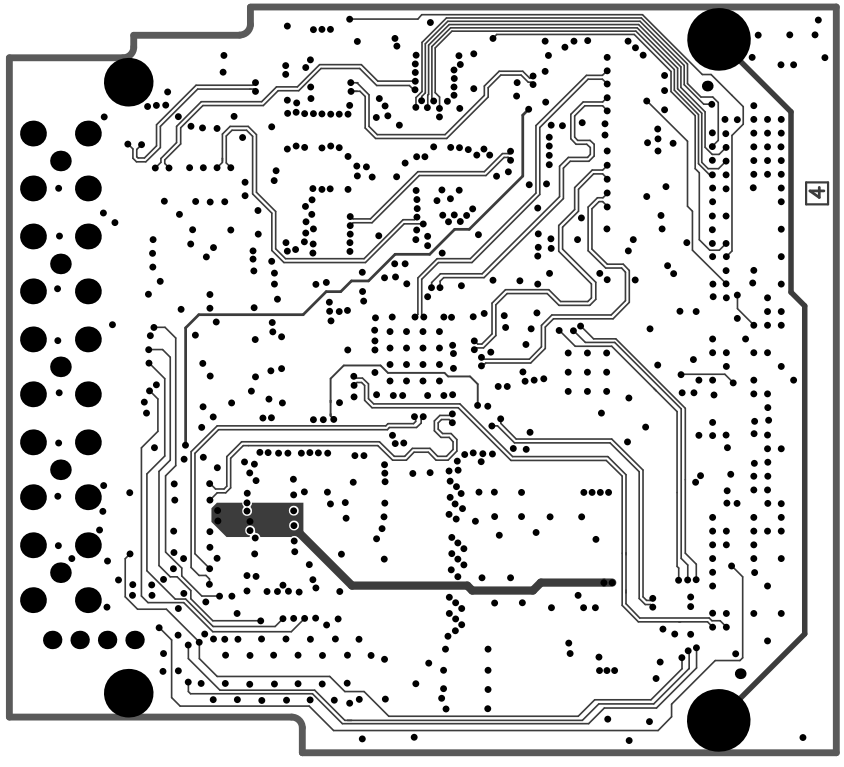
2



CERN

Number	EDA–XXXXX–VX
Drawn By	CREOTECH (GK)
DATE	12–03–2010
MOD.	–

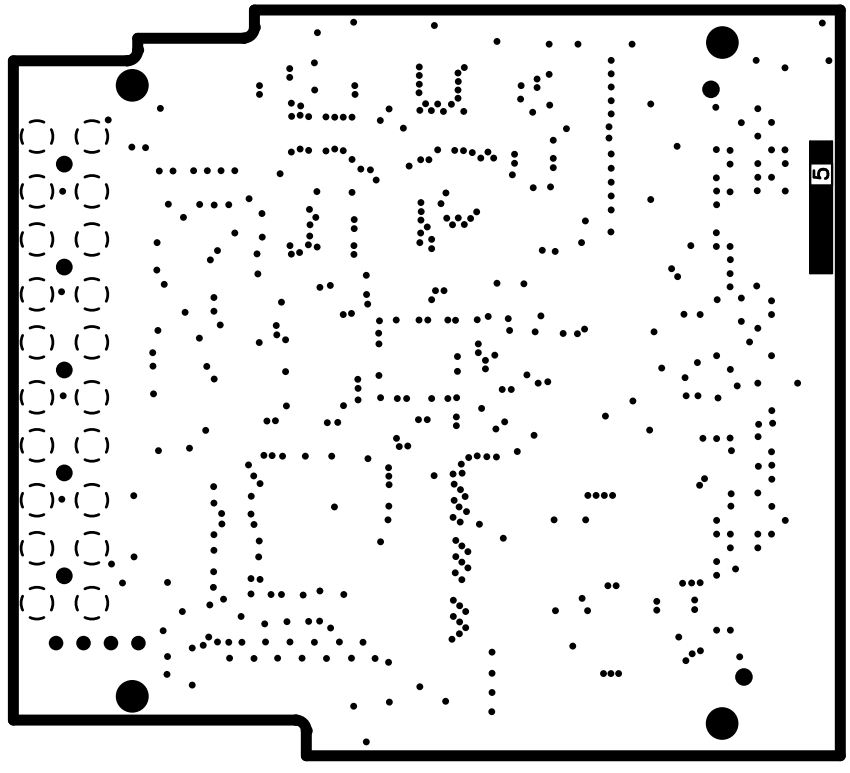
Print Date 1/19/2011 2:52:32 PM



CERN

Number	EDA–XXXXX–VX
Drawn By	CREOTECH (GK)
DATE	12–03–2010
MOD.	–

Print Date 1/19/2011 2:52:32 PM

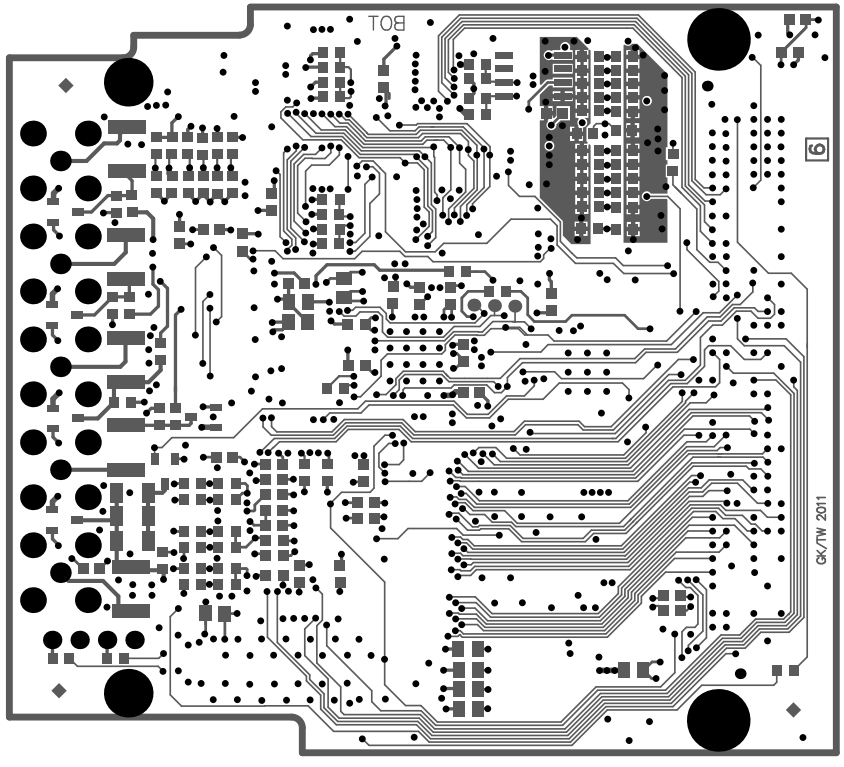


Number	EDA–XXXXX–VX
Drawn By	CREOTECH (GK)
DATE	12–03–2010
MOD.	–

Print Date 1/19/2011 2:52:32 PM

Plane L5 GND

5

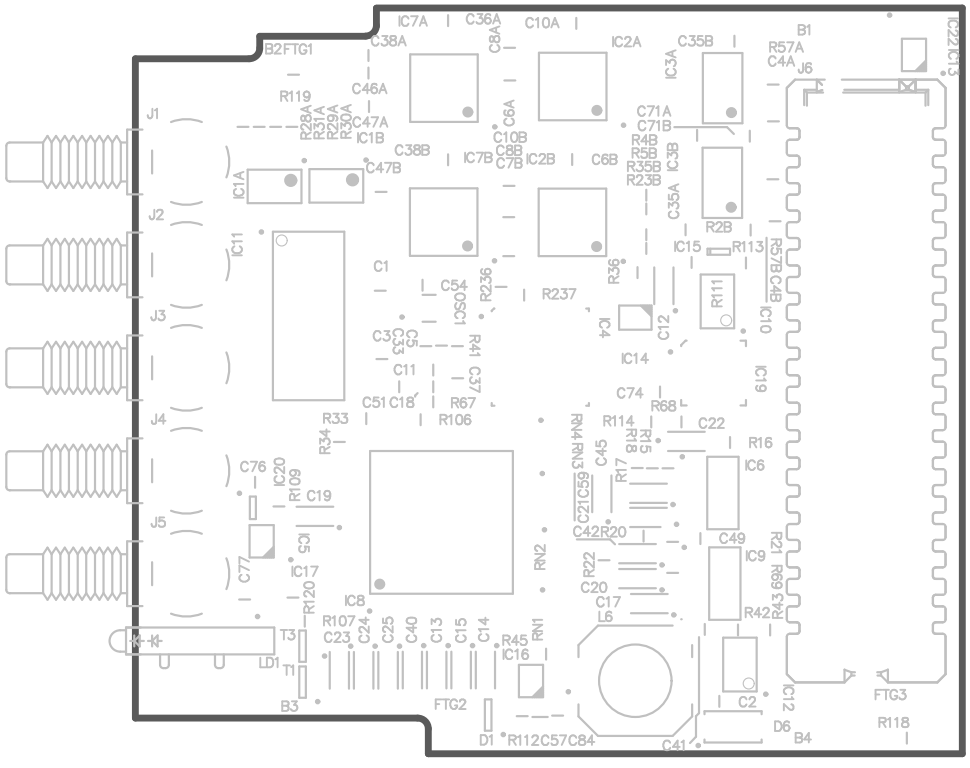


Number	EDA–XXXXX–VX
Drawn By	CREOTECH (GK)
DATE	12–03–2010
MOD.	–

Print Date 1/19/2011 2:52:32 PM

Bottom Layer

6



Number	EDA–XXXXX–VX
Drawn By	CREOTECH (GK)
DATE	12–03–2010
MOD.	–

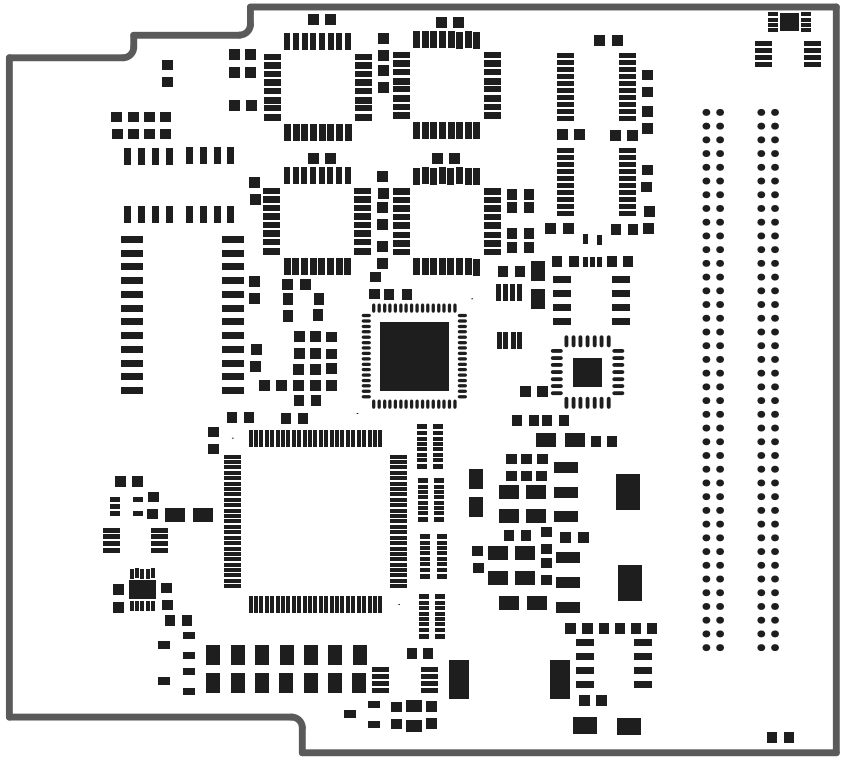
Print Date 1/19/2011 2:52:33 PM

Top Overlay

Number	EDA-XXXXX-VX
Drawn By	CREOTECH (GK)
DATE	12-03-2010
MOD.	-

Print Date 1/19/2011 2:52:33 PM

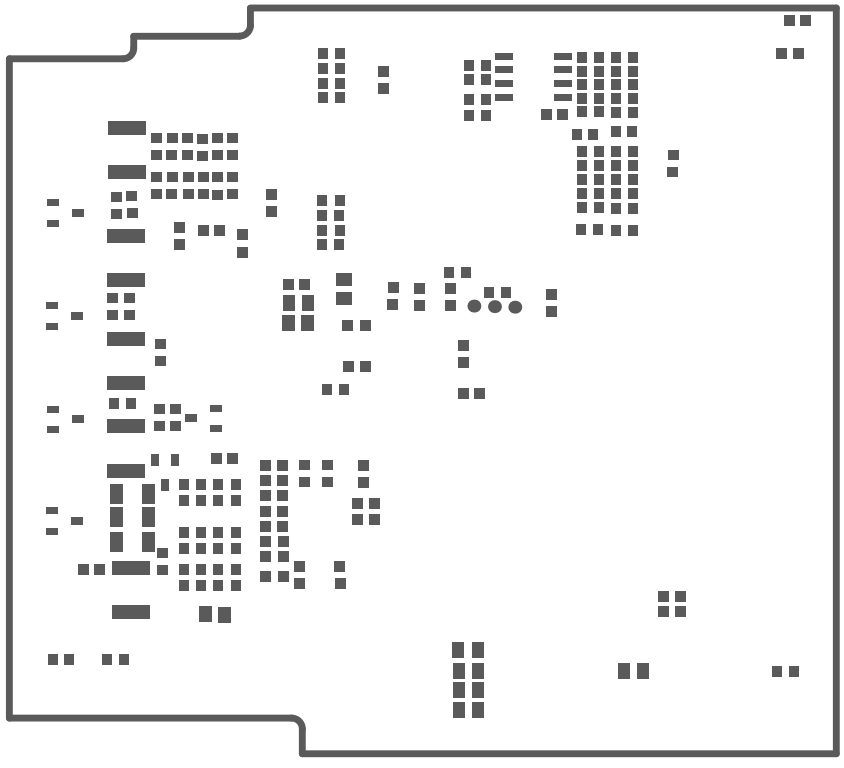
Bottom Overlay



Number	EDA-XXXXX-VX
Drawn By	CREOTECH (GK)
DATE	12-03-2010
MOD.	-

Print Date 1/19/2011 2:52:33 PM

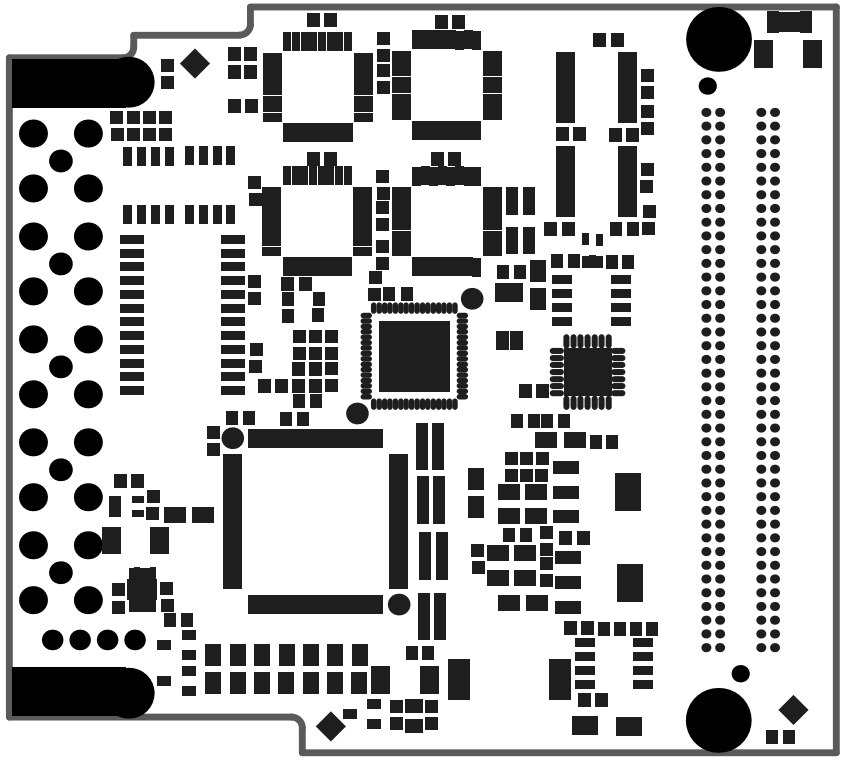
Top Paste



Number	EDA-XXXXX-VX
Drawn By	CREOTECH (GK)
DATE	12-03-2010
MOD.	-

Print Date 1/19/2011 2:52:33 PM

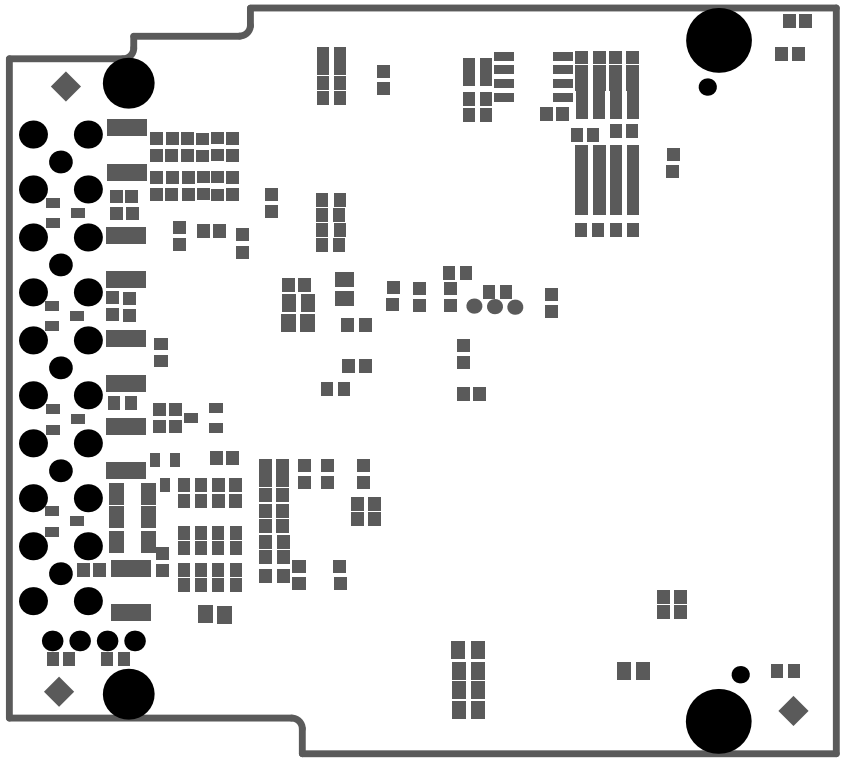
Bottom Paste



Number	EDA-XXXXX-VX
Drawn By	CREOTECH (GK)
DATE	12-03-2010
MOD.	-

Print Date 1/19/2011 2:52:33 PM

Top Solder



Number	EDA-XXXXX-VX
Drawn By	CREOTECH (GK)
DATE	12-03-2010
MOD.	-

Print Date 1/19/2011 2:52:33 PM

Bottom Solder

U_power_supply
power_supply.SchDoc
RESETn
RESETn

16-bit I/O Port Expander With Serial Interface
IC19
EXT_CSn
SCLK
SDI
SDO
R68
100
0603
1%
P3V3
C74
100nF
0603
C84
1uF
0603
GND
RESETn
P3V3
GND
CS
SCK
SI
SO
A2
A1
A0
RESET
INTB
INTA
VDD
VSS
EP
GPA7
GPA6
GPA5
GPA4
GPA3
GPA2
GPA1
GPA0
GPB7
GPB6
GPB5
GPB4
GPB3
GPB2
GPB1
GPB0
TDC_OEN
TERM_ENABLE
PLL_STATUS
PLL_LD
PLL_REFMON
TRIG_SEL
LED1
LED2
OUTPUT_ENABLE
MCP23S17-E/ML

U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
DELAY_D[9..0]
DELAY_LEN1
DELAY_LEN2
DIN1
DIN2
CLK1_P
CLK1_N
CLK2_P
CLK2_N
OUT1
OUT2
TDC_CAL_START_P
TDC_CAL_START_N

U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
DELAY_D[9..0]
DELAY_LEN3
DELAY_LEN4
DELAY_LEN1
DELAY_LEN2
DIN3
DIN4
DIN1
DIN2
CLK1_P
CLK1_N
CLK2_P
CLK2_N
TDC_CAL_START_N
TDC_CAL_START_P
OUT1
OUT2

U_OUTPUT_BUFFER
OUTPUT_BUFFER.SchDoc
IN1
IN2
IN3
IN4
OUT1
OUT2
OUT3
OUT4
RESETn
RESET
OUTPUT_ENABLE
CALIB_OUT1
CALIB_OUT2
CALIB_OUT3
CALIB_OUT4
J1
J2
J3
J4
SMC
GND

FMC connector.SchDoc
U_FMC connector
DELAY_D[9..0]
DIN1
DIN2
DIN3
DIN4
DELAY_LEN1
DELAY_LEN2
DELAY_LEN3
DELAY_LEN4

VREF MUST BE 2.5V or 3.3V

U_INPUT_LOGIC
INPUT_LOGIC.SchDoc
J5
SMC
GND
IN
TDC_START_P
TDC_START_N
TRIG_FPGA
TRIG_SEL
TRIG_OUT_LVTTL
TERM_ENABLE

TDC_START_P
TDC_START_N

U_TDC
TDC.SchDoc
RESETn
TDC_RESETn
TDC_CAL_START_P
TDC_CAL_START_N
TDC_START_P
TDC_START_N
TDC_CAL_STOP1
TDC_CAL_STOP2
TDC_CAL_STOP3
TDC_CAL_STOP4
TDC_START_DIS
TDC_STOP_DIS
TDC_ERR
TDC_EMPTY_FLAG
TDC_LOAD_FLAG
TDC_INT
TDC_OEN
TDC_CSN
TDC_RDN
TDC_WRN
TDC_ADR[3..0]
TDC_D[27..0]
TDC_STOP2_P
TDC_STOP2_N
TDC_STOP1_P
TDC_STOP1_N
TDC_REF_CLK

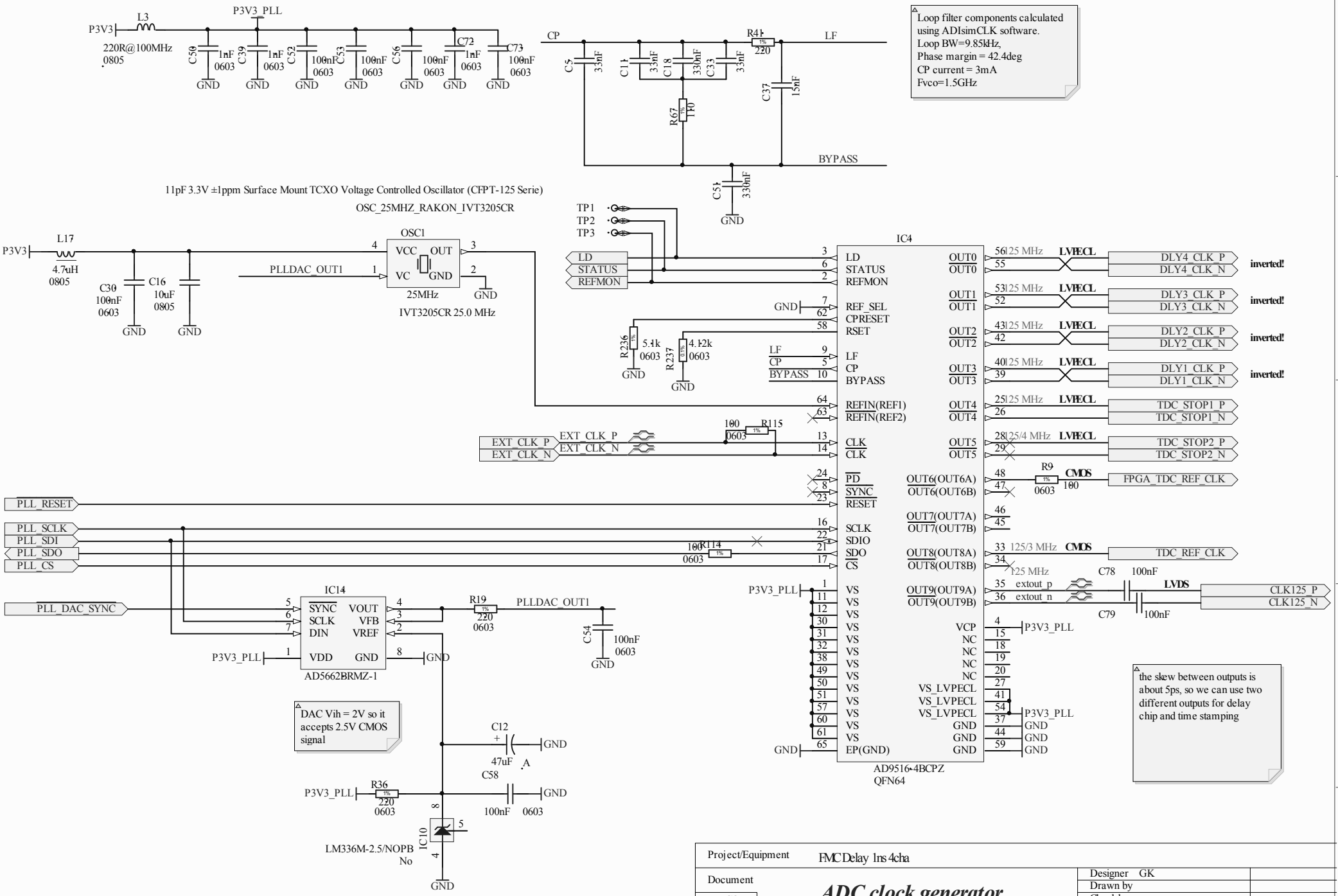
U_LED_MEM
LED_MEM.SchDoc
SDA
SCL
GA0
GA1
LED1
LED2

U_clock_generator
clock_generator.SchDoc
DLY1_CLK_P
DLY1_CLK_N
DLY2_CLK_P
DLY2_CLK_N
DLY3_CLK_P
DLY3_CLK_N
DLY4_CLK_P
DLY4_CLK_N
RESETn
PLL_RESET
TDC_STOP2_P
TDC_STOP2_N
TDC_STOP1_P
TDC_STOP1_N
TDC_REF_CLK
FPGA_TDC_REF_CLK
CLK125_P
CLK125_N
PLL_DAC_SYNC
PLL_SCLK
PLL_CS
PLL_SDO
PLL_SDI
SCLK
SDO
SDI
PLL_LD
PLL_STATUS
PLL_REFMON
LD
STATUS
REFMON
EXT_CLK_P
EXT_CLK_N
TRIG_OUT_LVTTL
EXT_CSn

Default mode:
TDC in R-Mode, 40MHz per channel. TDC driven by 125MHz/4 clock.
START: trigger
STOP: 125/4 clock delivered to STOP2 input
125MHz clock delivered to STOP1 input
27ps resolution.
trigger positions in reference with both 125MHz and 125/4 clocks can be captured

Calibration mode:
TDC in I-Mode,
LVTTL inputs, 10MHz max, TDC driven by 10MHz clock
START: 10MHz clock delivered to TDC_CAL_START
STOP: buffer output
81ps resolution

Project/Equipment	FMC Delay 1ns 4cha		
Document	**FMC delay top**	Designer GK	
BE-CO		Drawn by GK	
		Check by -	-
		Last Mod. -	1/19/2011
		File FMC_Delay_1ns_4Cha.SchDoc	
		Print Date 1/19/2011 2:52:43 PM	Sheet 1 of 9
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A3	Rev -


Loop filter components calculated using ADIsimCLK software.
Loop BW=9.85kHz,
Phase margin = 42.4deg
CP current = 3mA
Fvco=1.5GHz
11pF 3.3V ±1ppm Surface Mount TCXO Voltage Controlled Oscillator (CFPT-125 Serie)
OSC_25MHZ_RAKON_IVT3205CR
IVT3205CR 25.0 MHz
AD5662BRMZ-1
AD9516-4BCPZ
QFN64
LM336M-2.5/NOPB
DAC Vih = 2V so it accepts 2.5V CMOS signal
the skew between outputs is about 5ps, so we can use two different outputs for delay chip and time stamping
Project/Equipment FMC Delay 1ns 4cha
Document
ADC clock generator
Designer GK
Drawn by
Check by -
Last Mod. - 1/19/2011
File clock_generator.SchDoc
Print Date 1/19/2011 2:52:43 PM Sheet 2 of 9
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
EDA-XXXXX-VX-X
Size A4 Rev -

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.

VREF MUST BE 2.5V or 3.3V

DELAY_D[9..0] DELAY_D[9..0]

TDC_ADR[3..0] TDC_ADR[3..0]
TDC_D[27..0] TDC_D[27..0]

H

J6D

	h1		
GND	h2		
	h3		
GND	h4		
CLK125_P	h5	CLK125_P	CLK125_P
CLK125_N	h6	CLK125_N	CLK125_N
GND	h7		
TDC_D0	h8		
TDC_D1	h9		
GND	h10		
TDC_D4	h11		
TDC_D6	h12		
GND	h13		
TDC_D14	h14		
TDC_D15	h15		
GND	h16		
TDC_D22	h17		
TDC_D23	h18		
GND	h19		
TDC_ERR	h20		
TDC_INT	h21		
GND	h22		
TDC_ADR2	h23		
TDC_ADR3	h24		
GND	h25		
DIN2	h26		
DIN1	h27		
GND	h28		
DELAY_LEN1	h29		
DELAY_LEN2	h30		
GND	h31		
DELAY_D9	h32		
DELAY_D8	h33		
GND	h34		
DELAY_D5	h35		
DELAY_D4	h36		
GND	h37		
DELAY_D1	h38		
DELAY_D0	h39		
GND	h40		
VADJ			

G

J6G

	g1		
EXT_CLK_P	g2	EXT_CLK_P	EXT_CLK_P
EXT_CLK_N	g3	EXT_CLK_N	EXT_CLK_N
GND	g4		
GND	g5		
TRIG_OUT_LVTTL	g6		
TRIG_FPGA	g7		
GND	g8		
TDC_D2	g9		
TDC_D3	g10		
GND	g11		
TDC_D10	g12		
TDC_D11	g13		
GND	g14		
TDC_D20	g15		
TDC_D21	g16		
GND	g17		
TDC_EMPTY_FLAG	g18		
TDC_LOAD_FLAG	g19		
GND	g20		
EXT_CSn	g21		
TDC_CSN	g22		
GND	g23		
TDC_START_DIS	g24		
TDC_STOP_DIS	g25		
GND	g26		
DIN4	g27		
DIN3	g28		
GND	g29		
DELAY_LEN4	g30		
DELAY_LEN3	g31		
GND	g32		
DELAY_D7	g33		
DELAY_D6	g34		
GND	g35		
DELAY_D3	g36		
DELAY_D2	g37		
GND	g38		
VADJ	g39		
GND	g40		

D

J6B

	d1		
GND	d2		
GND	d3		
	d4		
GND	d5		
GND	d6		
TDC_D5	d7		
TDC_D7	d8		
GND	d9		
TDC_D12	d10		
TDC_D13	d11		
GND	d12		
TDC_D16	d13		
TDC_D17	d14		
GND	d15		
TDC_D24	d16		
TDC_D25	d17		
GND	d18		
TDC_WRN	d19		
TDC_RDN	d20		
GND	d21		
FPGA_TDC_REF_CLK	d22		
PLL_DAC_SYNC_N	d23		
GND	d24		
PLL_SCLK	d25		
PLL_CS	d26		
GND	d27		
TDI	d28		
TDO	d29		
P3V3_AUX	d30		
	d31		
GA1	d32		
P3V3	d33		
GND	d34		
P3V3	d35		
GND	d36		
P3V3	d37		
	d38		
	d39		
	d40		

C

J6A

GND	c1		
	c2		
	c3		
GND	c4		
GND	c5		
	c6		
	c7		
	c8		
GND	c9		
GND	c10		
TDC_D8	c11		
TDC_D9	c12		
GND	c13		
GND	c14		
TDC_D18	c15		
TDC_D19	c16		
GND	c17		
GND	c18		
TDC_D26	c19		
TDC_D27	c20		
GND	c21		
GND	c22		
TDC_ADR0	c23		
TDC_ADR1	c24		
GND	c25		
GND	c26		
PLL_SDI	c27		
PLL_SDO	c28		
GND	c29		
GND	c30		
SCL	c31	SCL	SCL
SDA	c32	SDA	SDA
GND	c33		
GND	c34		
GA0	c35	GA0	GA0
P12V0	c36		
GND	c37		
P12V0	c38		
GND	c39		
P3V3	c40		
GND			

FTG1 FTG2 FTG3 FTG6 FTG5 FTG4

FTG1 ... FTG6
Reference points for the component mounting machine.

B1 B4

R 118 0 R

GND

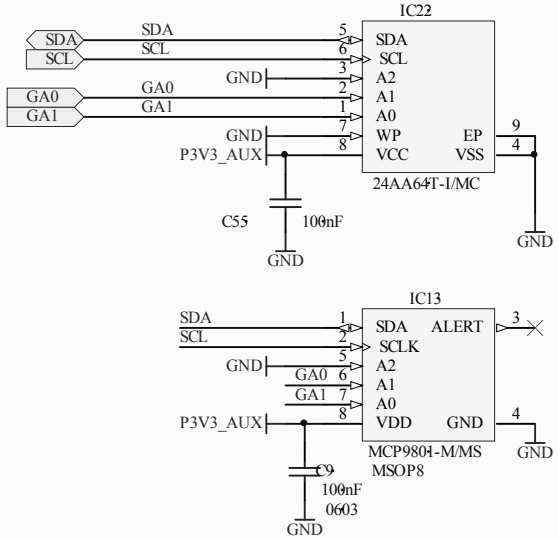
B1 ... B4
screw holes for mounting the FmcAdc to the carrier board.

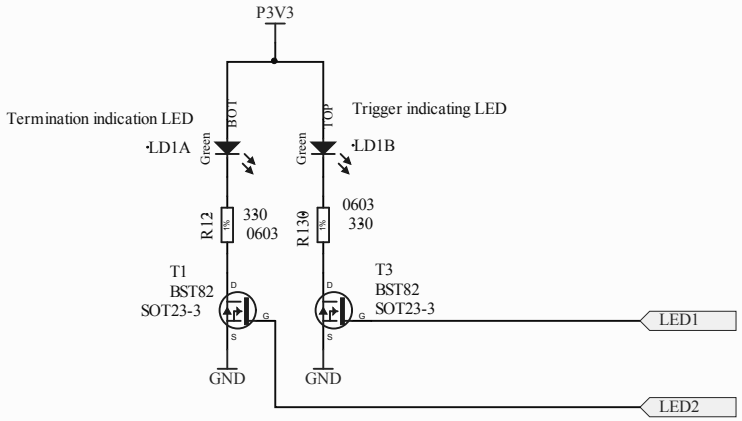
B2 B3

R 119 0 R

GND

Project/Equipment	FMC Delay 1ns 4cha
Document	**FMC Connector**
BE-CO / CERN	European Organization for Nuclear Research CH-1211 Geneve 23 - SwitzerLA_Pd
Designer	Greg Kasprowicz,
Drawn by	Greg Kasprowicz 10/07/2010
Check by	M.C., T.W., E.B. -
Last Mod.	- 1/19/2011
File	FMC connector.SchDoc
Print Date	1/19/2011 2:52:43 PM Sheet 3 of 9
	EDA-XXXXX-XX-X Size A3 Rev -

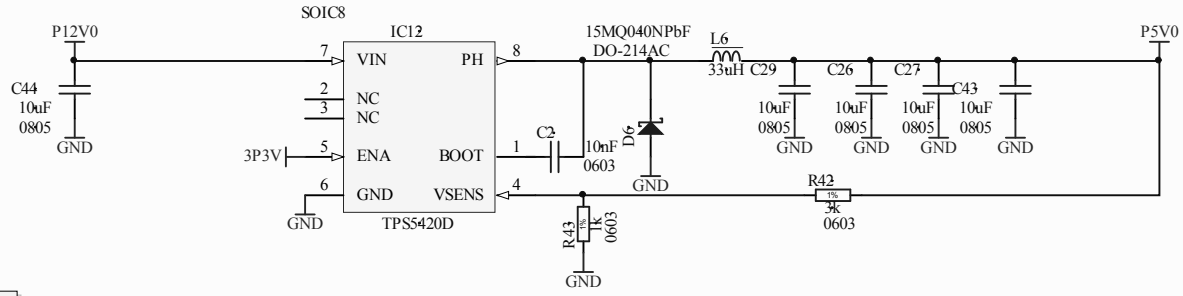




24AA64T = 1 0 1 0 0 GA0 GA1
MCP9801 = 1 0 0 1 0 GA0 GA1

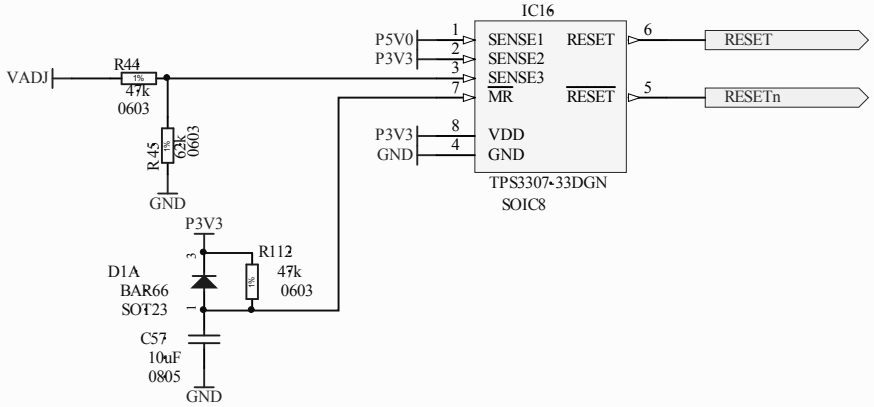
Project/Equipment	FMC Delay 1ns 4cha		
Document	**LED and MEMORY**	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check by -	-
		Last Mod. -	1/19/2011
		File LED_MEM.SchDoc	
		Print Date 1/19/2011 2:52:44 PM	Sheet 4 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -

P5V0 is used to power TDC chip. It is then used to supply LDO regulators, so it doesn't need to be very clean and stable

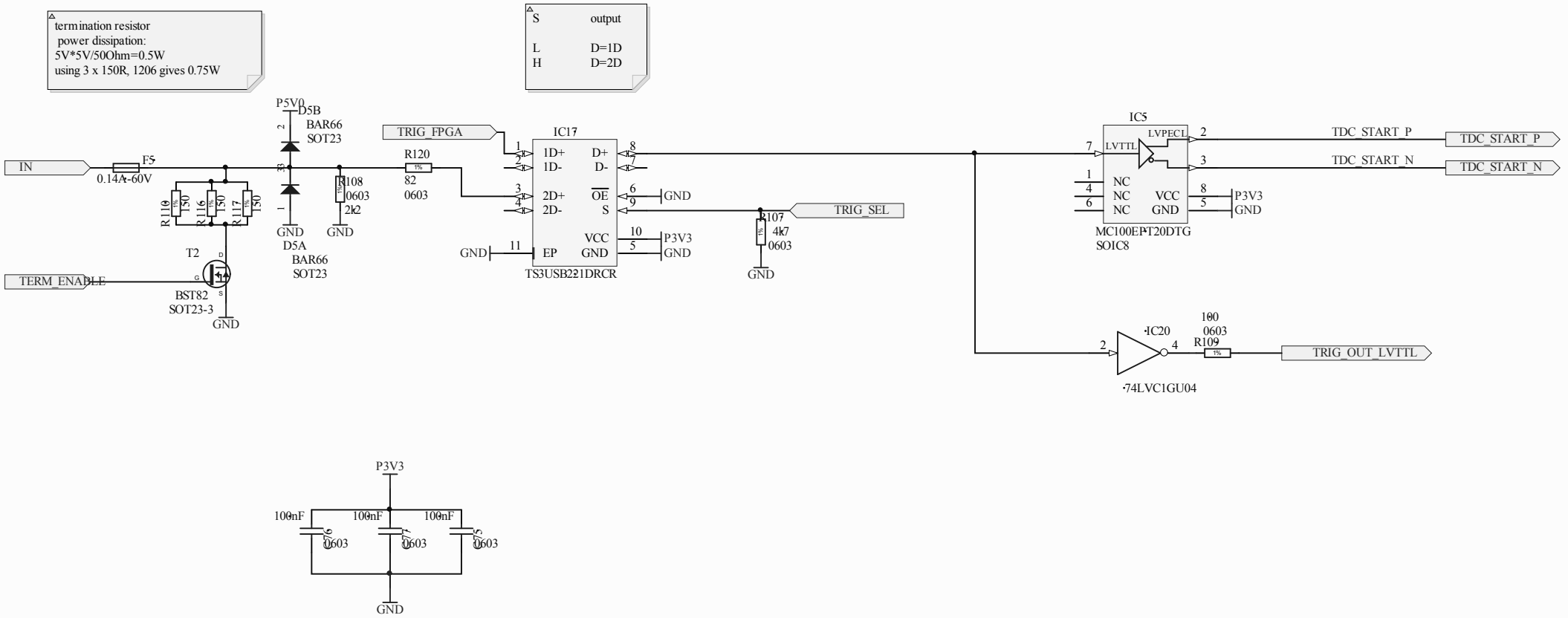


TPS3307-33D thresholds

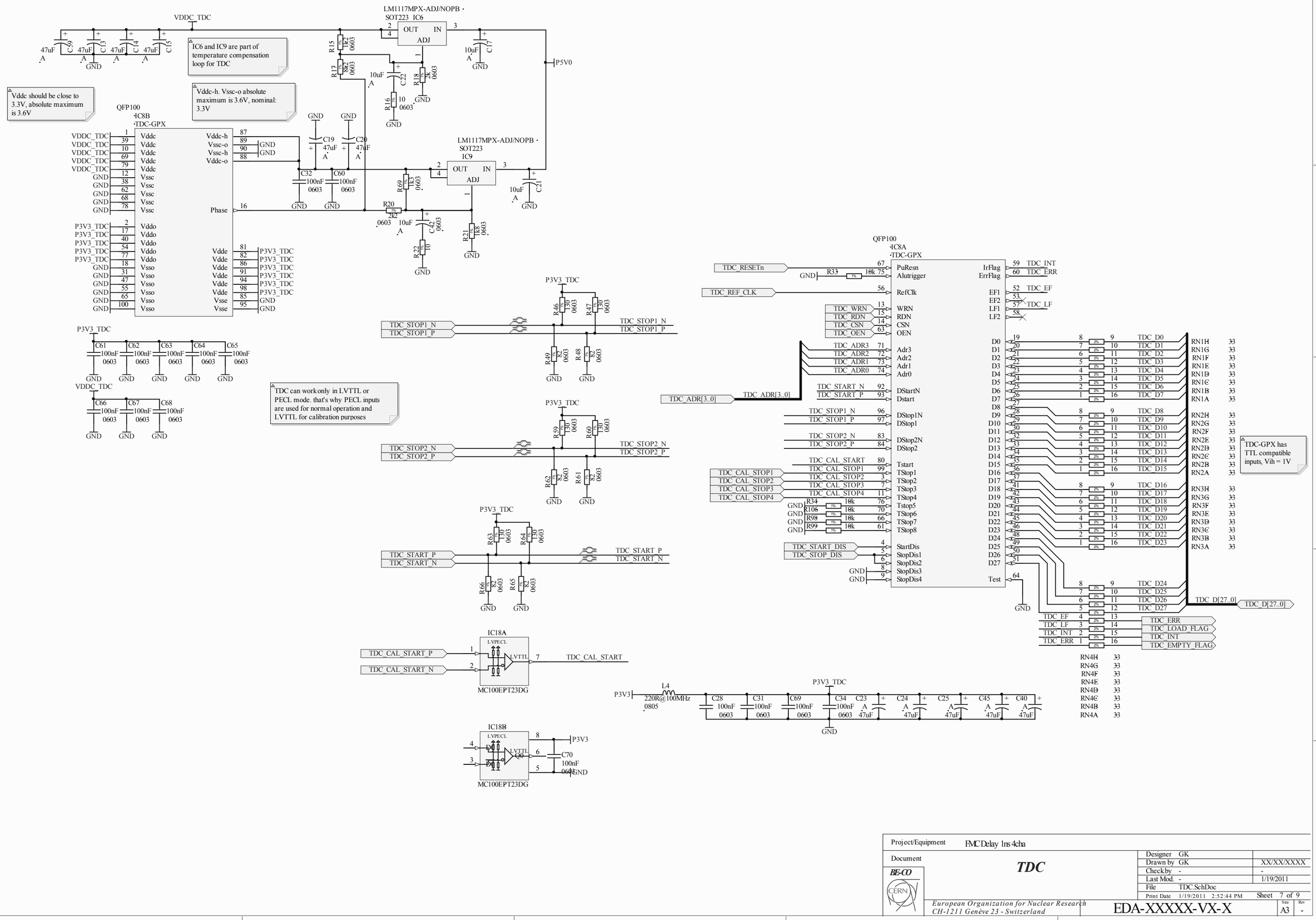
sense1	sense2	sense3
4.55V	2.93V	1.25V



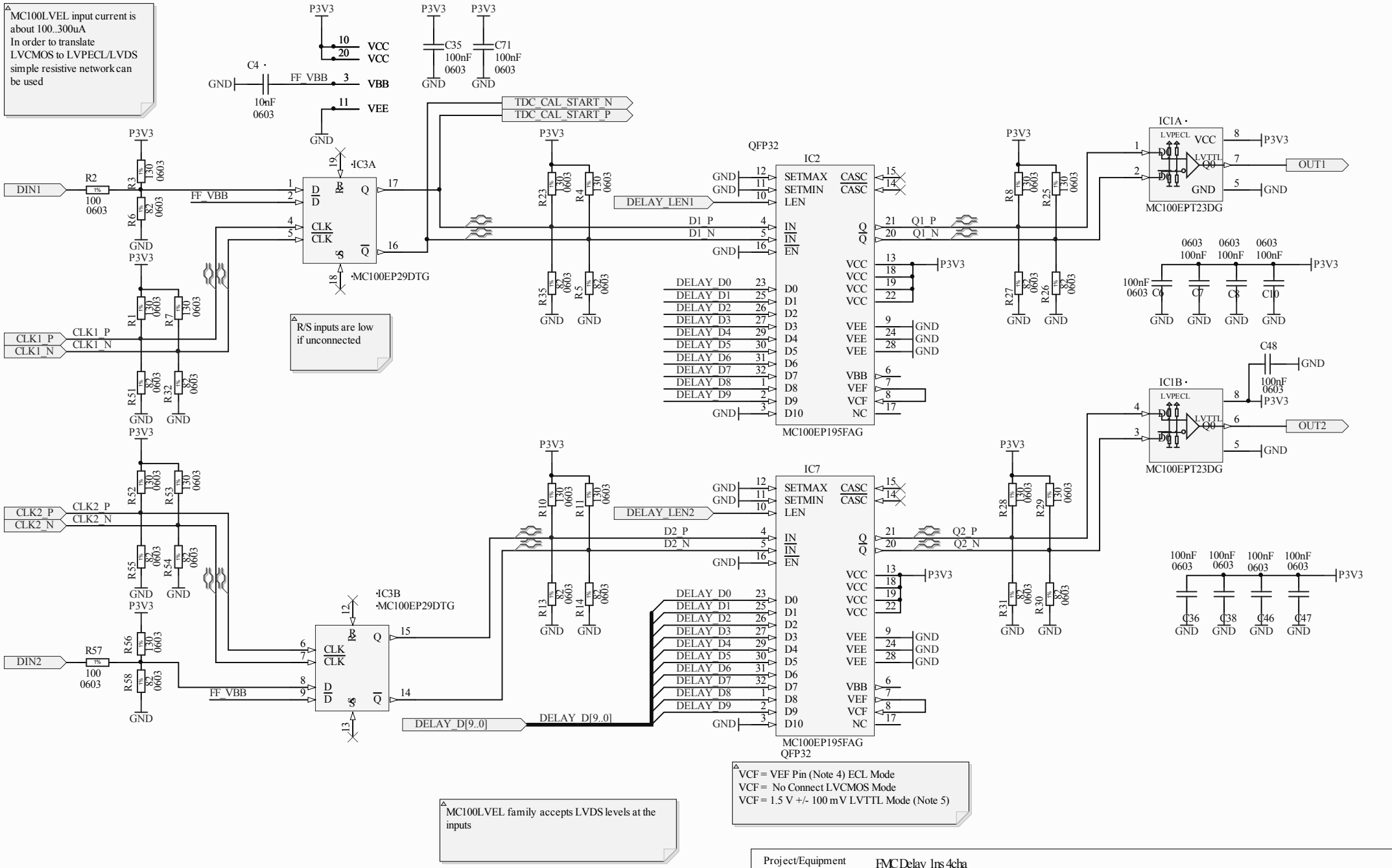
Project/Equipment	FMC Delay 1ns 4cha		
Document	**Power supplies** -	Designer GK	
		Drawn by	
		Check by -	-
		Last Mod. -	1/19/2011
		File power_supply.SchDoc	
		Print Date 1/19/2011 2:52:44 PM	Sheet 5 of 9
BE-CO CERN	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	**Input logic**	Designer GK	
	-	Drawn by	
		Check by -	-
		Last Mod. -	1/19/2011
		File INPUT_LOGIC.SchDoc	
		Print Date 1/19/2011 2:52:44 PM	Sheet 6 of 9
BE-CO CERN	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4 / Rev -



Project/Equipment	FMC Delay 1ns 4cha
Document	**TDC**
Designer	GK
Drawn by	GK XX/XX/XXXX
Checkby	- -
Last Mod.	- 1/19/2011
File	TDC.SchDoc
Print Date	1/19/2011 2:52:44 PM Sheet 7 of 9
BE-CO / CERN	*European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland*
	EDA-XXXXX-VX-X Size A3 Rev -



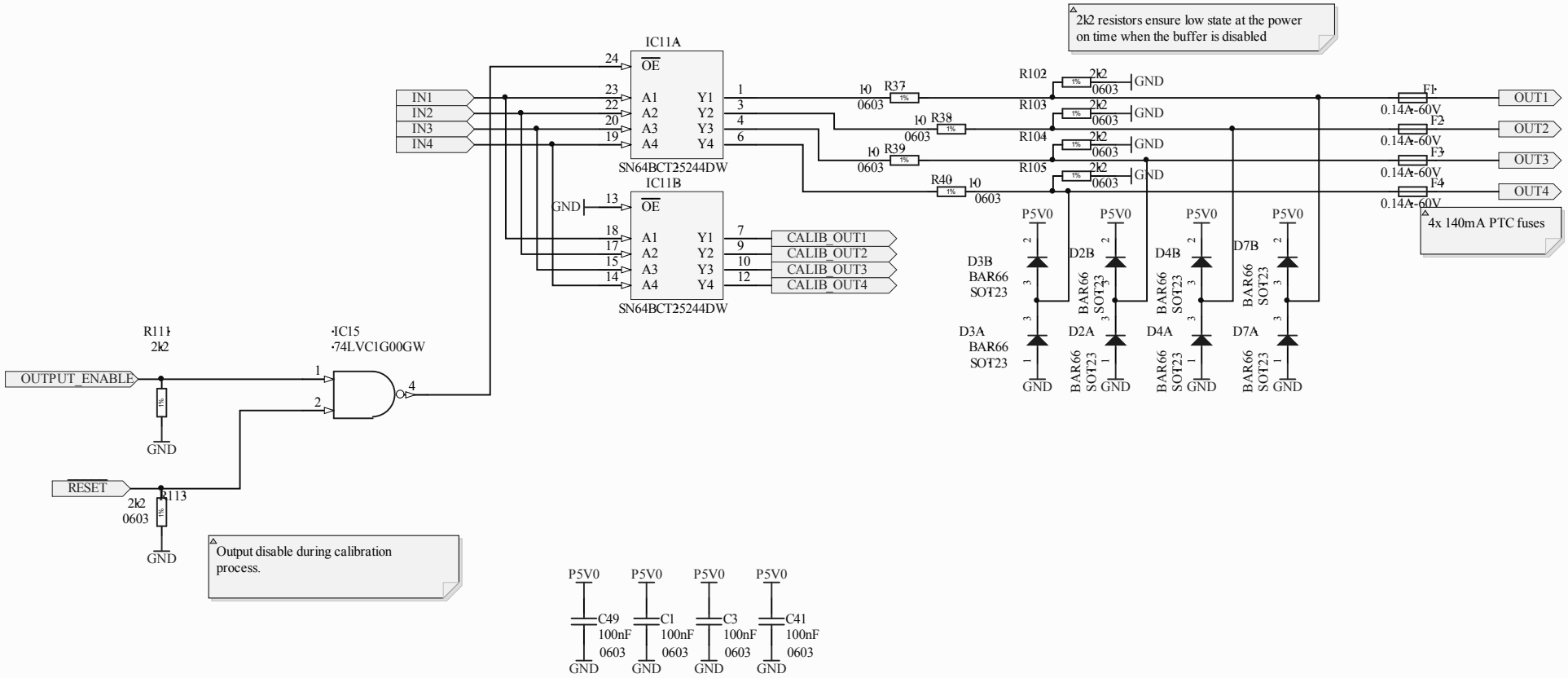
Project/Equipment	FMC Delay 1ns 4cha		
Document	**DELAY**	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check by -	-
		Last Mod. -	1/19/2011
		File CHANNEL_DELAY.SchDoc	
		Print Date 1/19/2011 2:52:44 PM	Sheet 8 of 9

BE-CO

European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

EDA-XXXXX-VX-X

Size A4 | Rev -



Project/Equipment	FMC Delay 1ns 4cha		
Document	**Output buffer**	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check by -	-
		Last Mod. -	1/19/2011
		File OUTPUT_BUFFER.SchDoc	
		Print Date 1/19/2011 2:52:44 PM	Sheet 9 of 9
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