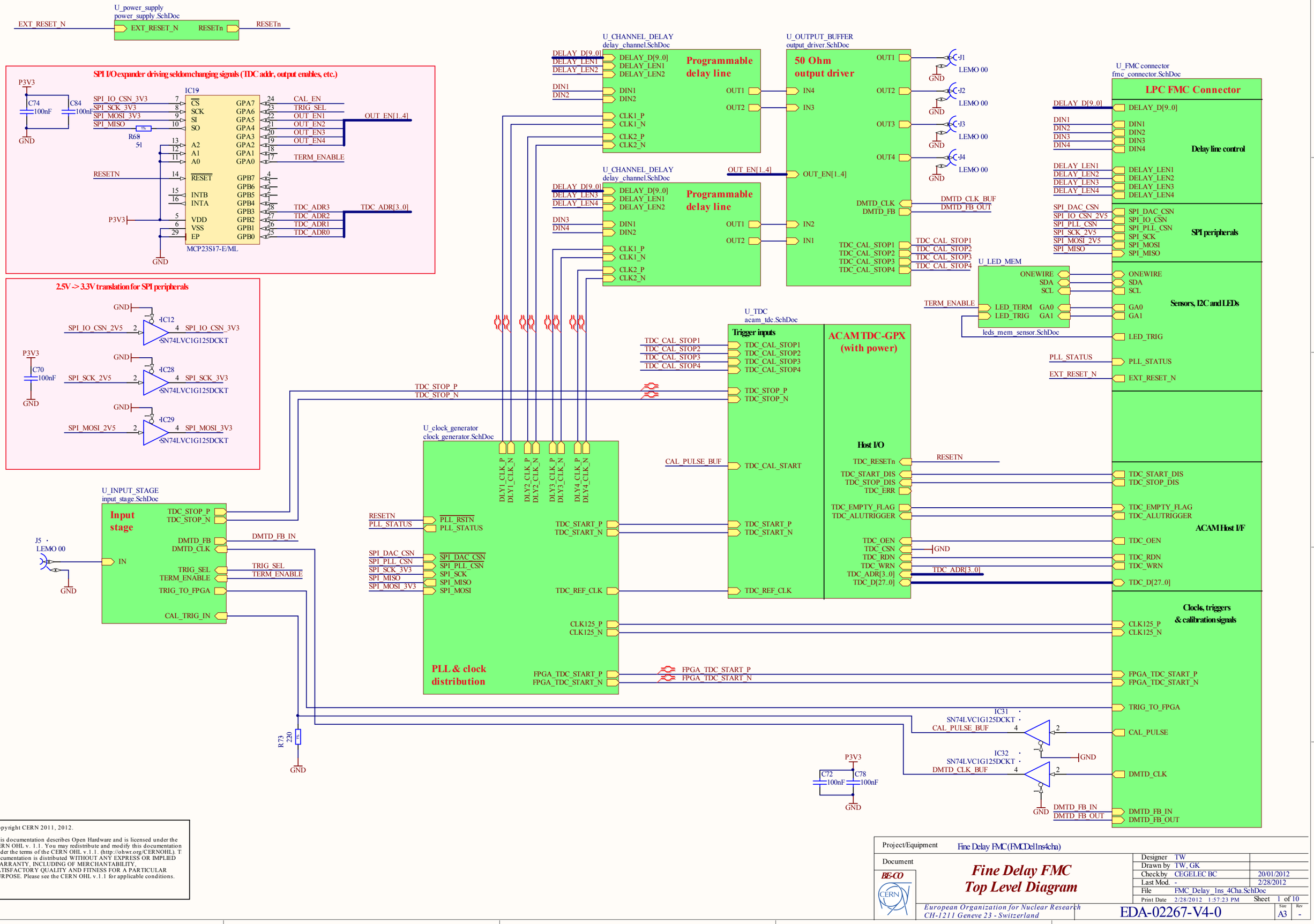

Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document: **Fine Delay FMC Top Level Diagram**

Designer	TW	
Drawn by	TW, GK	
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	FMC_Delay_1ns_4Cha.SchDoc	
Print Date	2/28/2012 1:57:23 PM	Sheet 1 of 10

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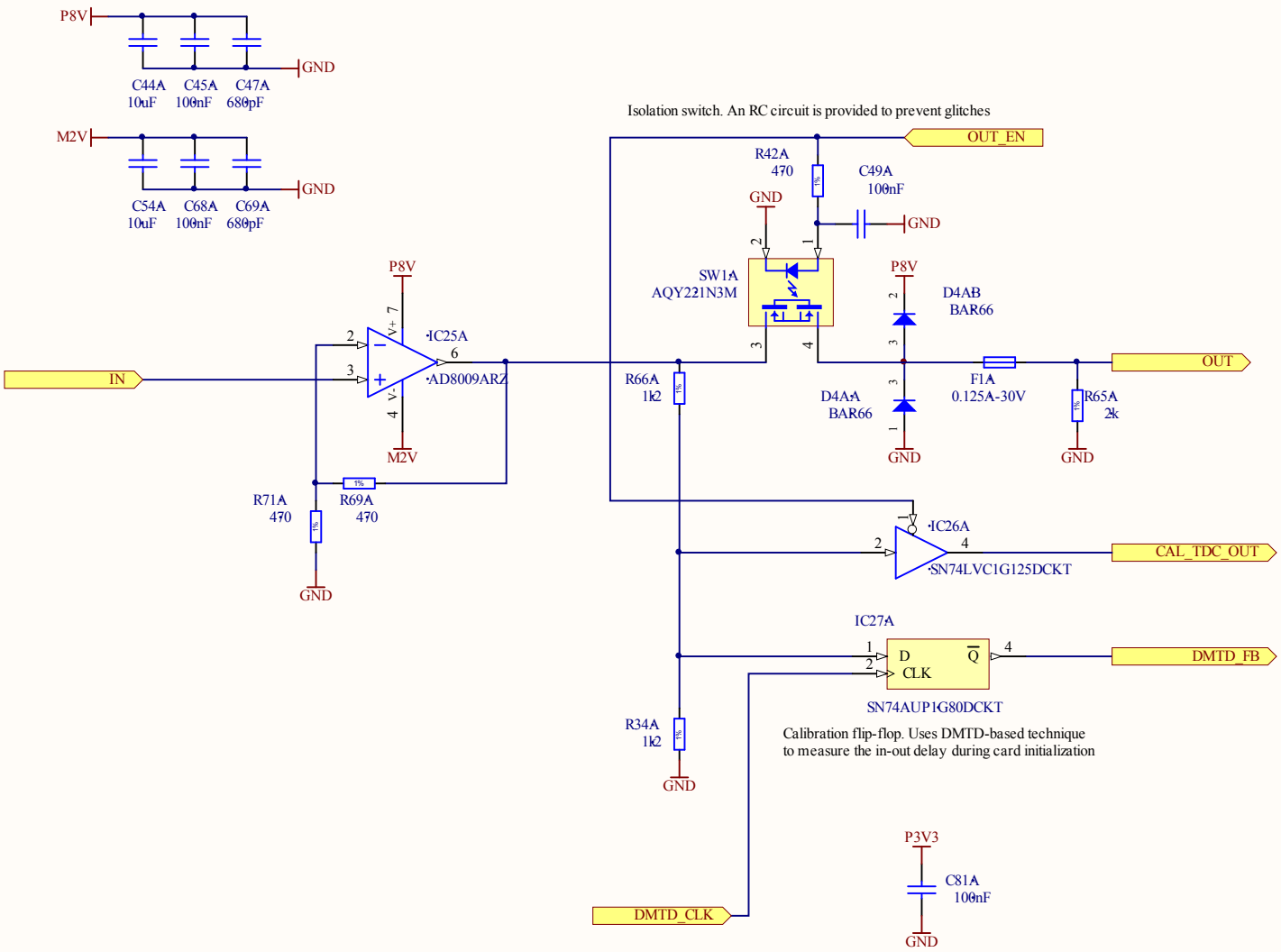

Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

Fine Delay FMC
Single output channel

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Designer	TW	
Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
Print Date	2/28/2012 1:57:23 PM	Sheet 10 of 10

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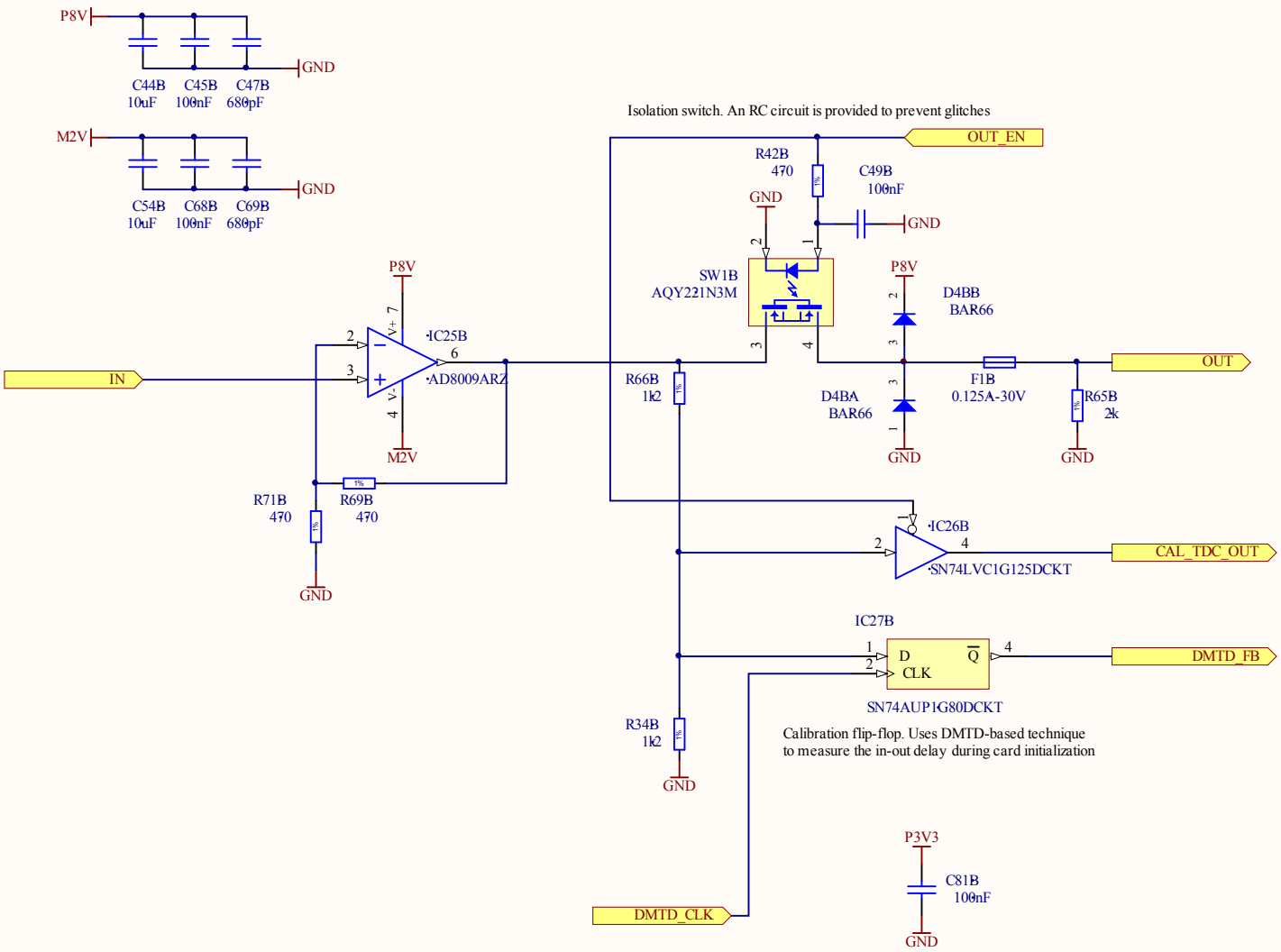
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

Fine Delay FMC
Single output channel

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Designer	TW	
Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
Print Date	2/28/2012 1:57:24 PM	Sheet 10 of 10

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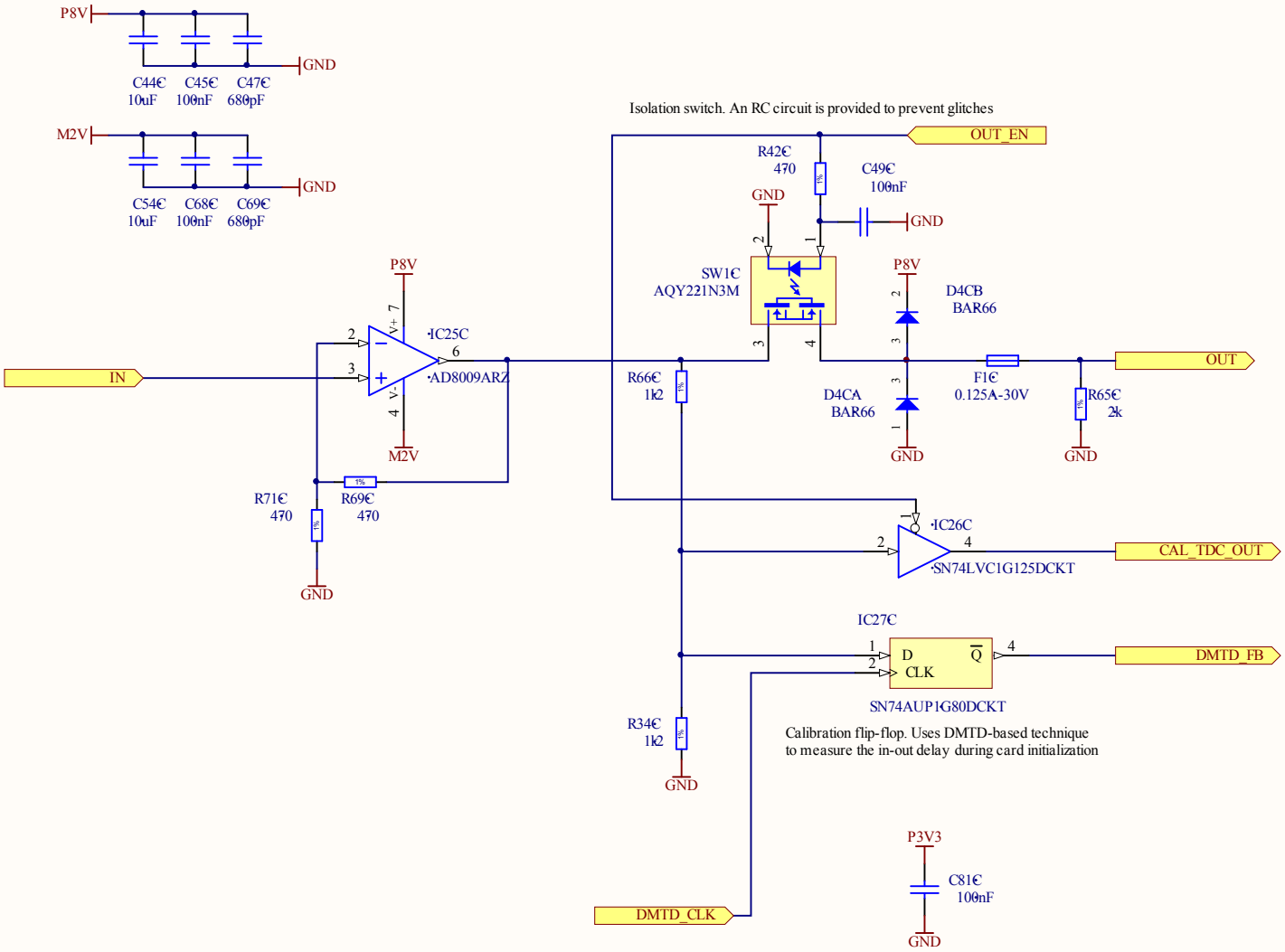
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

Fine Delay FMC
Single output channel

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Designer	TW	
Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
Print Date	2/28/2012 1:57:24 PM	Sheet 10 of 10

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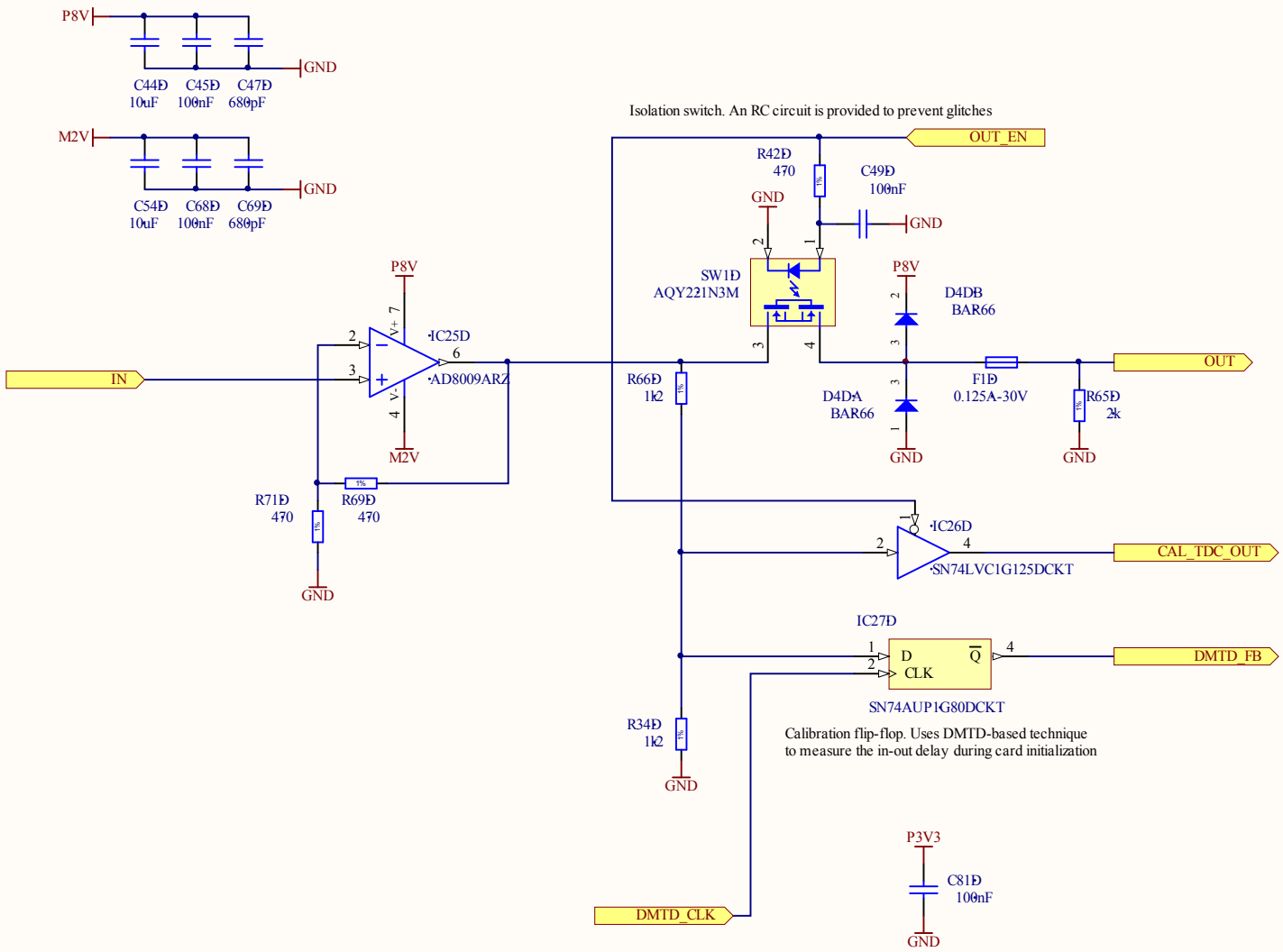
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document: **Fine Delay FMC**
Single output channel

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CH-1211 Geneve 23 - Switzerland

Designer	TW	
Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
Print Date	2/28/2012 1:57:24 PM	Sheet 10 of 10

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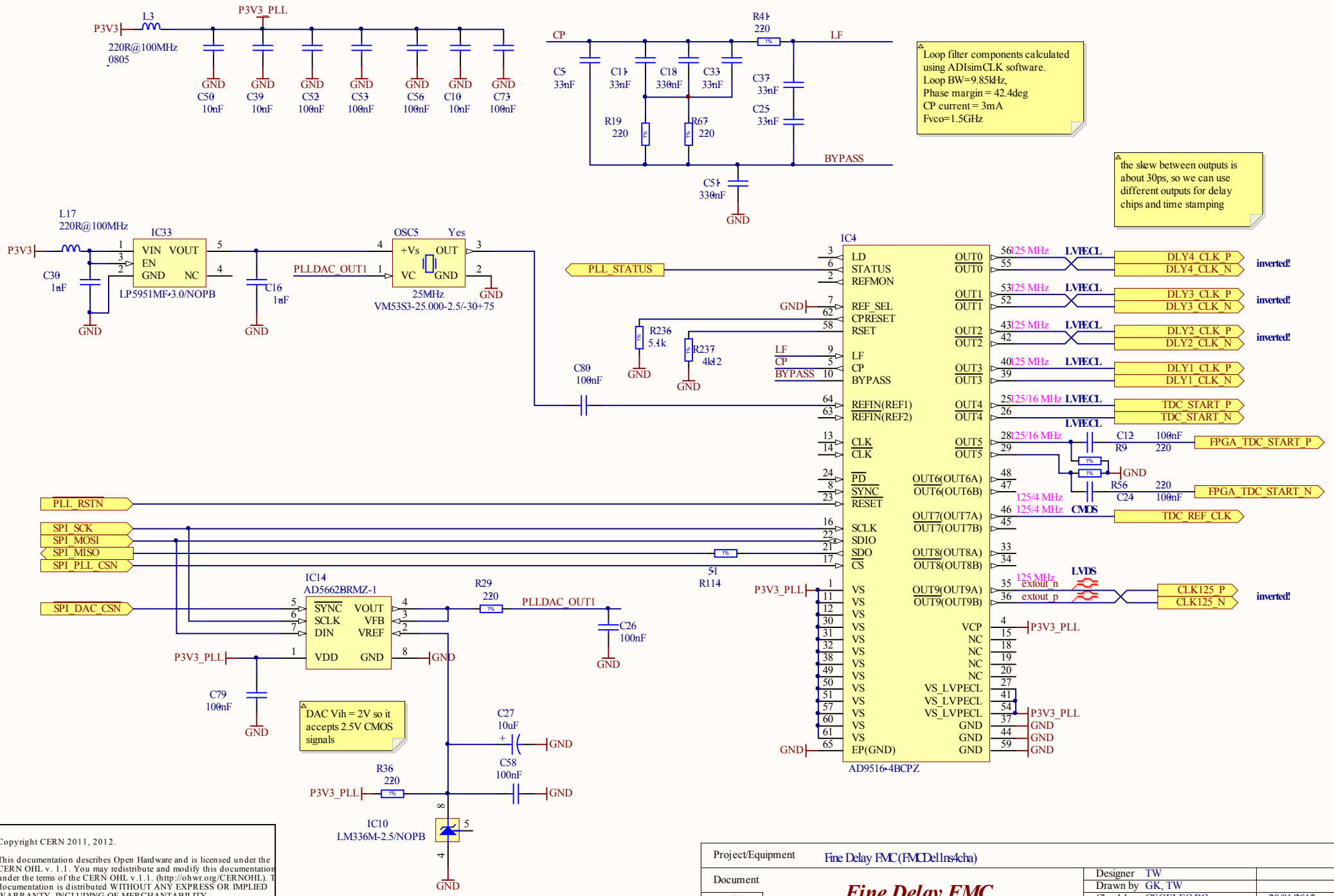
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

Fine Delay FMC
PLL & clock distribution

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Designer	TW	
Drawn by	GK, TW	
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	clock_generator.SchDoc	
Print Date	2/28/2012 1:57:24 PM	Sheet 2 of 10

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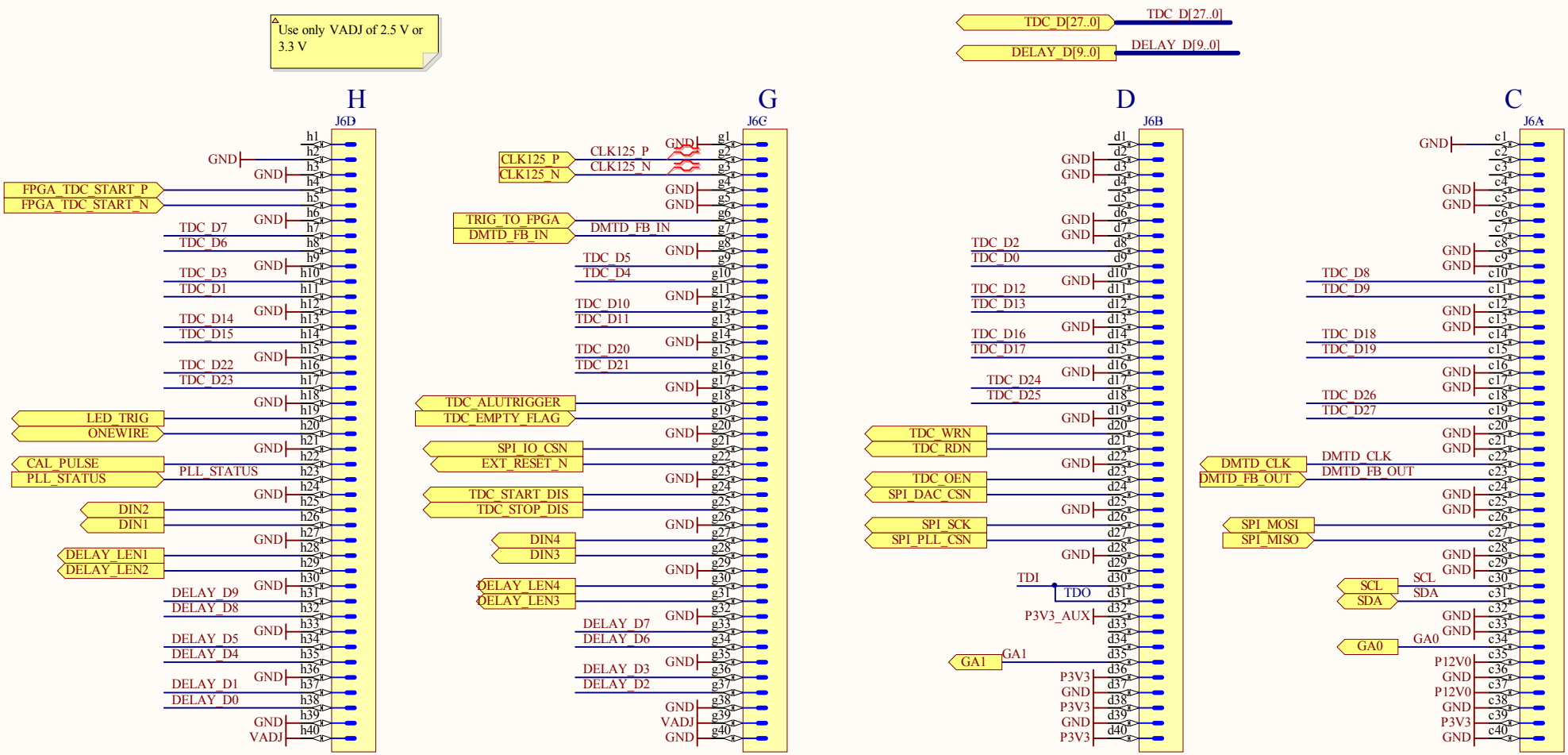
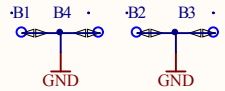
Size A4 | Rev -

Use only VADJ of 2.5 V or 3.3 V





B1 ... B4
screw holes for attaching the FMC to the carrier board.

FTG1 ... FTG6
Reference points for the component mounting machine.

Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

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Fine Delay FMC
FMC connector wiring

European Organization for Nuclear Research
CH-1211 Geneve 23 - SwitzerLA_Pd

Designer	GK, TW	
Drawn by	GK, TW	10/07/2010
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	fmc_connector.SchDoc	
Print Date	2/28/2012 1:57:24 PM	Sheet 3 of 10

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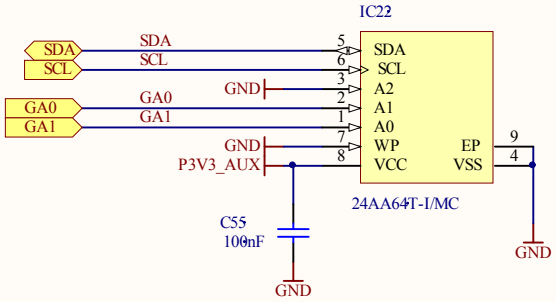
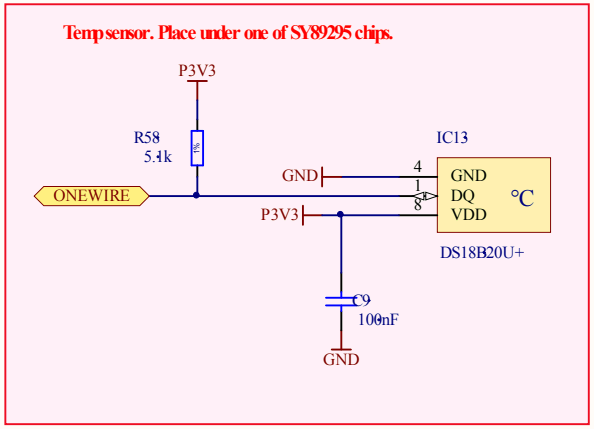
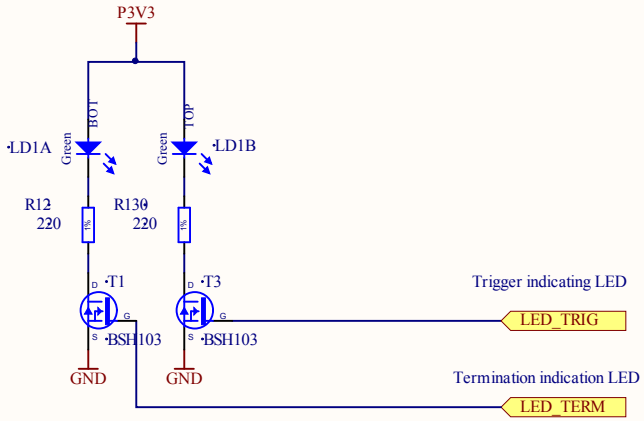
Size A4 | Rev -

24AA64T = 1 0 1 0 0 GA0 GA1
Place the temperature sensor under one of the delays







Project/Equipment	Fine Delay FMC (FMCDel1ns4cha)
Document	

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Fine Delay FMC
LEDs, sensors and ID EEPROM

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Designer	GK, TW	
Drawn by	GK, TW	18/01/2012
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	leds_mem_sensor.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 4 of 10

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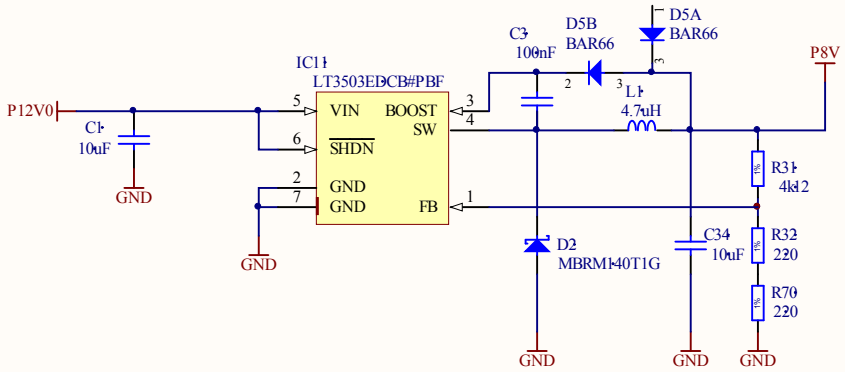
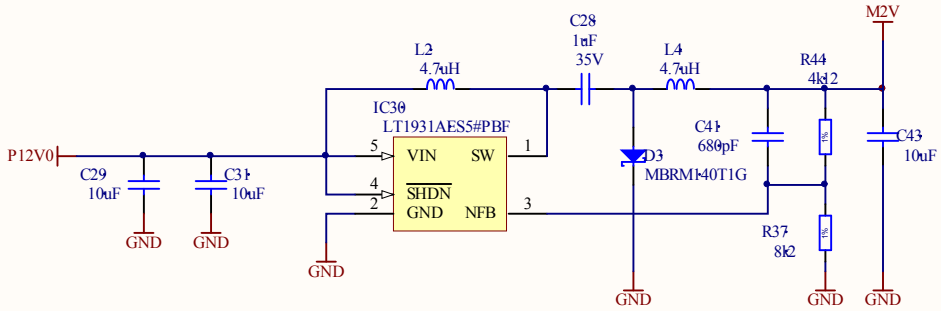
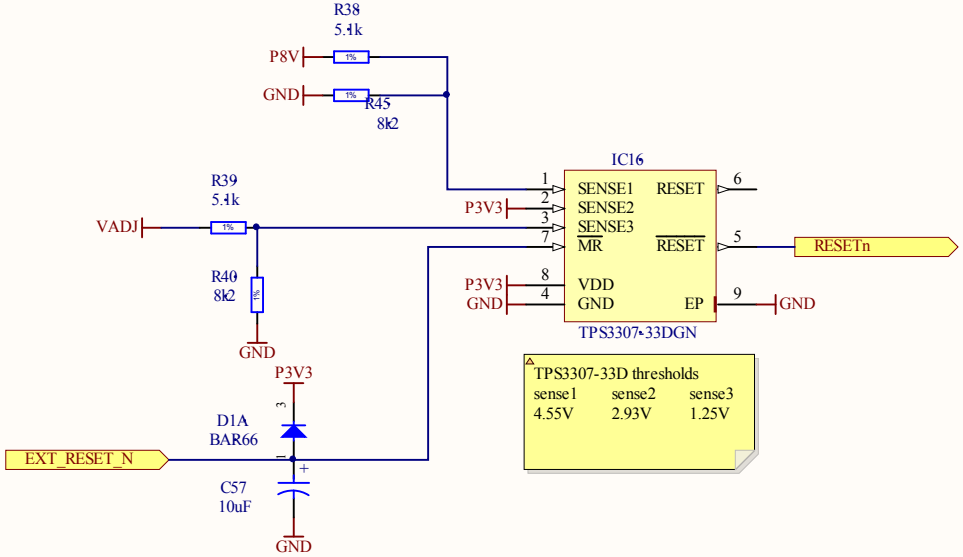
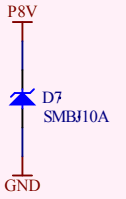
Size A4 | Rev -







10 V transil to protect the PSU/drivers when overvoltage on output



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

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Fine Delay FMC
Power supply & supervisor

Designer	TW, GK	
Drawn by	TW, GK	18/01/2012
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	power_supply.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 5 of 10

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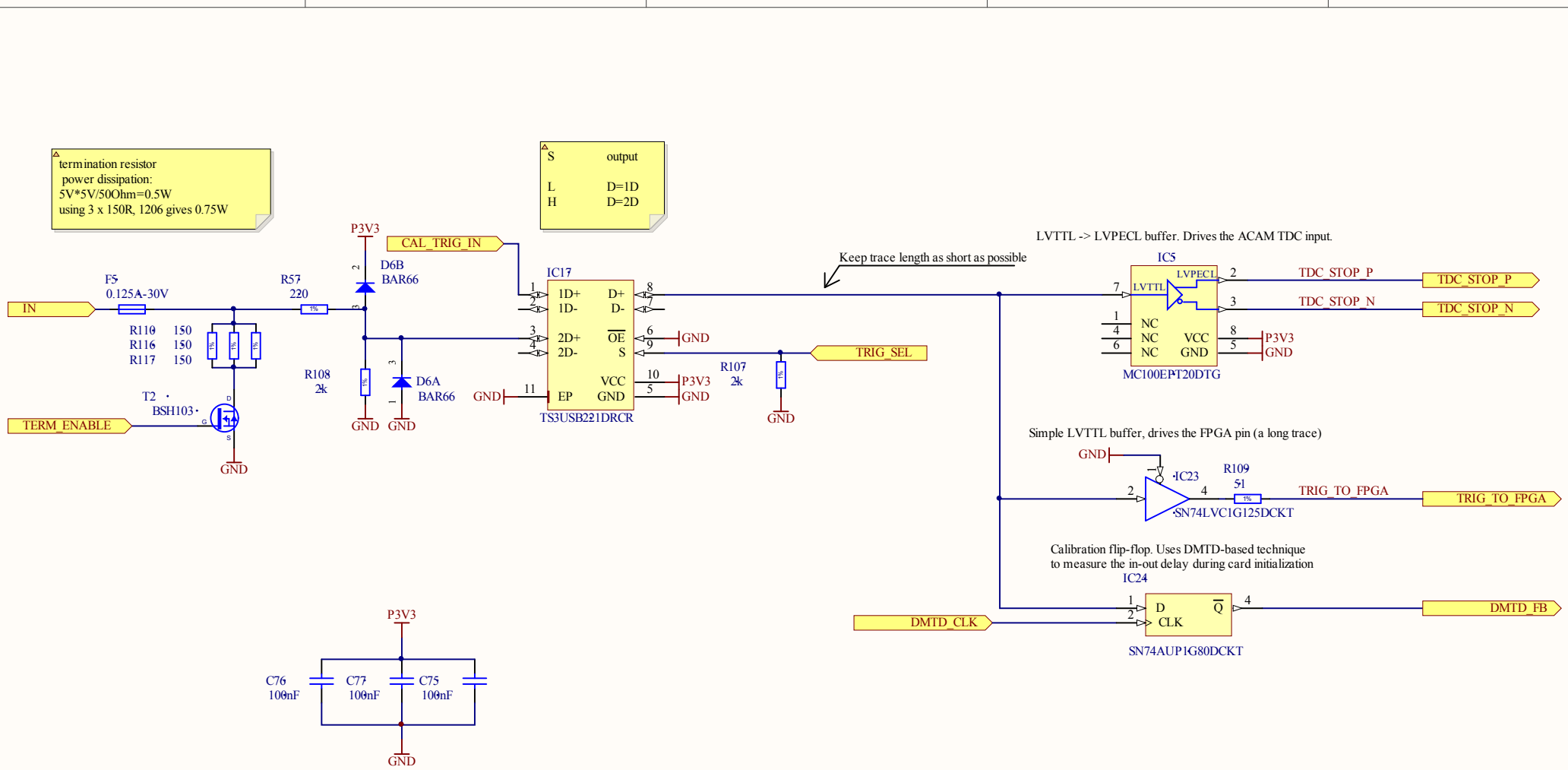
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document: **Fine Delay FMC**
Input stage logic

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Designer	TW, GK	
Drawn by	TW, GK	19/01/2012
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	input_stage.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 6 of 10

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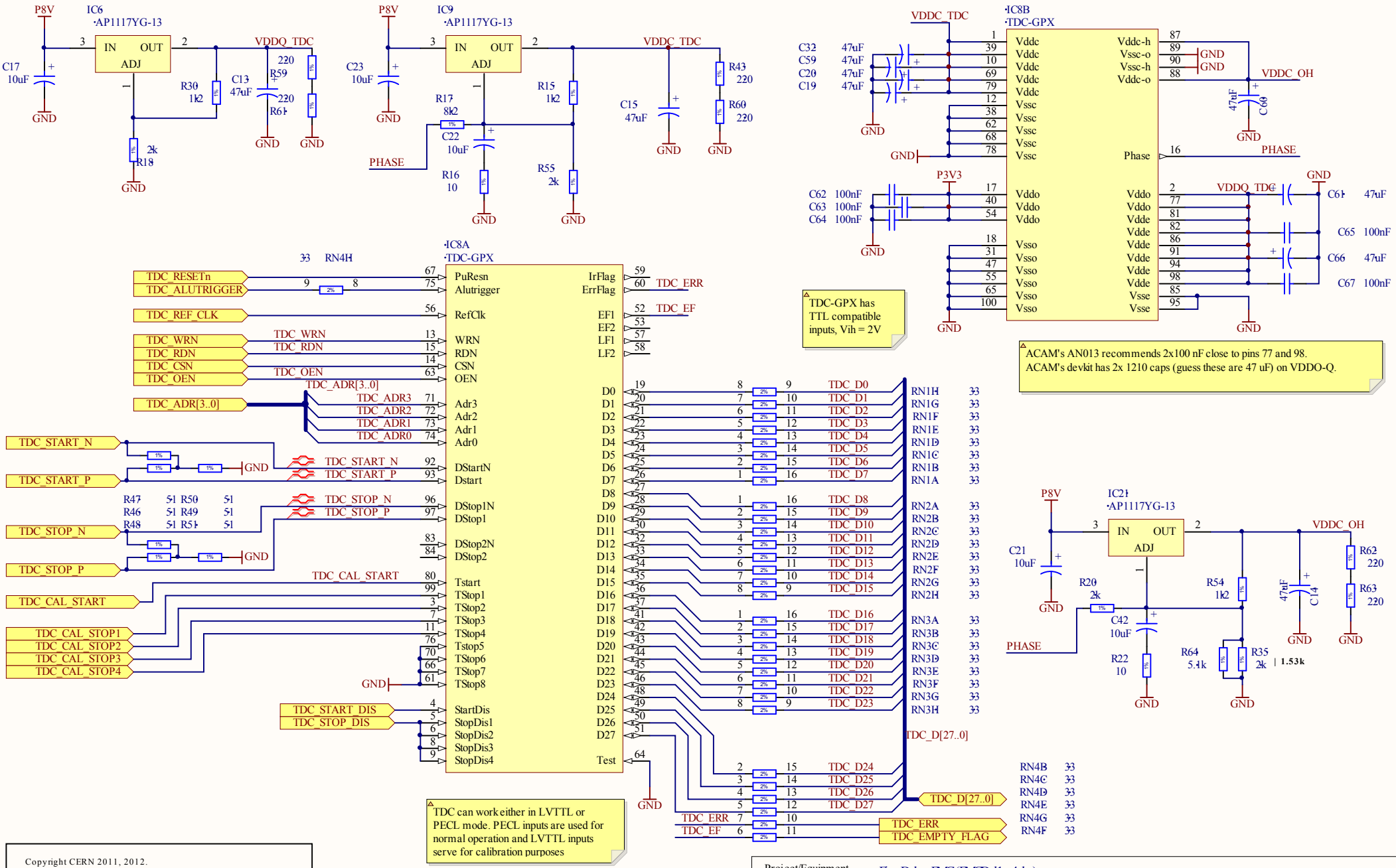
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

Fine Delay FMC
ACAM TDC + power supply

Designer	TW, GK	
Drawn by	TW, GK	01/01/2011
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	acam_tdc.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 7 of 10

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European Organization for Nuclear Research
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EDA-02267-V4-0

Size A4 | Rev -

MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used

IC3 power
P3V3
10 VCC
20 VCC
C4A 10nF
GND
FF_VBB
3 VBB
11 VEE
C35A 100nF
C71A 100nF

VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV (or 2k2 resistor to GND) - LVTTL Mode (Note 5)

IC3AA
MC100EP29DTG
DIN1
R1A
CLK1_P
CLK1_N
R/S inputs are low if unconnected
R8A
R10A
R13A

IC2A
SY89295UMG
DELAY_LEN1
D1_P
D1_N
DELAY_D0
DELAY_D1
DELAY_D2
DELAY_D3
DELAY_D4
DELAY_D5
DELAY_D6
DELAY_D7
DELAY_D8
DELAY_D9
R11A 2k
R2A R3A R6A
R4A R5A R7A
Q1_P
Q1_N

IC1AA
SY100EP23LZG
OUT1
C6A C7A C8A 100nF

IC3AB
MC100EP29DTG
DIN2
R52A
CLK2_P
CLK2_N
R14A R21A R27A
FF_VBB
DELAY_D[9..0]

IC7A
SY89295UMG
DELAY_LEN2
D2_P
D2_N
R53A 2k
R23A R24A R28A
R25A R26A R33A
Q2_P
Q2_N

IC1AB
SY100EP23LZG
OUT2
C36A C38A C46A 100nF

D inputs are reversed in IC7 to simplify PCB routing.

Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)
Document

Fine Delay FMC
Programmable delay line

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European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

Designer	TW, GK	
Drawn by	TW, GK	13/07/2011
Check by	CEGELEC BC	18/01/2012
Last Mod.	-	2/28/2012
File	delay_channel.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 8 of 10

EDA-02267-V4-0

Size A4 | Rev -

MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used

IC3 power

P3V3 10 VCC 20 VCC
C4B 10nF FF_VBB 3 VBB 11 VEE
GND
C35B 100nF C71B 100nF

VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV (or 2k2 resistor to GND) - LVTTL Mode (Note 5)

IC3BA
MC100EP29DTG

DIN1 51 R1B FF_VBB
CLK1_P CLK1_N
R8B R10B R13B GND

R/S inputs are low if unconnected

IC2B
SY89295UMG

DELAY_LEN1
D1_P D1_N
DELAY_D0 DELAY_D1 DELAY_D2 DELAY_D3 DELAY_D4 DELAY_D5 DELAY_D6 DELAY_D7 DELAY_D8 DELAY_D9
R2B R3B R6B R4B R5B R7B
Q1_P Q1_N
R11B 2k

IC1BA
LVPECL LVTTL
SY100EP23LZG
OUT1
C6B 100nF C7B 100nF C8B 100nF P3V3
C48B 100nF

IC1BB
LVPECL LVTTL
SY100EP23LZG
OUT2
C36B 100nF C38B 100nF C46B 100nF P3V3

IC3BB
MC100EP29DTG

DIN2 51 R52B FF_VBB
CLK2_P CLK2_N
R14B R21B R27B

IC7B
SY89295UMG

DELAY_LEN2
D2_P D2_N
R23B R24B R28B
Q2_P Q2_N
R53B 2k
R25B R26B R33B

DELAY_D[9..0]

D inputs are reversed in IC7 to simplify PCB routing.

Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)
Document

Fine Delay FMC
Programmable delay line

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European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

Designer	TW, GK	
Drawn by	TW, GK	13/07/2011
Check by	CEGELEC BC	18/01/2012
Last Mod.	-	2/28/2012
File	delay_channel.SchDoc	
Print Date	2/28/2012 1:57:26 PM	Sheet 8 of 10

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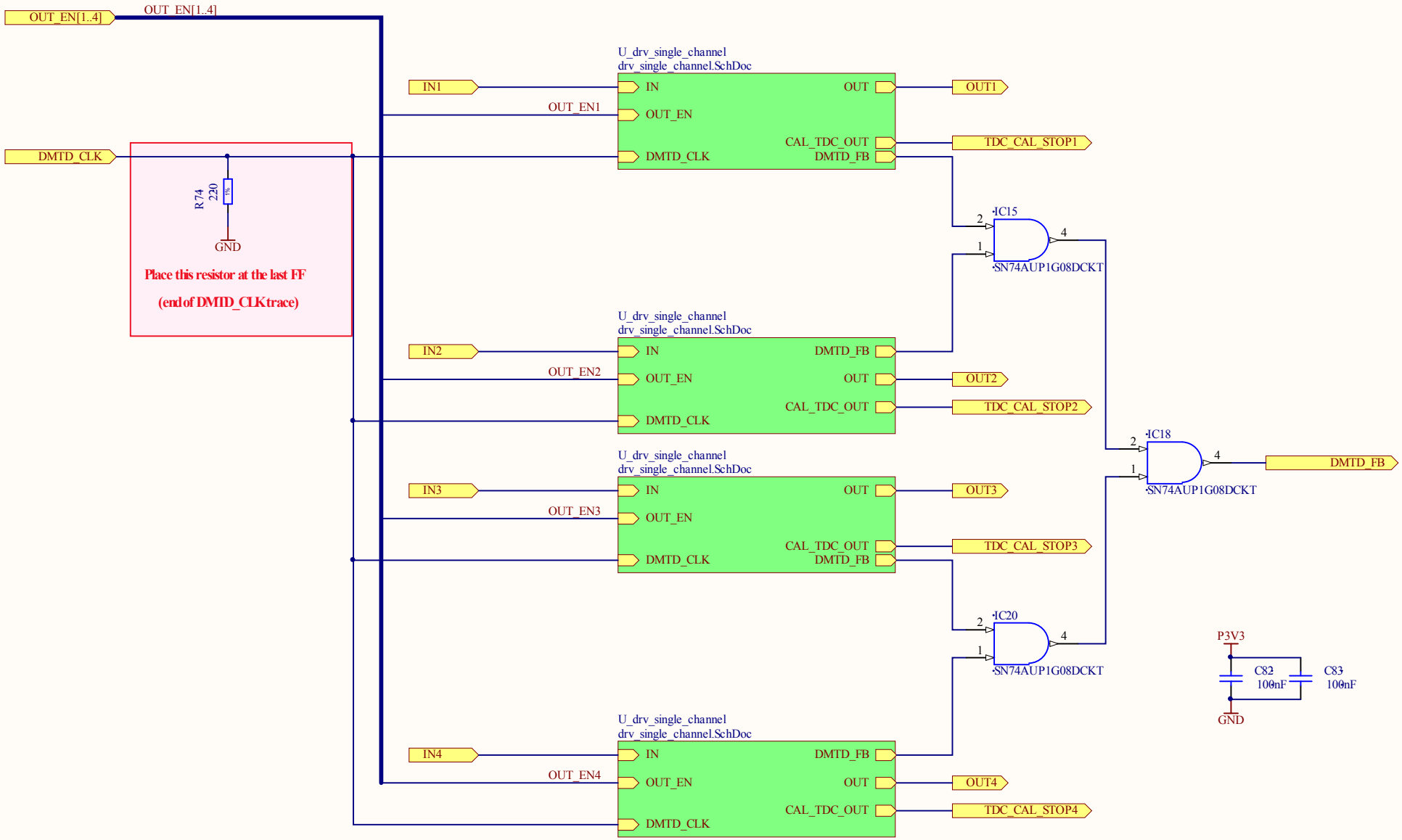
Size A4 | Rev -



Project/Equipment: Fine Delay FMC (FMCDel1ns4cha)

Document

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Fine Delay FMC
Output buffer/driver (all channels)

European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

Designer	TW	
Drawn by	TW	01/12/2011
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	output_driver.SchDoc	
Print Date	2/28/2012 1:57:26 PM	Sheet 9 of 10

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Size A4 | Rev -