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Project/Equipment

Fine Delay FMC(FMDelIns4cha)

Document



**Fine Delay FMC
Single output channel**

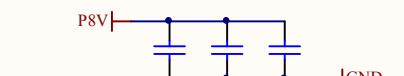
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Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
Print Date	2/28/2012 1:57:23 PM	Sheet 10 of 10

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EDA-02267-V4-0

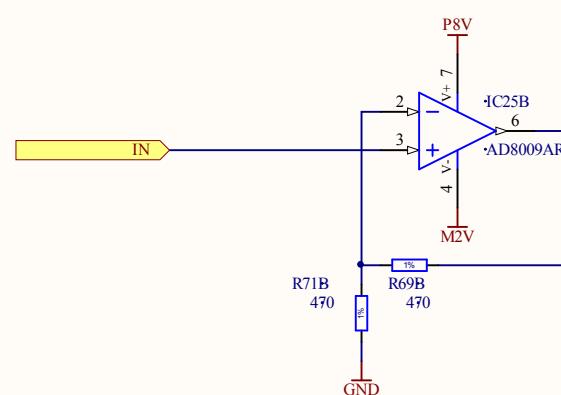
Size Rev
A4 -

A

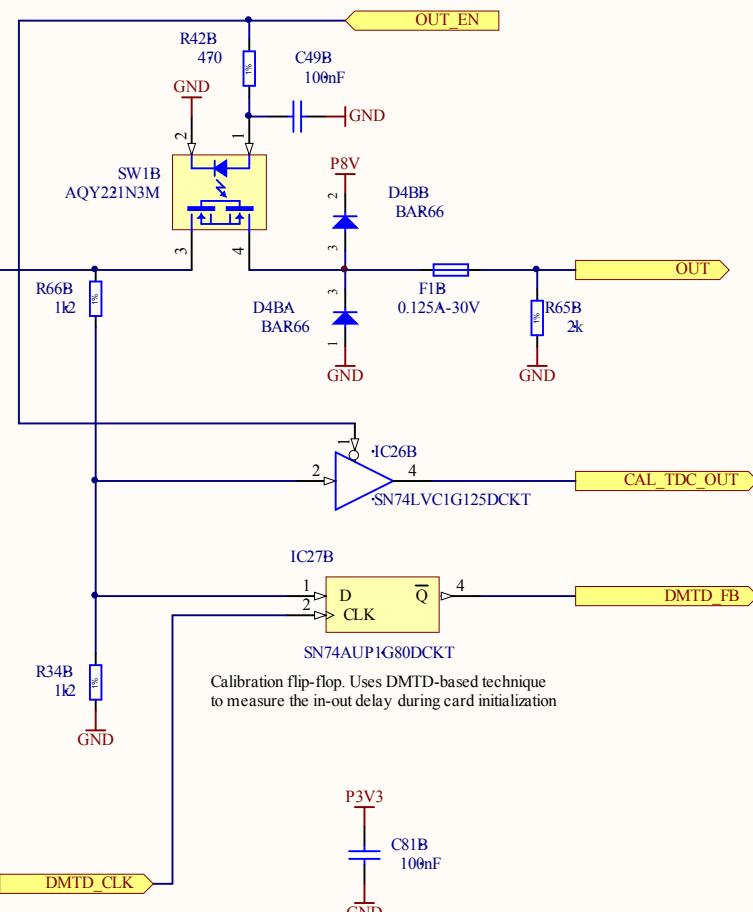


C44B 10 μ F
C45B 100nF
C47B 680pF

C54B 10 μ F
C68B 100nF
C69B 680pF



Isolation switch. An RC circuit is provided to prevent glitches



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Project/Equipment

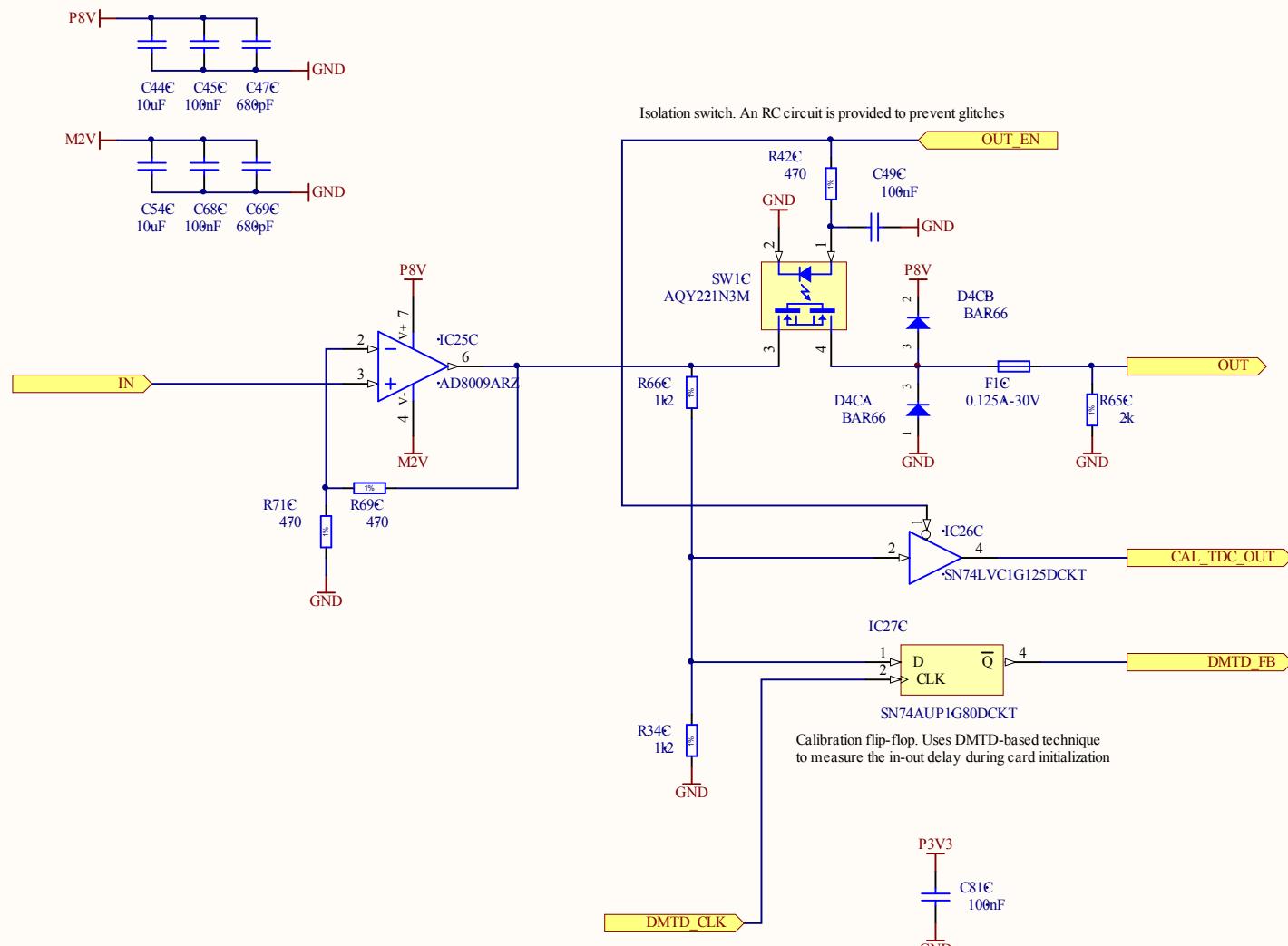
Fine Delay FMC(FMCDeIns4cha)

Document



Fine Delay FMC
Single output channel

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Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
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Project/Equipment

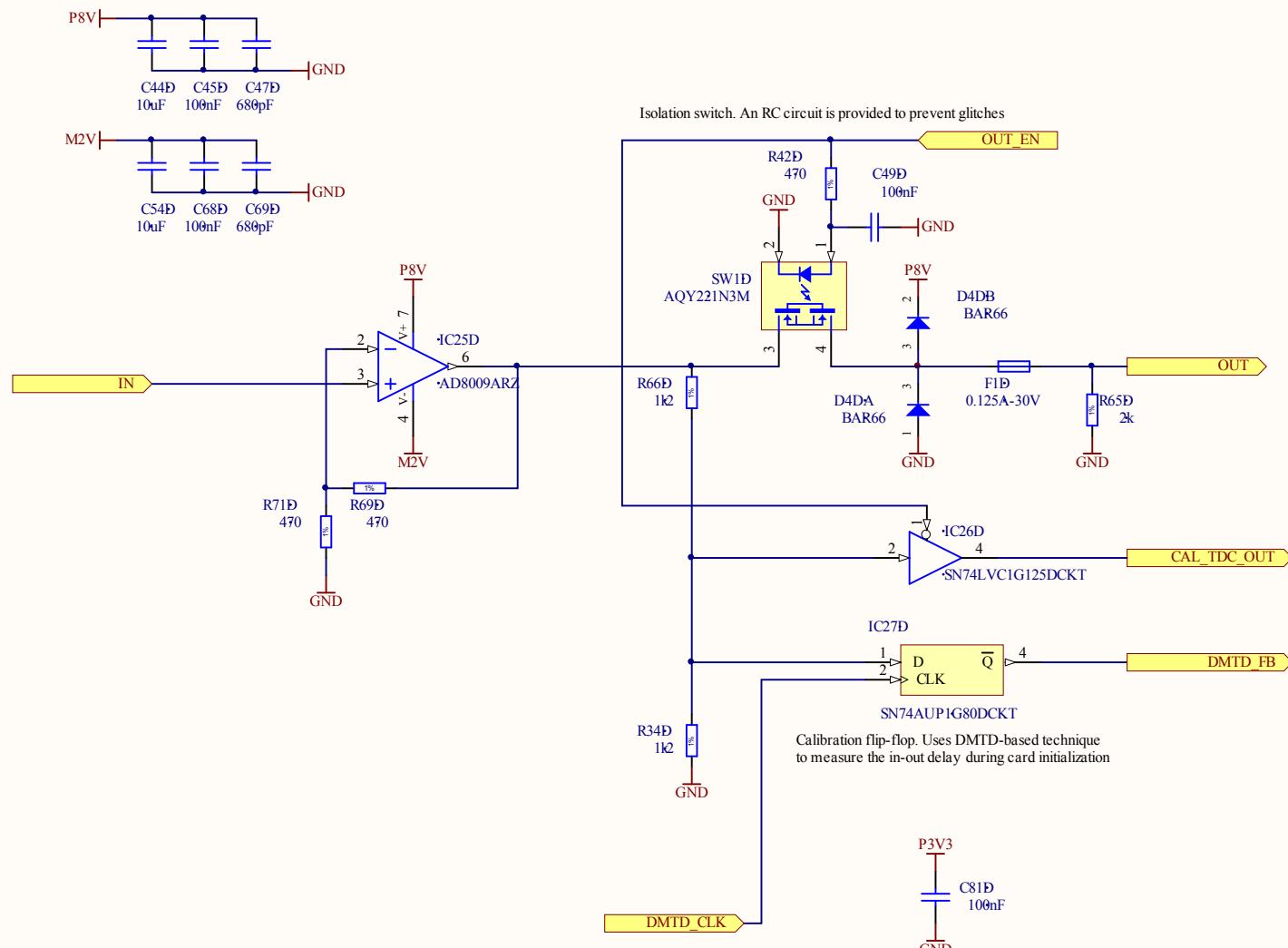
Fine Delay FMC(FMDelIns4cha)

Document



Fine Delay FMC
Single output channel

Designer	TW	19/01/2012
Drawn by	TW	19/01/2012
Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
Print Date	2/28/2012 1:57:24 PM	Sheet 10 of 10
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Project/Equipment

Fine Delay FMC(FMDelIns4cha)

Document

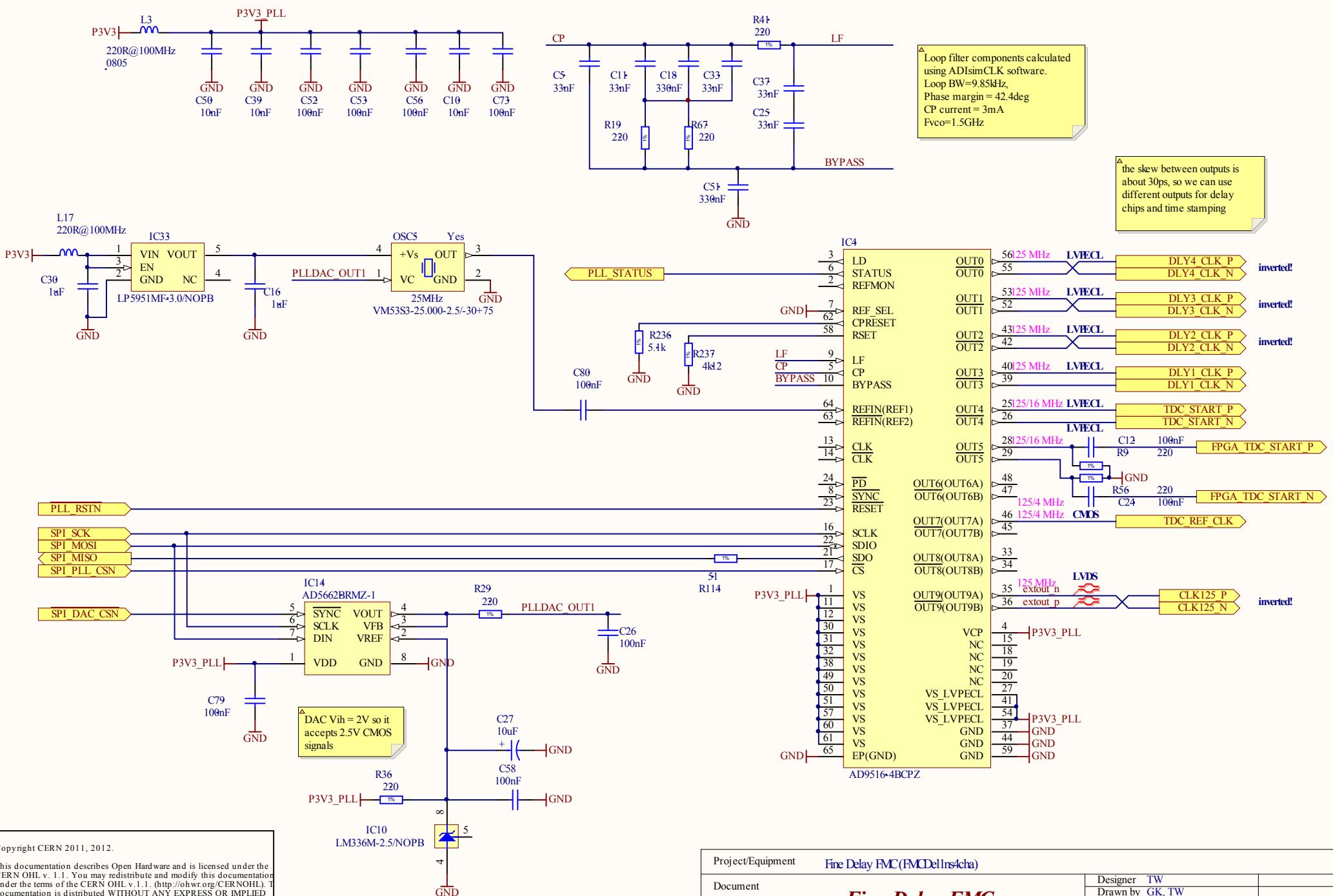


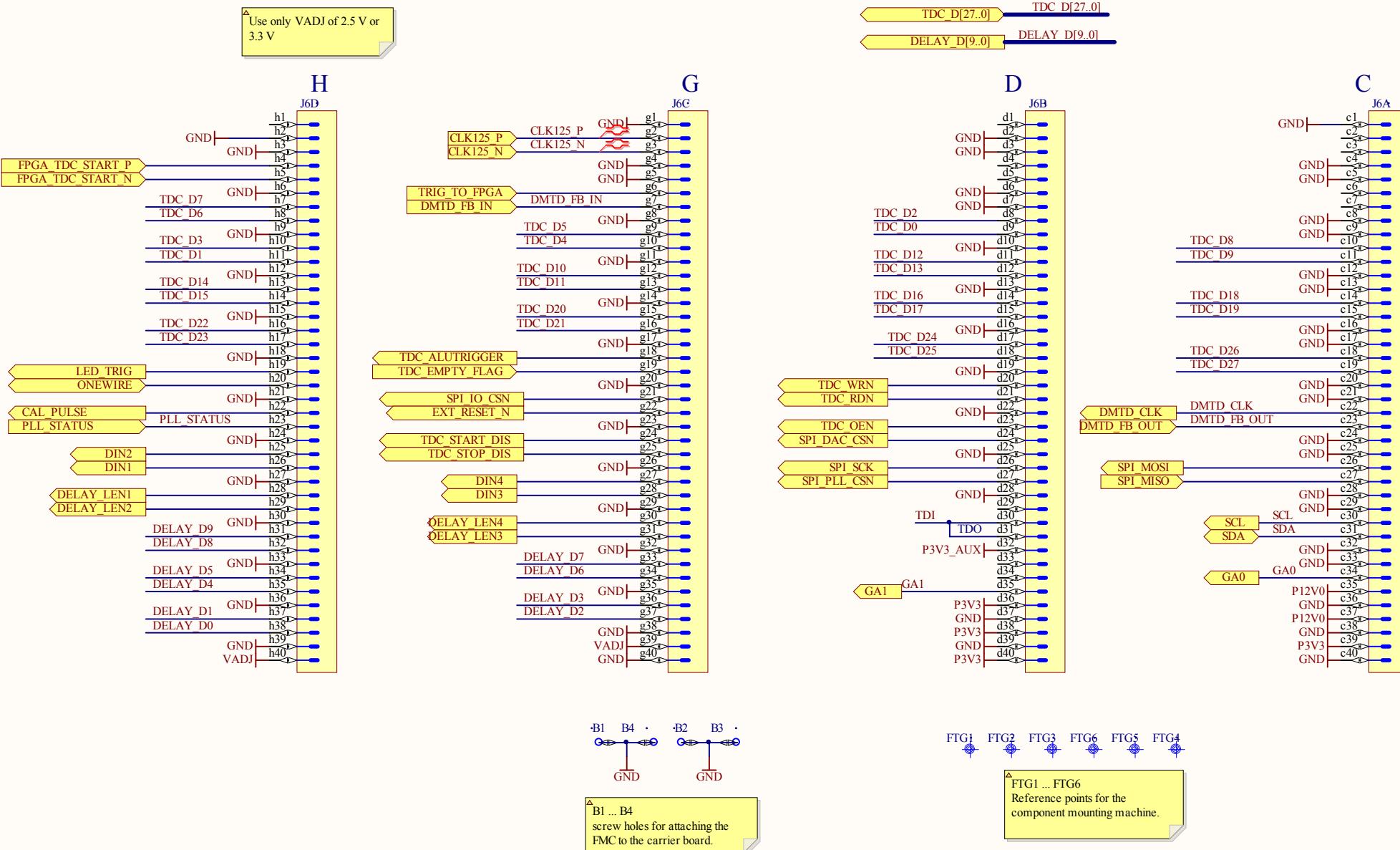
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Checkby	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	drv_single_channel.SchDoc	
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**Fine Delay FMC
Single output channel**

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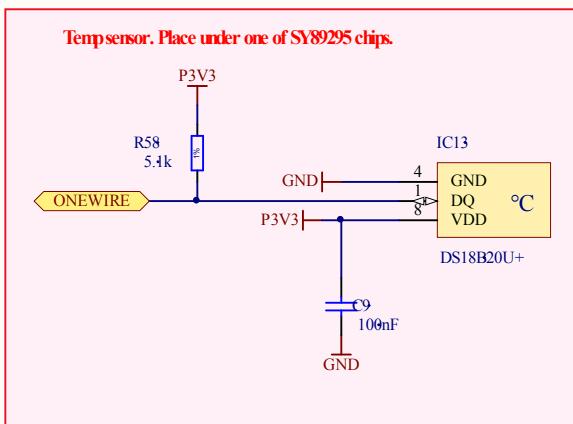
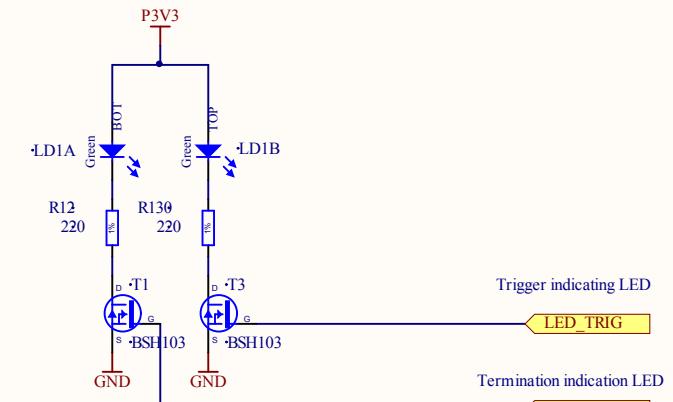
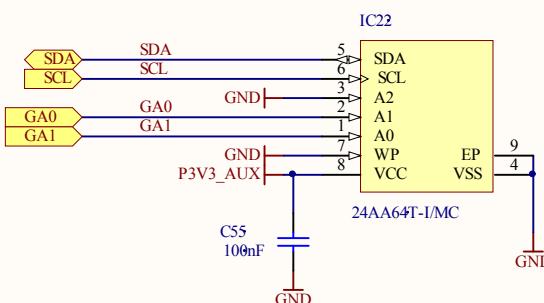
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Project/Equipment	Fine Delay FMC (FMCDe1ns4cha)		
Document		Designer GK, TW	10/07/2010
BE-CO	Fine Delay FMC	Drawn by GK, TW	20/01/2012
	FMC connector wiring	Checkby CEGELEC BC	2/28/2012
		Last Mod. -	File fmc_connector.SchDoc
		Print Date 2/28/2012 1:57:24 PM	Sheet 3 of 10
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland		EDA-02267-V4-0	Size A4 Rev -

A

A

$24AA64T = 1\ 0\ 1\ 0\ 0\ GA0\ GA1$
Place the temperature sensor under one of the delays



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Project/Equipment

Fine Delay FMC(FMCDelIns4cha)

Document



Fine Delay FMC LEDs, sensors and ID EEPROM

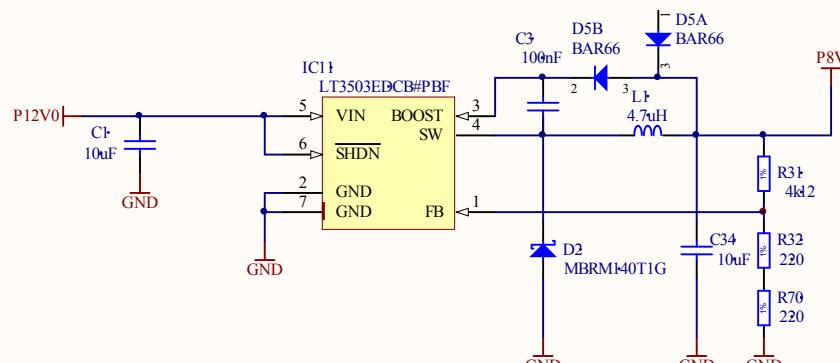
Designer	GK, TW	
Drawn by	GK, TW	18/01/2012
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	leds_mem_sensor.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 4 of 10

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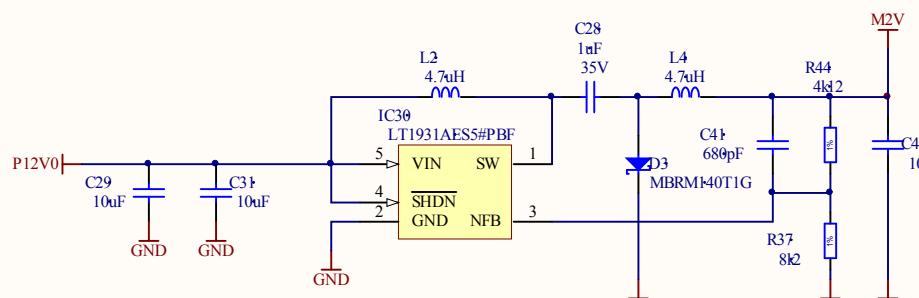
EDA-02267-V4-0

E

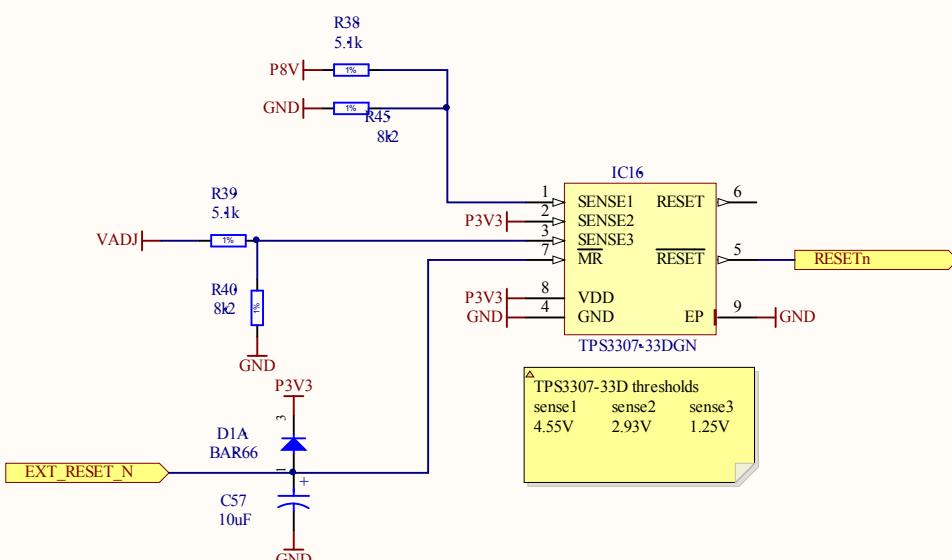
A



B



C



10V transient to protect the PSU/drivers when overvoltage on output

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Project/Equipment Fine Delay FMC(FMCDelIns4cha)

Document

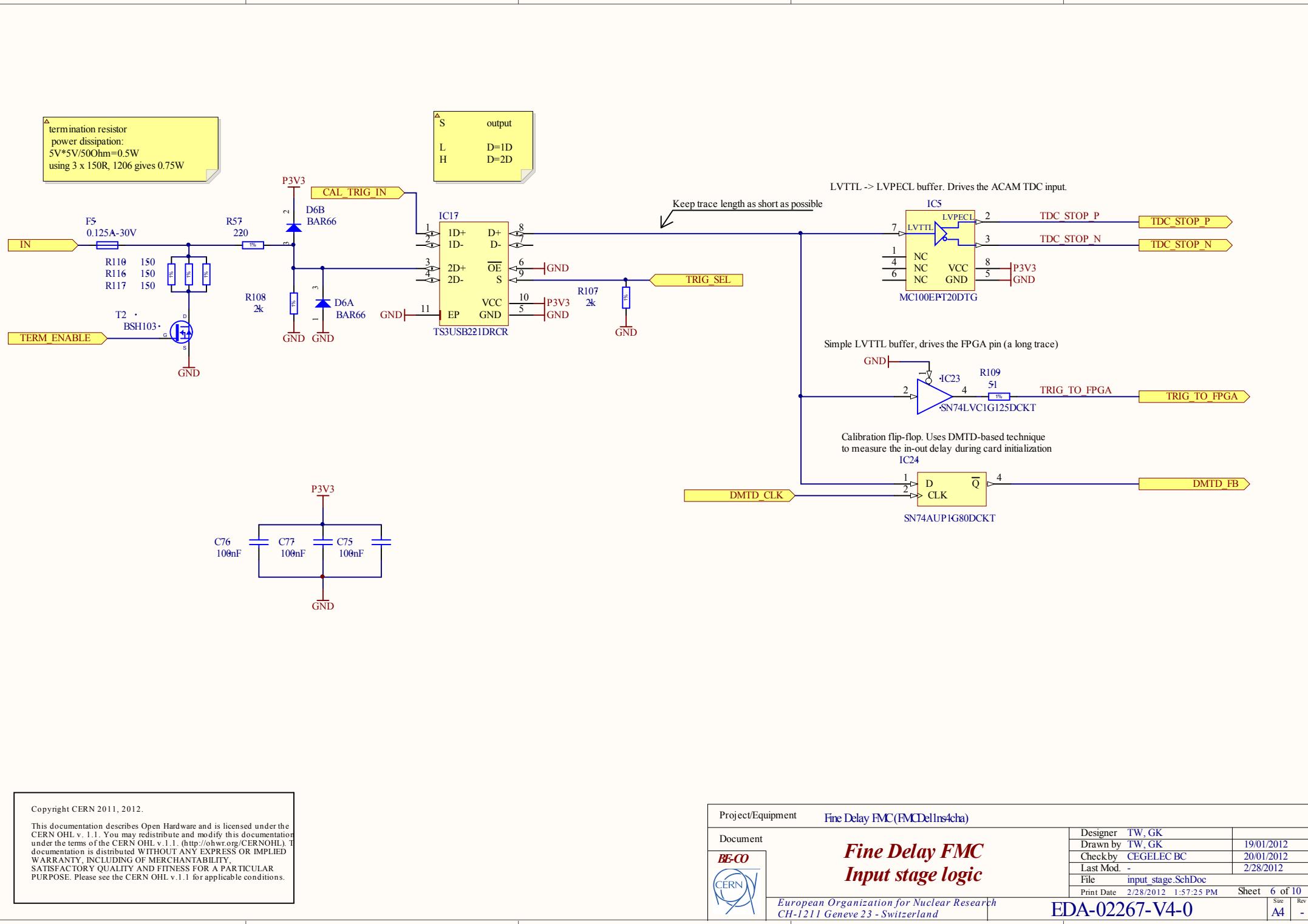


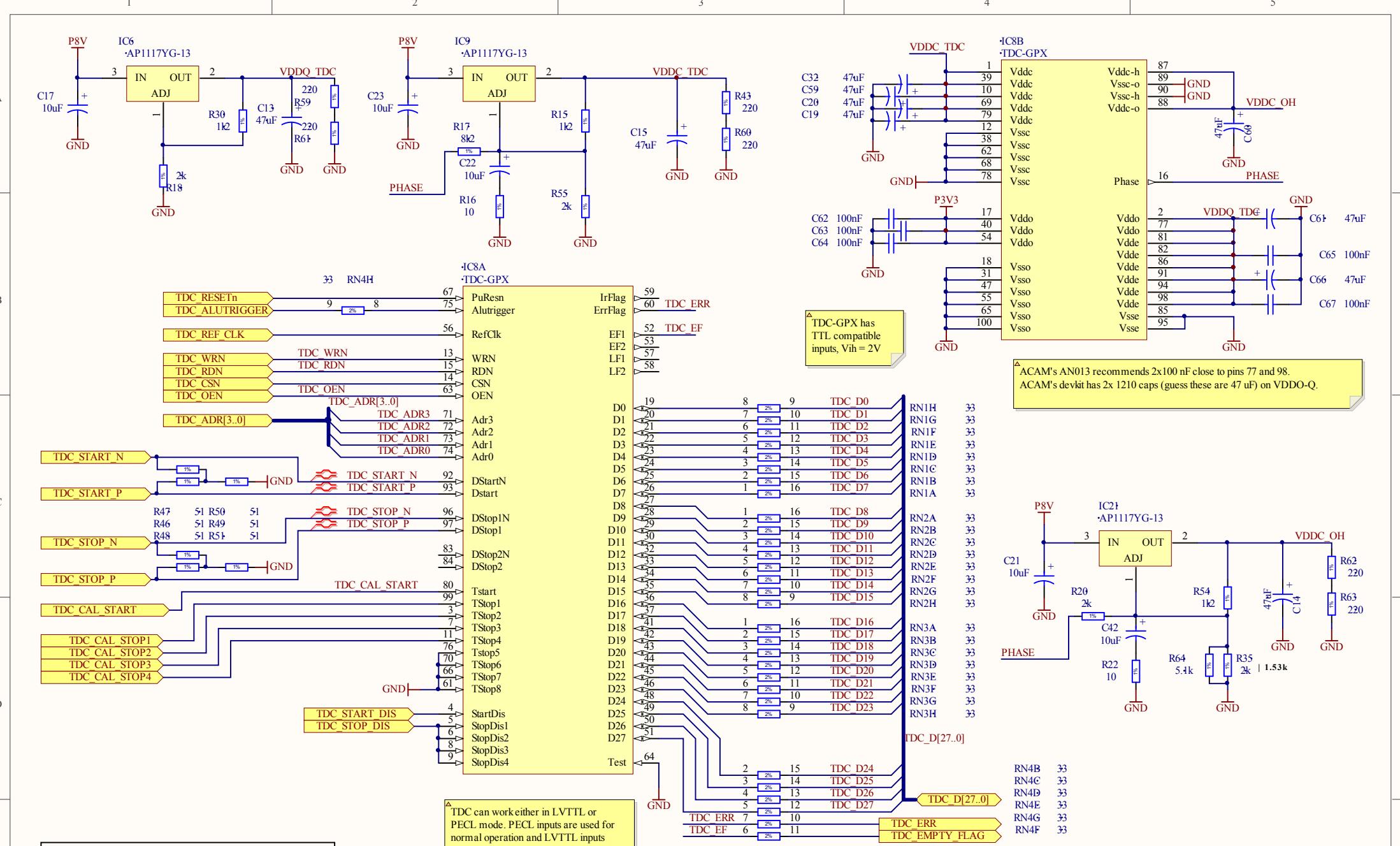
Designer TW, GK
Drawn by TW, GK
Checkby CEGELEC BC
Last Mod. -
File power_supply.SchDoc
Print Date 2/28/2012 1:57:25 PM Sheet 5 of 10

Fine Delay FMC Power supply & supervisor

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EDA-02267-V4-0





Project/Equipment

Fine Delay FMC(FMCDelIns4cha)

Document



Fine Delay FMC

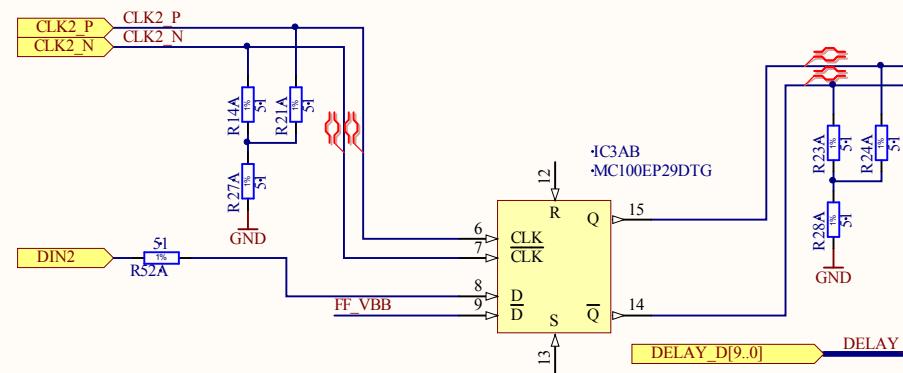
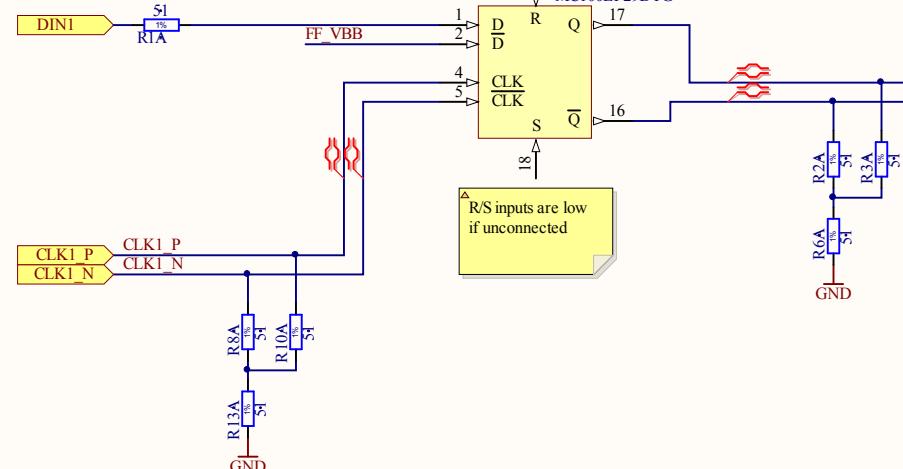
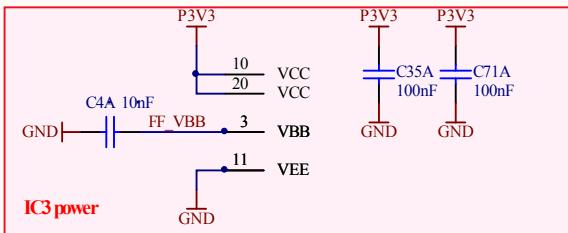
ACAM TDC + power supply

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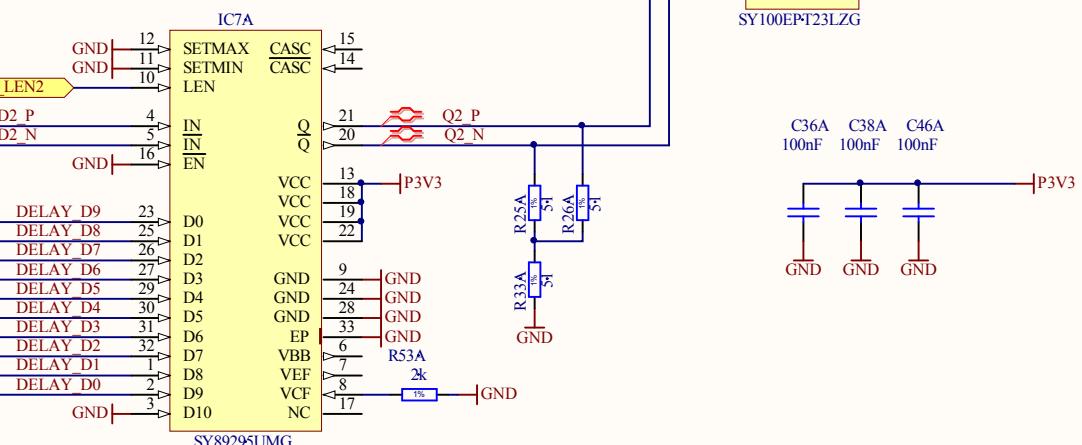
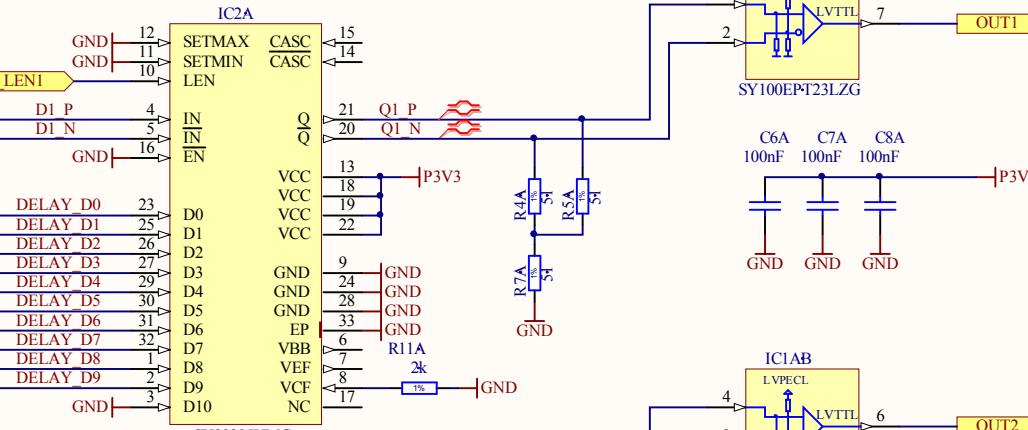
EDA-02267-V4-0

Designer	TW, GK	01/01/2011
Drawn by	TW, GK	
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	acam_tdc.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 7 of 10
Size	A4	Rev -

MC100LVEL input current is about 100..300uA
In order to translate LVCMS to LVPECL/LVDS simple resistive network can be used



VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMS Mode
VCF = 1.5 V +/- 100 mV (or 2k resistor to GND) - LVTTI Mode
(Note 5)



D inputs are reversed in IC7 to simplify PCB routing.

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Project/Equipment Fine Delay FMC(FMCDelIns4cha)

Document



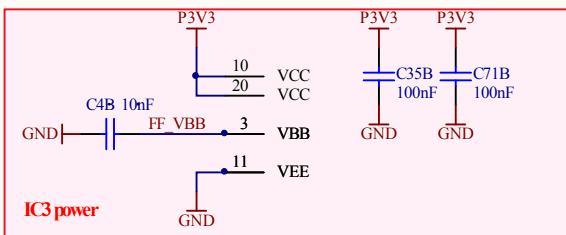
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Fine Delay FMC Programmable delay line

Designer	TW, GK	13/07/2011
Drawn by	TW, GK	
Check by	CEGELEC BC	18/01/2012
Last Mod.	-	2/28/2012
File	delay_channel.SchDoc	
Print Date	2/28/2012 1:57:25 PM	Sheet 8 of 10

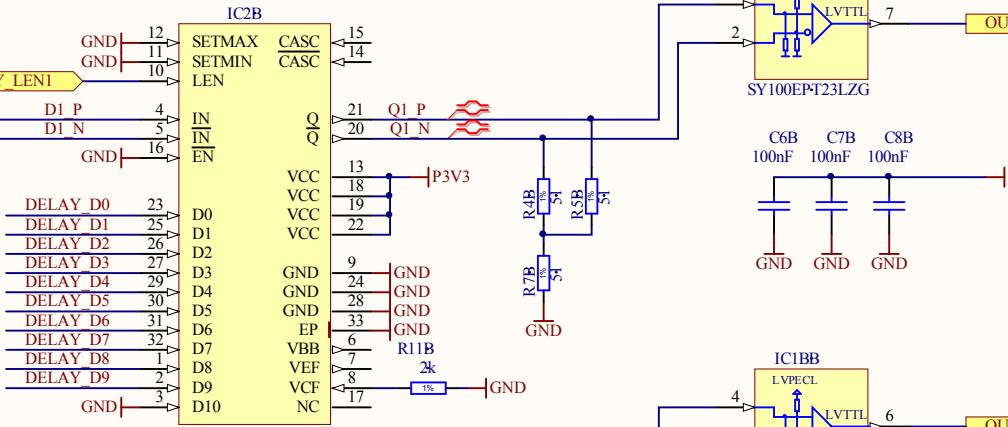
EDA-02267-V4-0

- MC100LVEL input current is about 100..300 μ A
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used



The circuit diagram illustrates a D flip-flop (M74HC108) with its R/S inputs connected to ground. The circuit includes a 2-to-1 multiplexer (M74151) controlled by DIN1, and two inverters (R1B, R2B) with their outputs connected to the R/S inputs of the flip-flop. The clock inputs CLK1_P and CLK1_N are connected to the M74151's data inputs. The M74151's enable input S1 is connected to ground through resistor R13B. The M74151's output is connected to the clock inputs of the flip-flop via resistor R10B. The Q output of the flip-flop is connected to ground through resistor R6B.

△ VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV (or 2k Ω resistor to GND) - LVTTL Mode
(Note 5)



The diagram shows the internal circuitry of the SY100EPT23LZG driver. It consists of two main integrated circuits: IC7B and SY80205UMC.

- IC7B:** This section contains a driver stage. The inputs include LEN2 (pin 12), SETMAX (pin 11), SETMIN (pin 10), IN (pin 4), IN (pin 5), EN (pin 16), and various delay lines labeled DELAY D9 through DELAY D0 (pins 23, 25, 26, 27, 29, 30, 31, 32, 1, 2, 3 respectively).
- SY80205UMC:** This section contains a driver stage. The inputs include LEN (pin 15), CASC (pin 14), Q (pin 21), Q (pin 20), Q2 P (pin 2), Q2 N (pin 1), VCC (pins 13, 18, 19, 22), GND (pins 9, 24, 28, 33), EP (pin 6), VBB (pin 7), VEF (pin 8), VCF (pin 9), and NC (pin 17).
- Output Stage:** The outputs from IC7B and SY80205UMC are connected to a common-emitter stage. The collector of this stage is connected to the primary winding of a transformer (indicated by a yellow box labeled 'SY100EPT23LZG').
- Filtering and Decoupling:** The circuit includes three capacitors connected to ground: C36B (100nF), C38B (100nF), and C46B (100nF). These capacitors are labeled P3V3, P3V3, and P3V3 respectively.

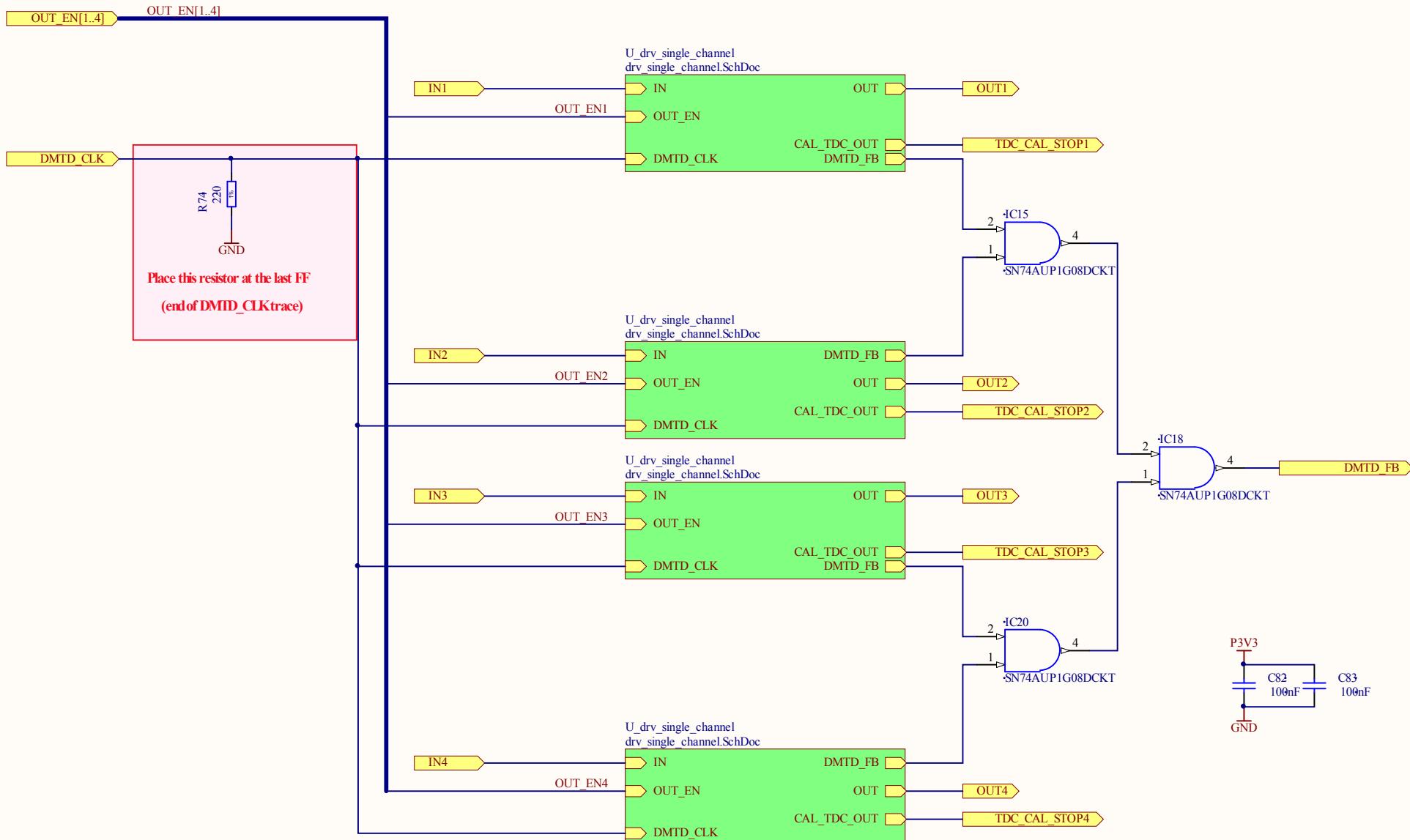
⚠ D inputs are reversed in IC7 to simplify PCB routing.

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		Check by CEGELEC BC	18/01/2012
		Last Mod. -	2/28/2012
		File delay_channel.SchDoc	
		Print Date 2/28/2012 1:57:26 PM	Sheet 8 of 10
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Project/Equipment

Document



Fine Delay FMC(FMCDelIns4cha)

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Drawn by	TW	
Check by	CEGELEC BC	20/01/2012
Last Mod.	-	2/28/2012
File	output_driver.SchDoc	
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Fine Delay FMC

Output buffer/driver (all channels)

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