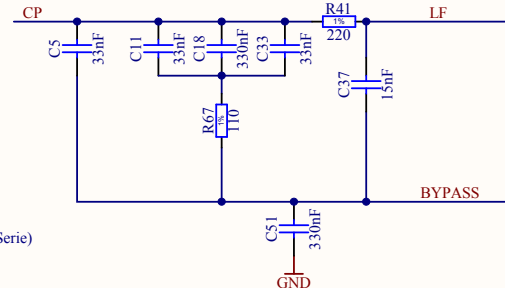
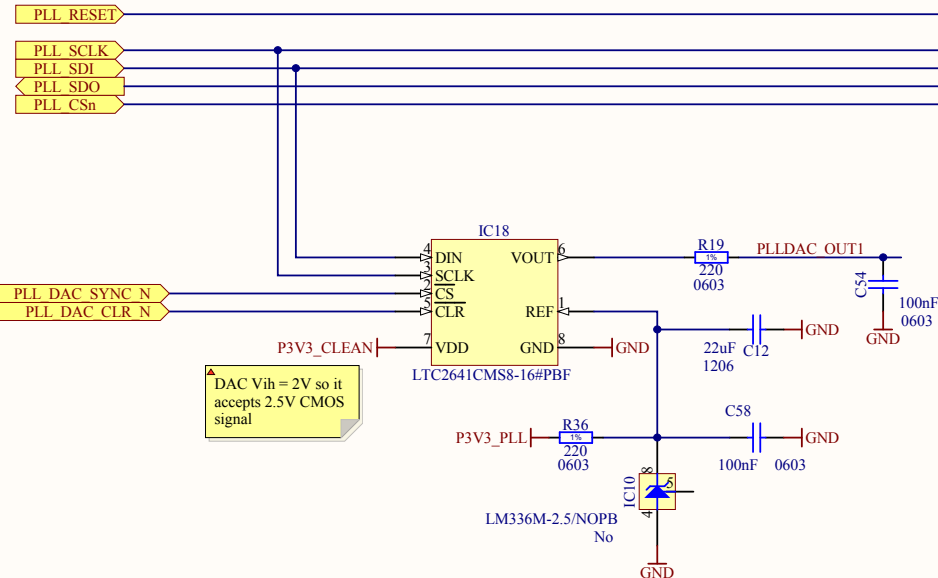
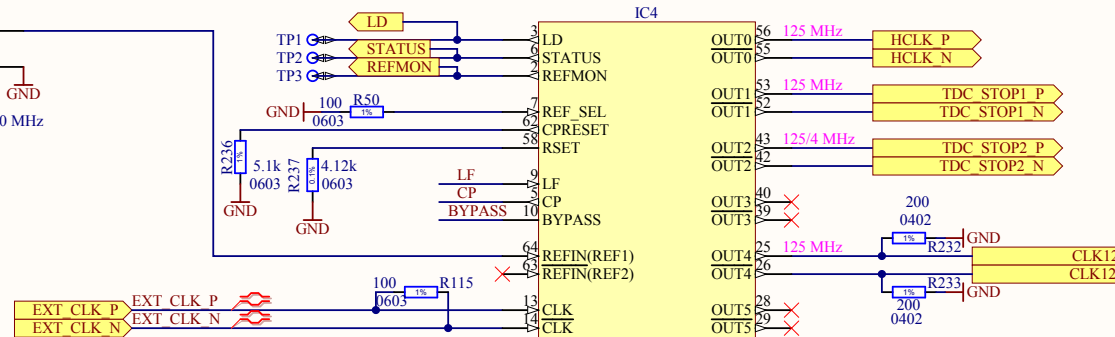
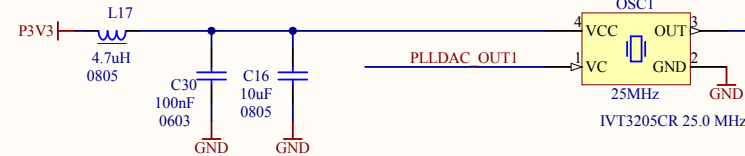


Default mode:
TDC in R-Mode, 40MHz per channel. TDC driven by 125MHz/4 clock.
START: trigger
STOP: 125/4 clock delivered to STOP1 input
125MHz clock delivered to STOP1 input
27ps resolution.
trigger positions in reference with both 125MHz and 125/4 clocks can be captured




Calibration mode:
TDC in I-Mode,
LVTTTL inputs, 10MHz max, TDC driven by 10MHz clock
START: 10MHz clock delivered to TDC_CAL_START
STOP: buffer output
81ps resolution



OSC_25MHZ_RAKON_IVT3205CR



- the skew between outputs is about 5ps, so we can use two different outputs for delay chip and time stamping

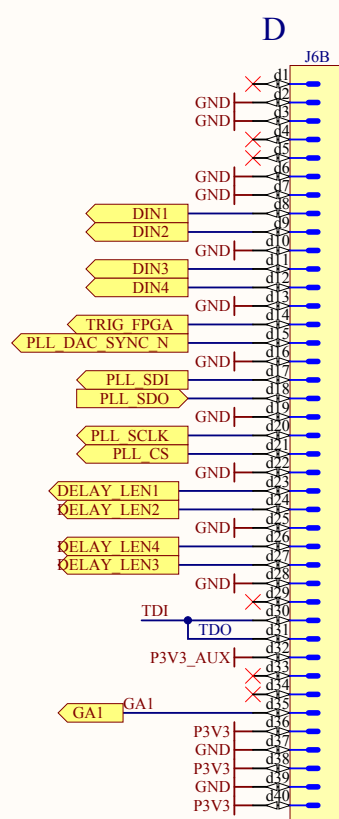
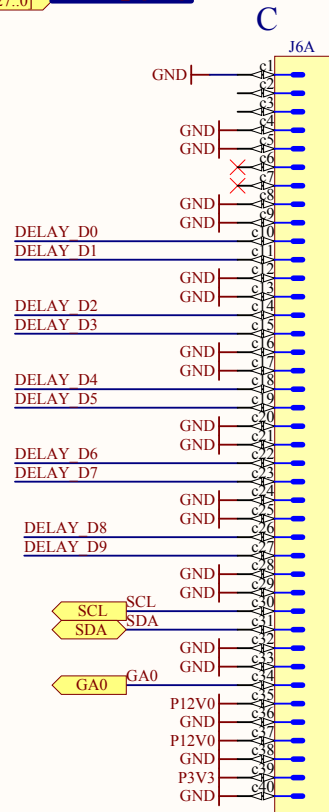
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		Print Date	2010-11-24 20:16:10
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		Size	A4
		Rev	-

TDC_ADR[3..0]
TDC_D[27..0]

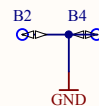
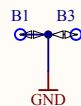
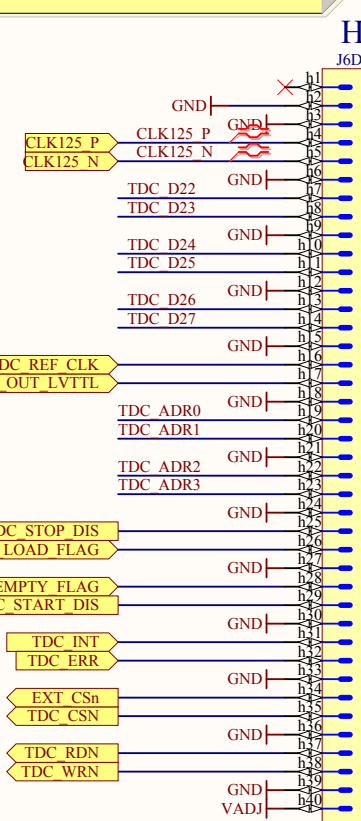
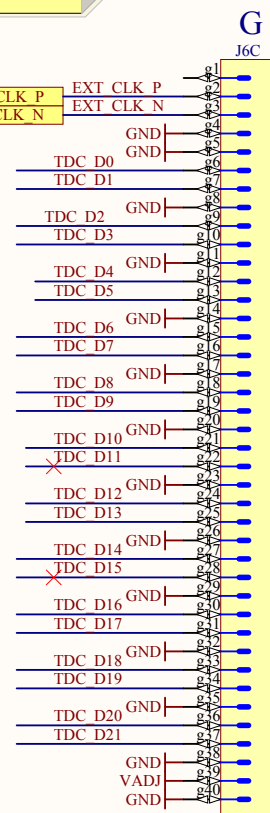
DELAY_D[9..0]
DELAY_D[9..0]

VREF MUST BE 2.5V

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.



EXT_CLK_P
EXT_CLK_N



B1 ... B4
screw holes for mounting the
FmcAde to the carrier board.



FTG1 ... FTG6
Reference points for the
component mounting machine.

Project/Equipment FMC Delay 1ns 4cha

Document

BE-CO



SAMTEC VITA 57
Low Pin Count Connector

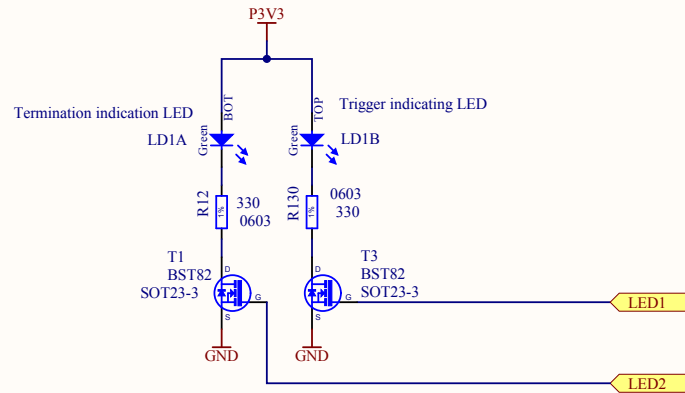
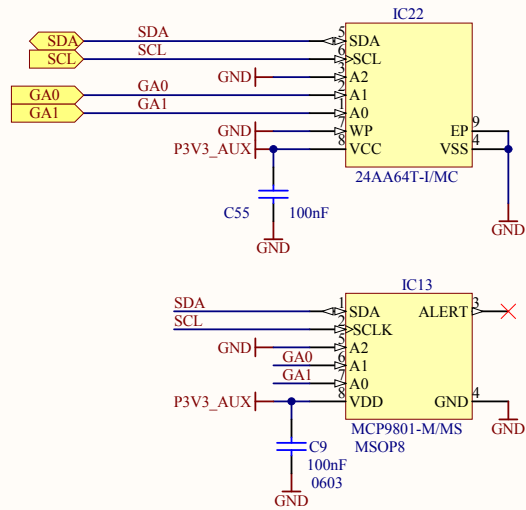
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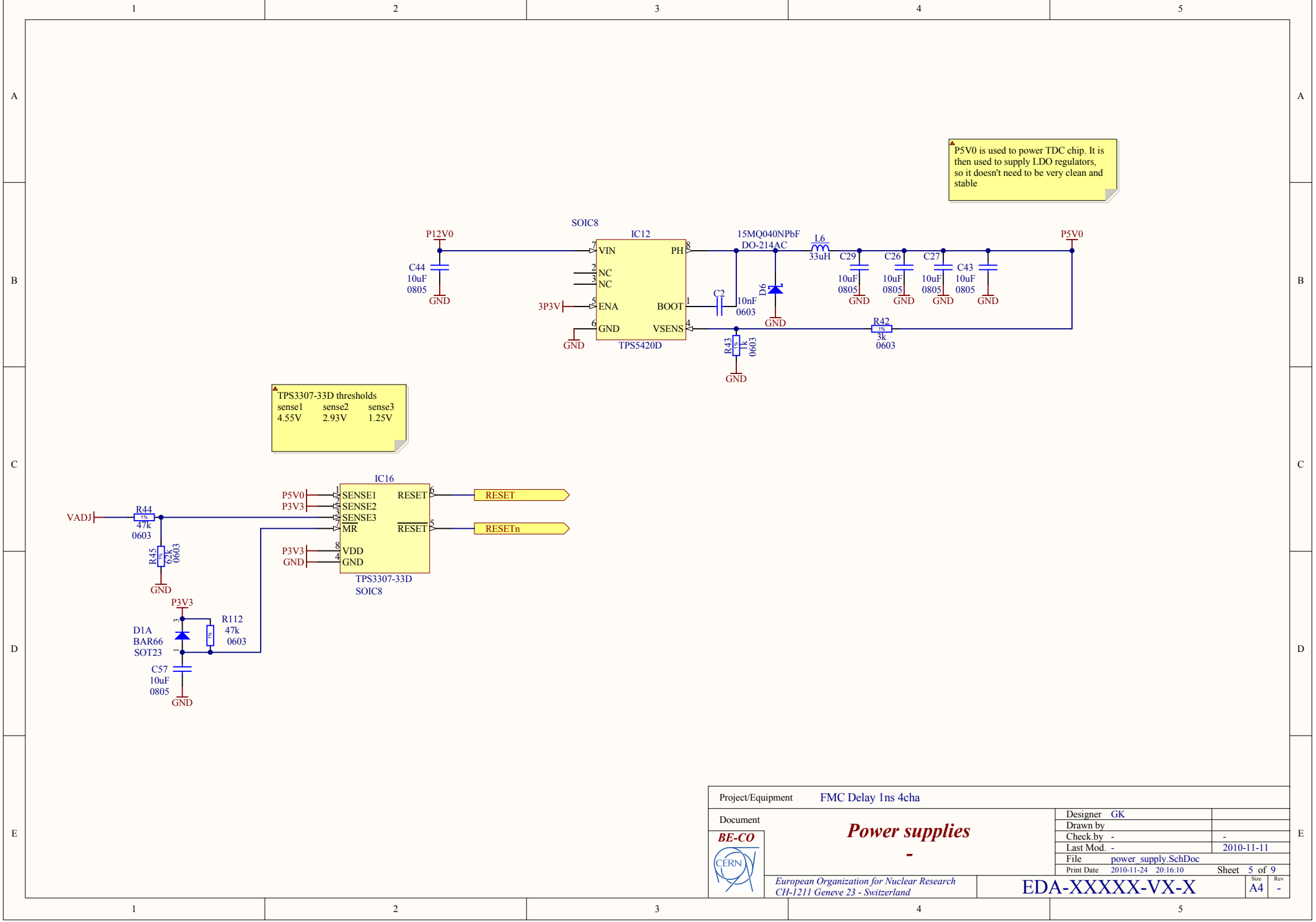


24AA64T = 1 0 1 0 0 GA0 GA1
 MCP9801 = 1 0 0 1 0 GA0 GA1

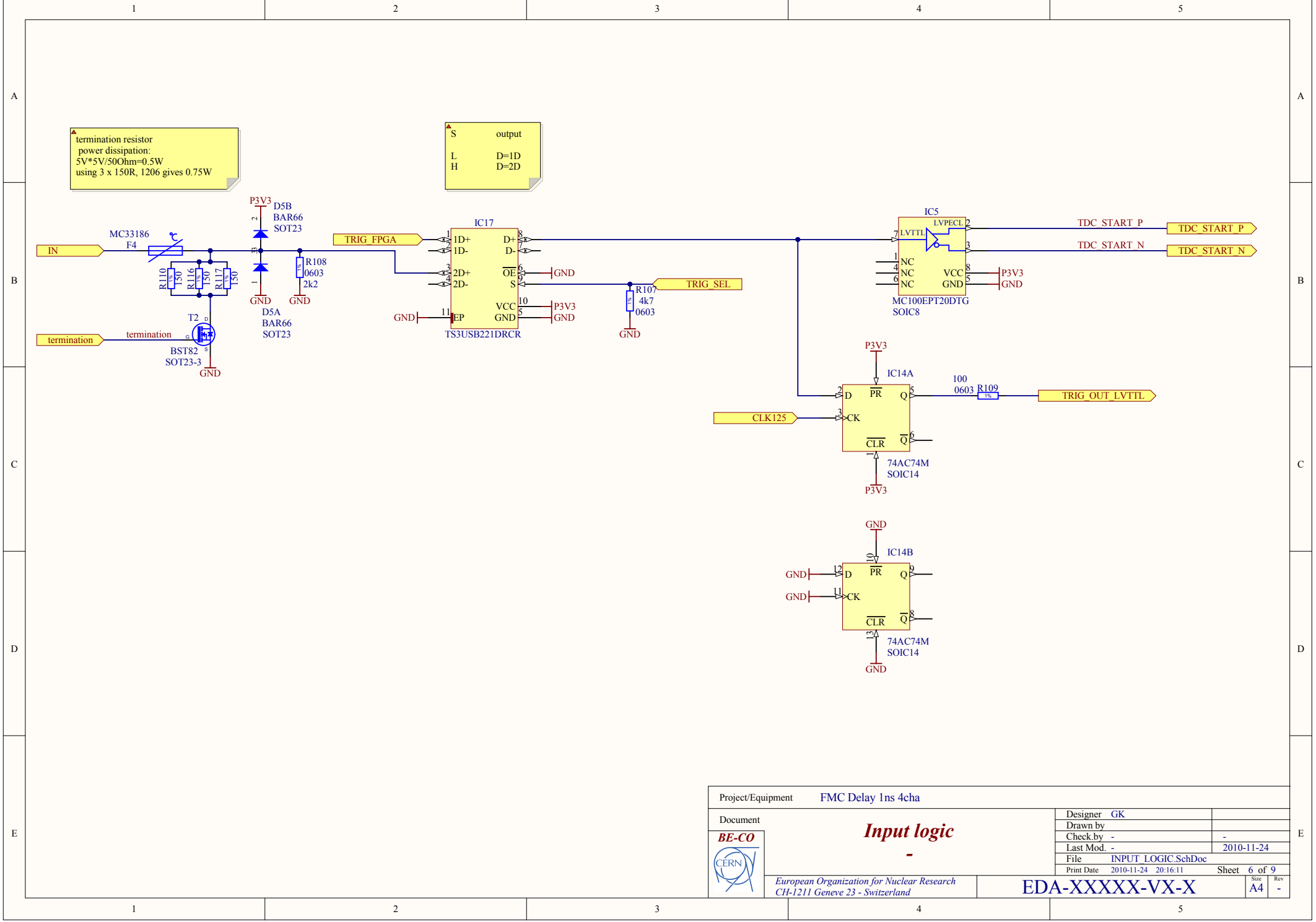
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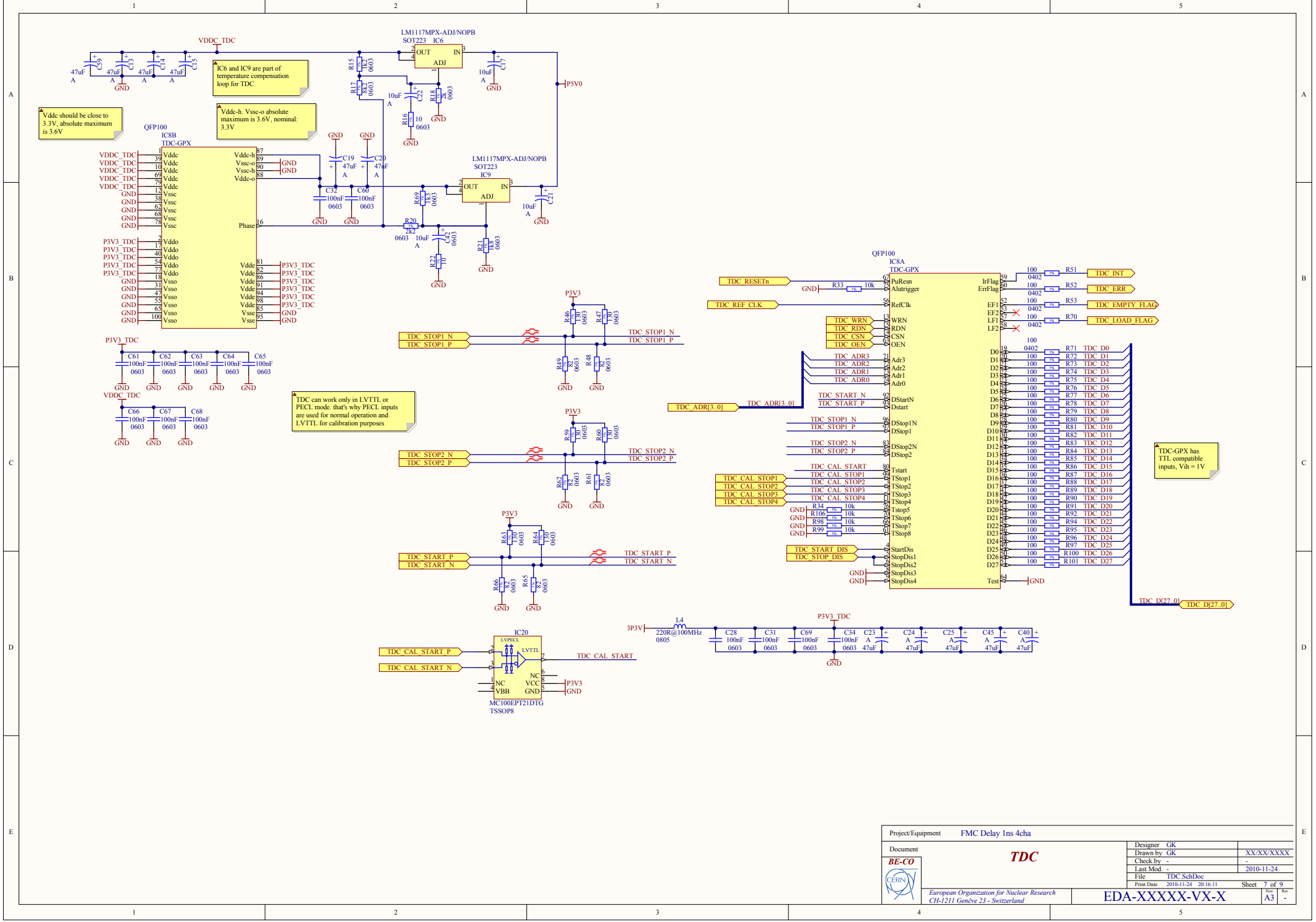
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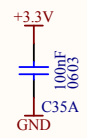
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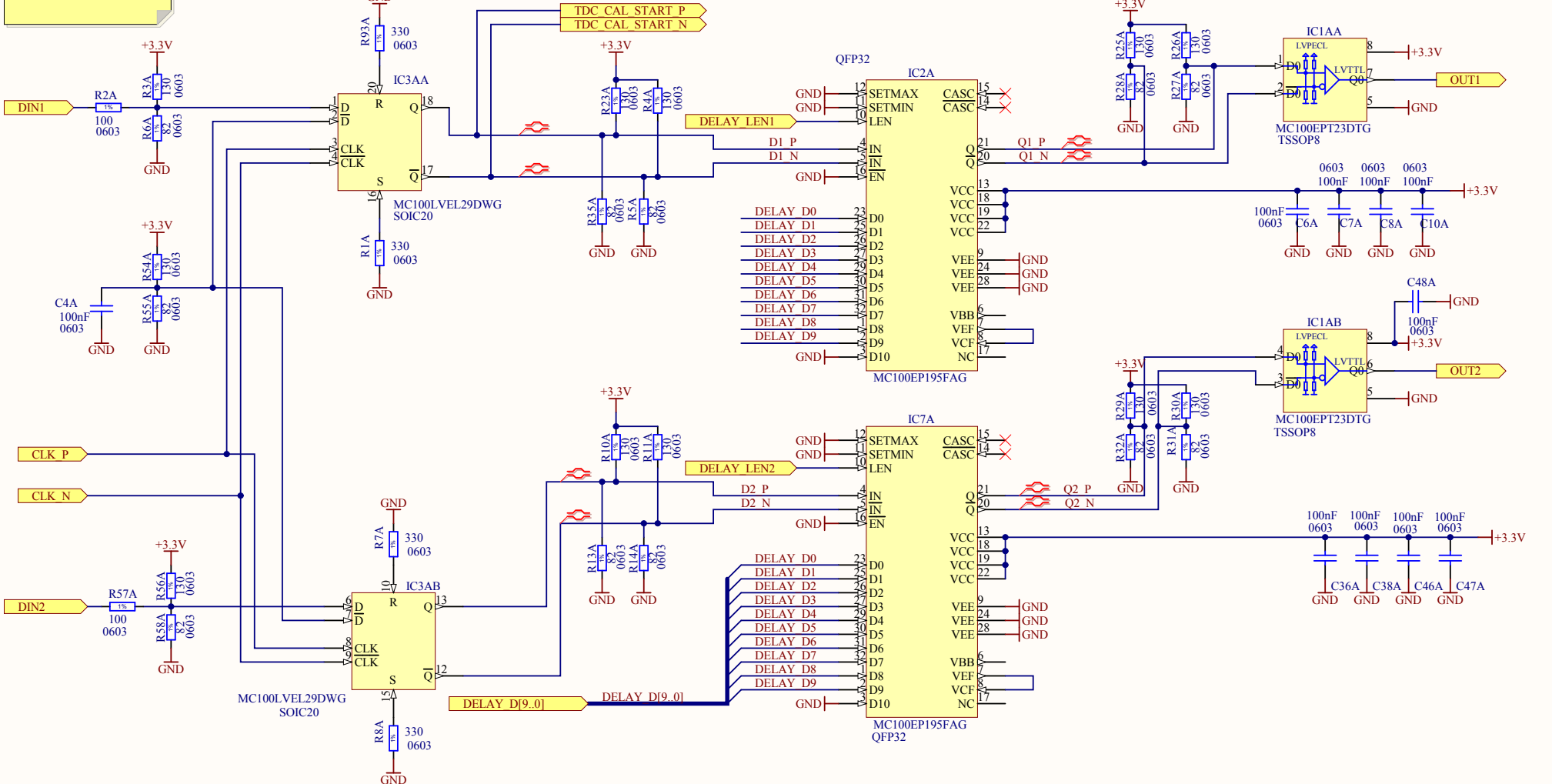
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		Sheet	6 of 9
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MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used



VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTTL Mode (Note 5)

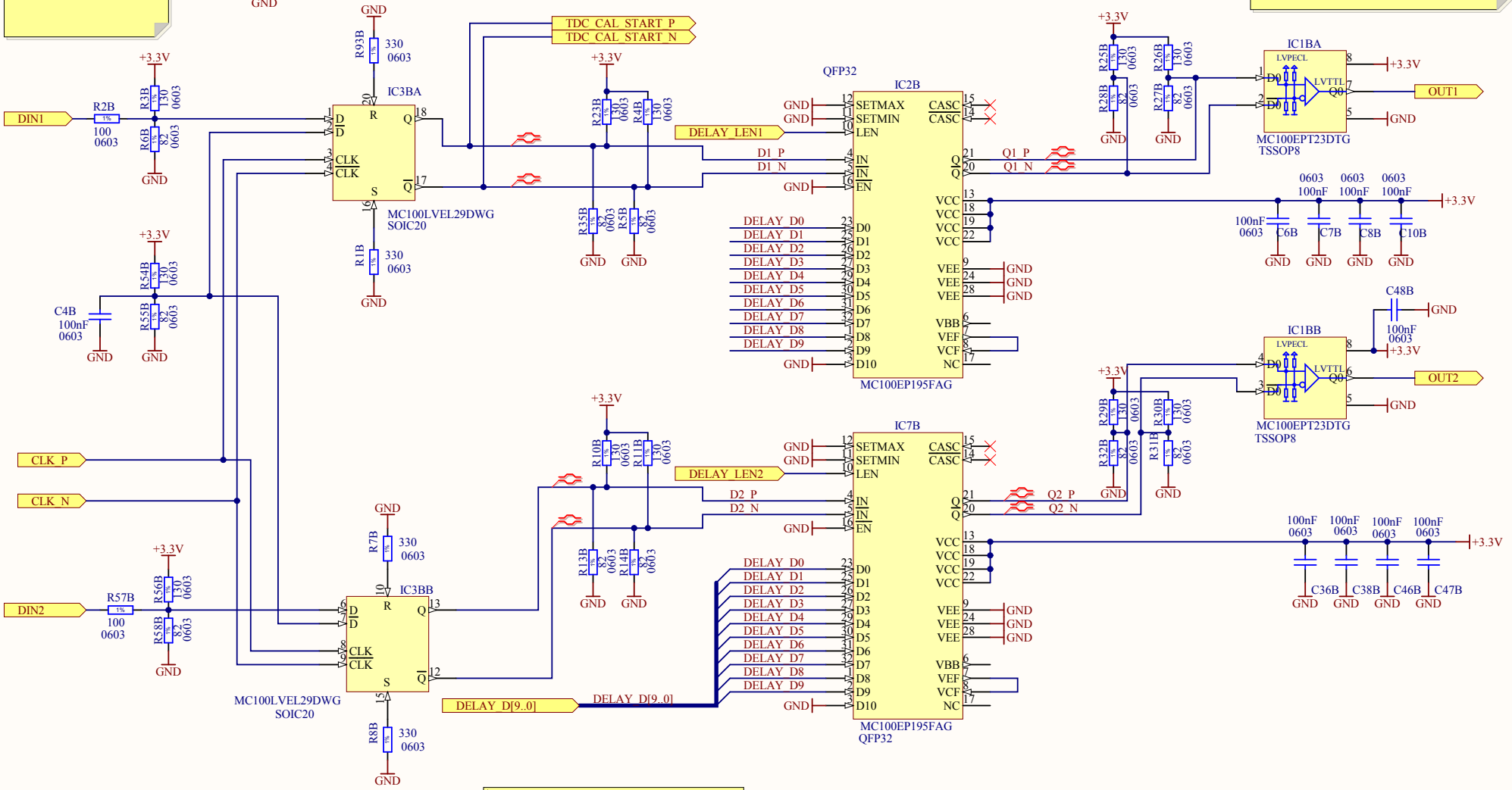


MC100LVEL family accepts LVDS levels at the inputs



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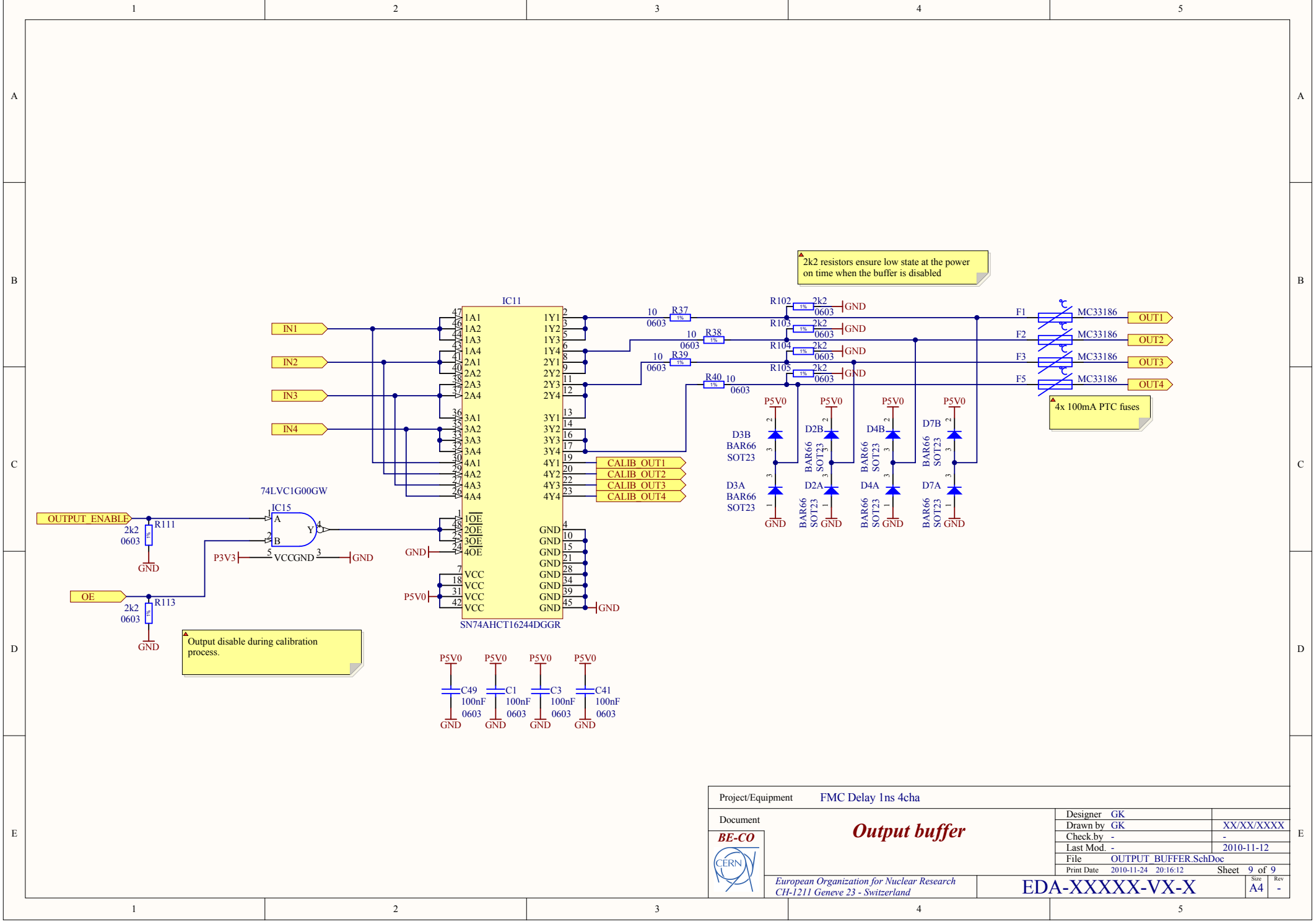
MC100LVEL input current is about 100..300uA
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Project/Equipment		FMC Delay 1ns 4cha	
Document		DELAY	
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		Size	Rev
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