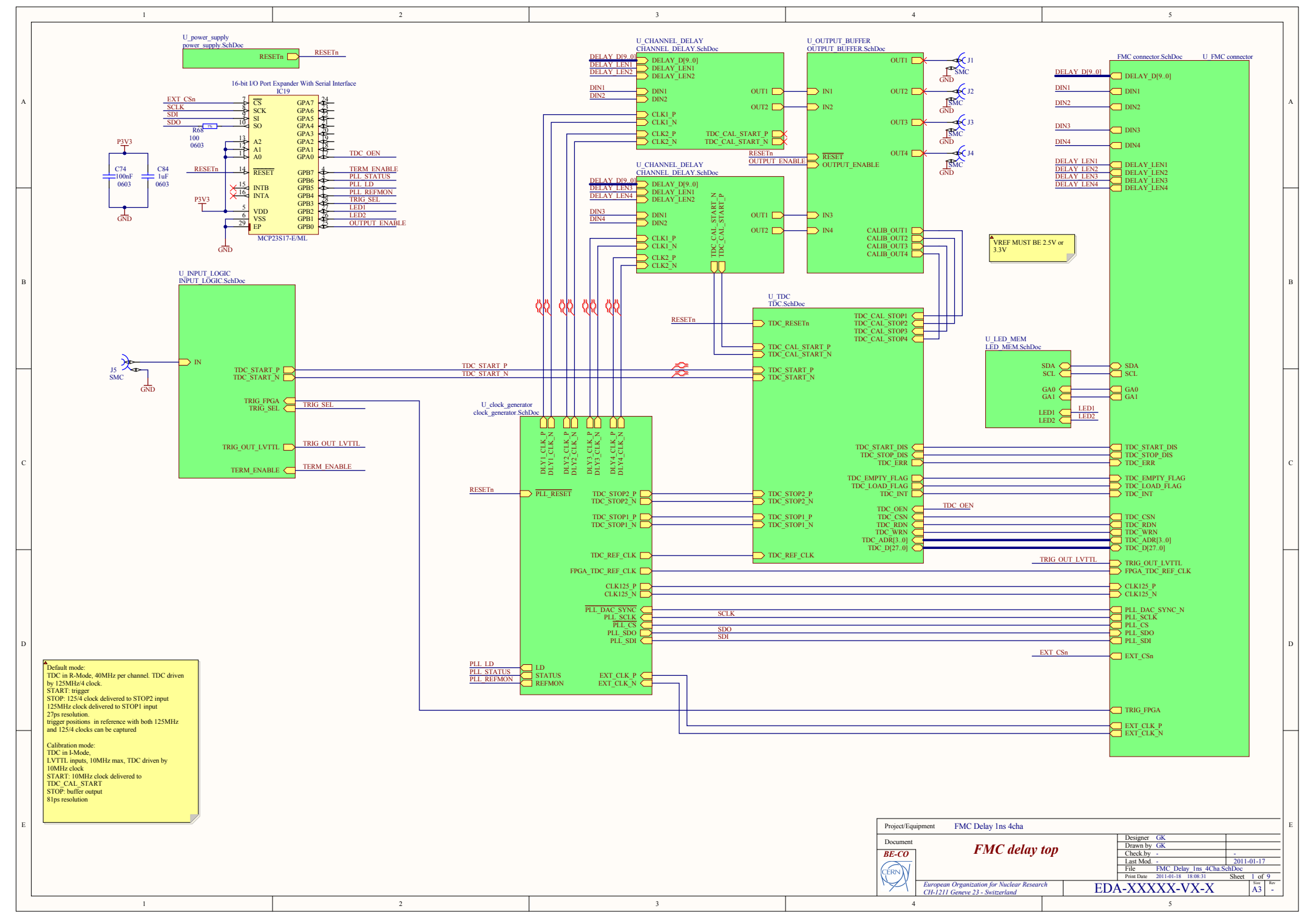
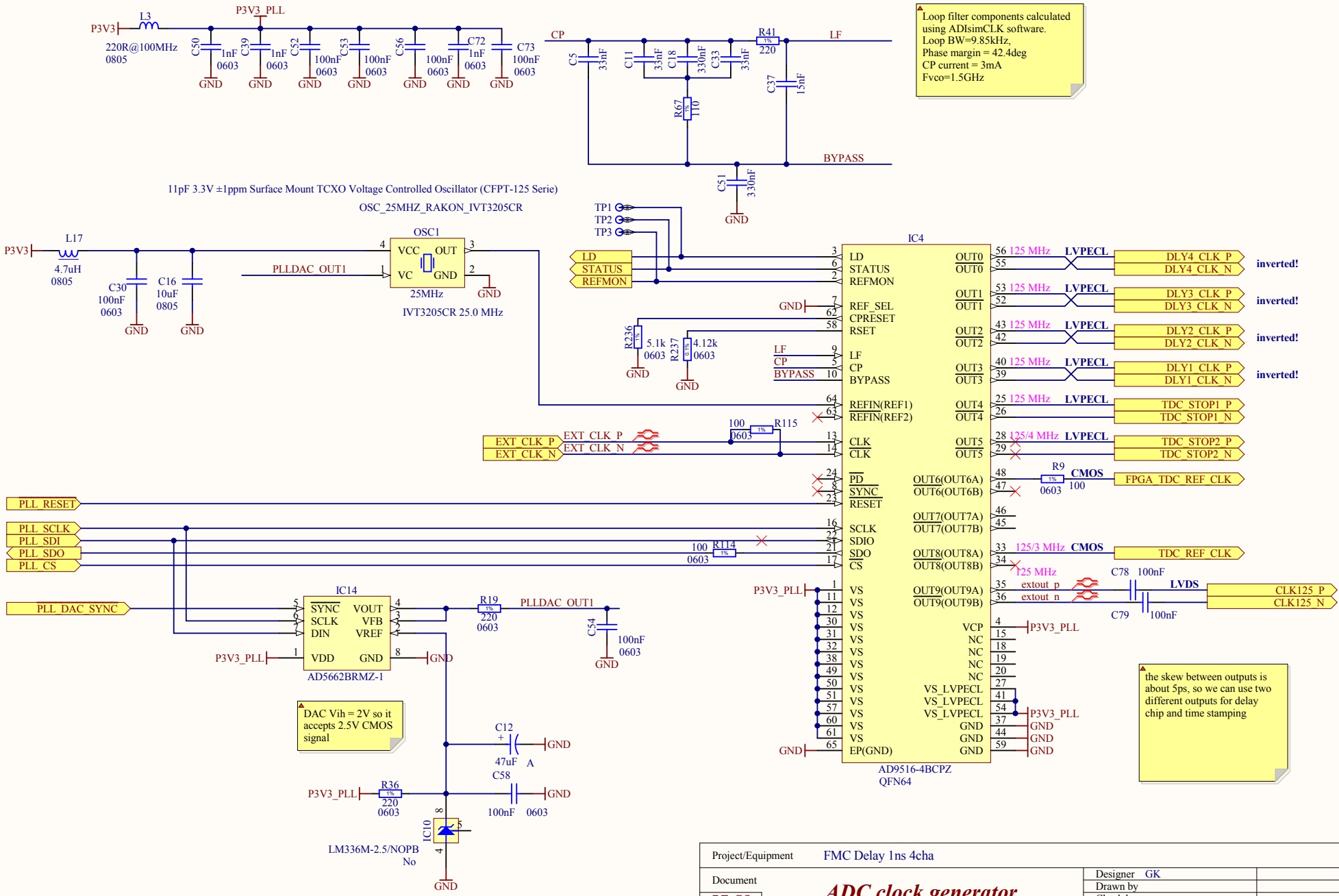
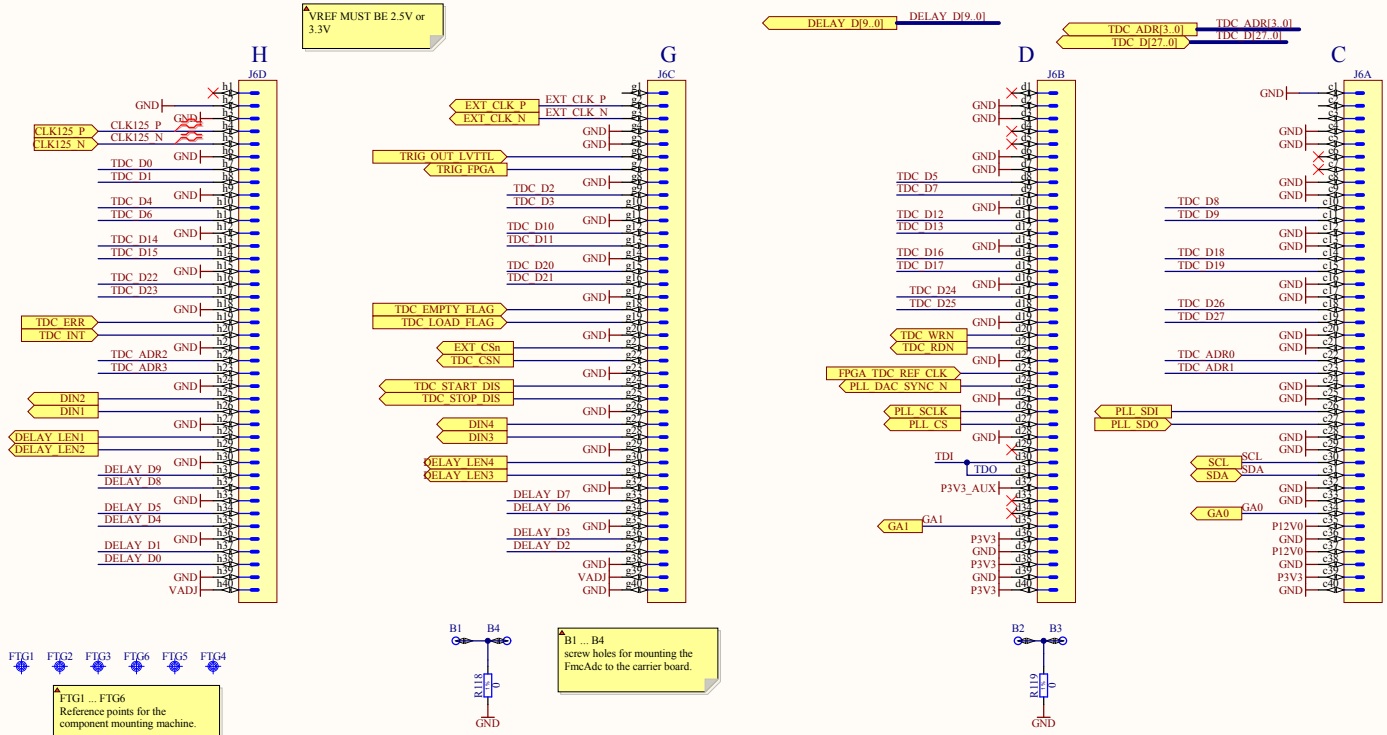

U_power_supply
power_supply.SchDoc
RESETn
16-bit I/O Port Expander With Serial Interface
IC19
MCP23S17-E/ML
U_CHANNEL_DELAY
CHANNEL_DELAY.SchDoc
U_OUTPUT_BUFFER
OUTPUT_BUFFER.SchDoc
FMC connector.SchDoc
U_FMC connector
U_INPUT_LOGIC
INPUT_LOGIC.SchDoc
U_TDC
TDC.SchDoc
U_LED_MEM
LED_MEM.SchDoc
U_clock_generator
clock_generator.SchDoc
VREF MUST BE 2.5V or 3.3V
Default mode:
TDC in R-Mode, 40MHz per channel. TDC driven by 125MHz/4 clock.
START: trigger
STOP: 125/4 clock delivered to STOP2 input
125MHz clock delivered to STOP1 input
27ps resolution.
trigger positions in reference with both 125MHz and 125/4 clocks can be captured
Calibration mode:
TDC in I-Mode,
LVTTL inputs, 10MHz max, TDC driven by 10MHz clock
START: 10MHz clock delivered to TDC_CAL_START
STOP: buffer output
81ps resolution
Project/Equipment
FMC Delay 1ns 4cha
Document
FMC delay top
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
Check.by -
Last Mod. -
2011-01-17
File FMC_Delay_1ns_4Cha.SchDoc
Print Date 2011-01-18 18:08:31
Sheet 1 of 9
EDA-XXXXX-VX-X
Size A3
Rev -


Loop filter components calculated using ADIsimCLK software.
Loop BW=9.85kHz,
Phase margin = 42.4deg
CP current = 3mA
Fvco=1.5GHz
11pF 3.3V ±1ppm Surface Mount TCXO Voltage Controlled Oscillator (CFPT-125 Serie)
OSC_25MHZ_RAKON_IVT3205CR
IVT3205CR 25.0 MHz
AD5662BRMZ-1
AD9516-4BCPZ
QFN64
LM336M-2.5/NOPB
DAC Vih = 2V so it accepts 2.5V CMOS signal
the skew between outputs is about 5ps, so we can use two different outputs for delay chip and time stamping
Project/Equipment FMC Delay 1ns 4cha
Document
ADC clock generator
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by
Check.by -
Last Mod. - 2011-01-17
File clock_generator.SchDoc
Print Date 2011-01-18 18:08:31
Sheet 2 of 9
EDA-XXXXX-VX-X
Size A4
Rev -

CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.

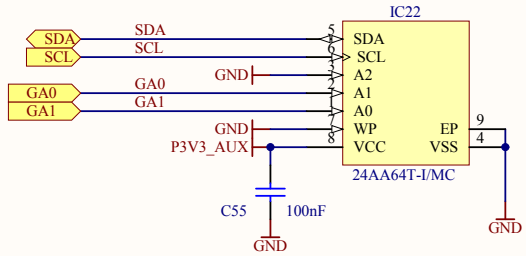
VREF MUST BE 2.5V or 3.3V

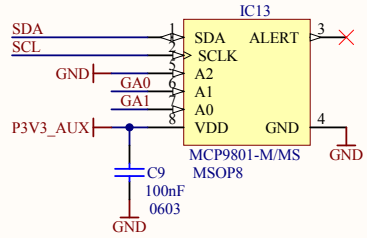


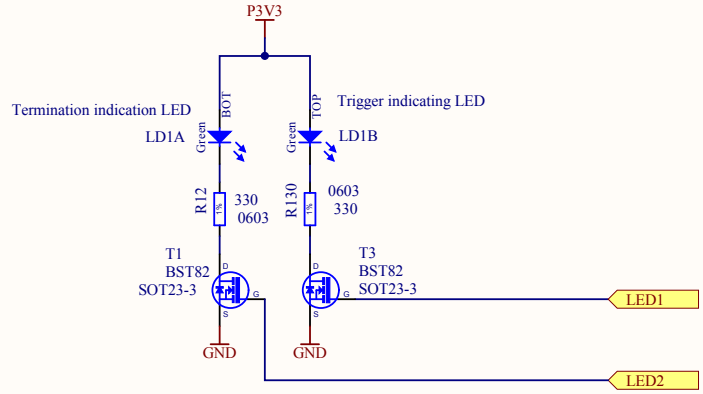
FTG1 ... FTG6
Reference points for the component mounting machine.

B1 ... B4
screw holes for mounting the FmcAdc to the carrier board.

Project/Equipment	FMC Delay 1ns 4cha		
Document	**FMC Connector**	Designer Greg Kasprowicz,	
BE-CO		Drawn by Greg Kasprowicz	10/07/2010
		Check.by M.C., T.W., E.B.	-
		Last Mod. -	2011-01-09
		File FMC connector.SchDoc	
		Print Date 2011-01-18 18:08:32	Sheet 3 of 9
European Organization for Nuclear Research CH-1211 Geneve 23 - SwitzerLA Pd	EDA-XXXXX-XX-X	Size A3	Rev -

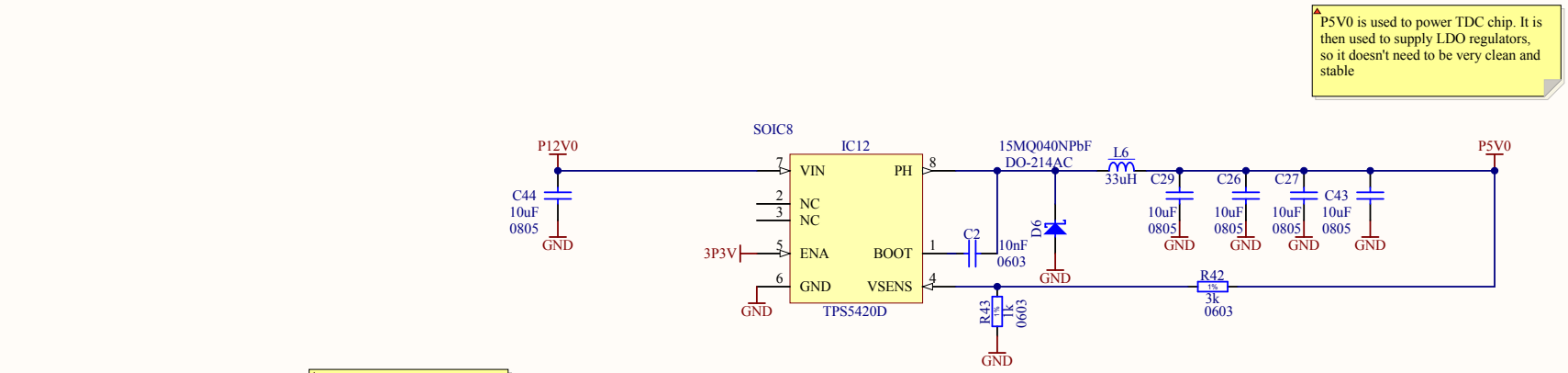


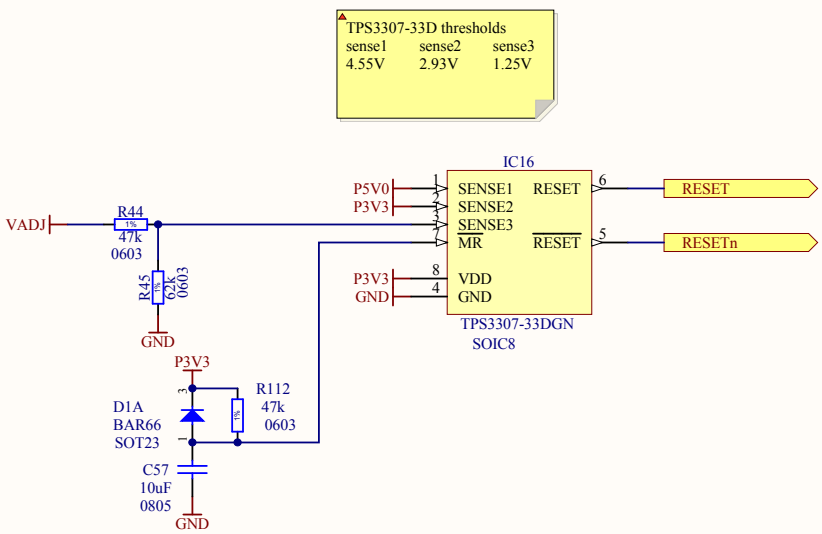




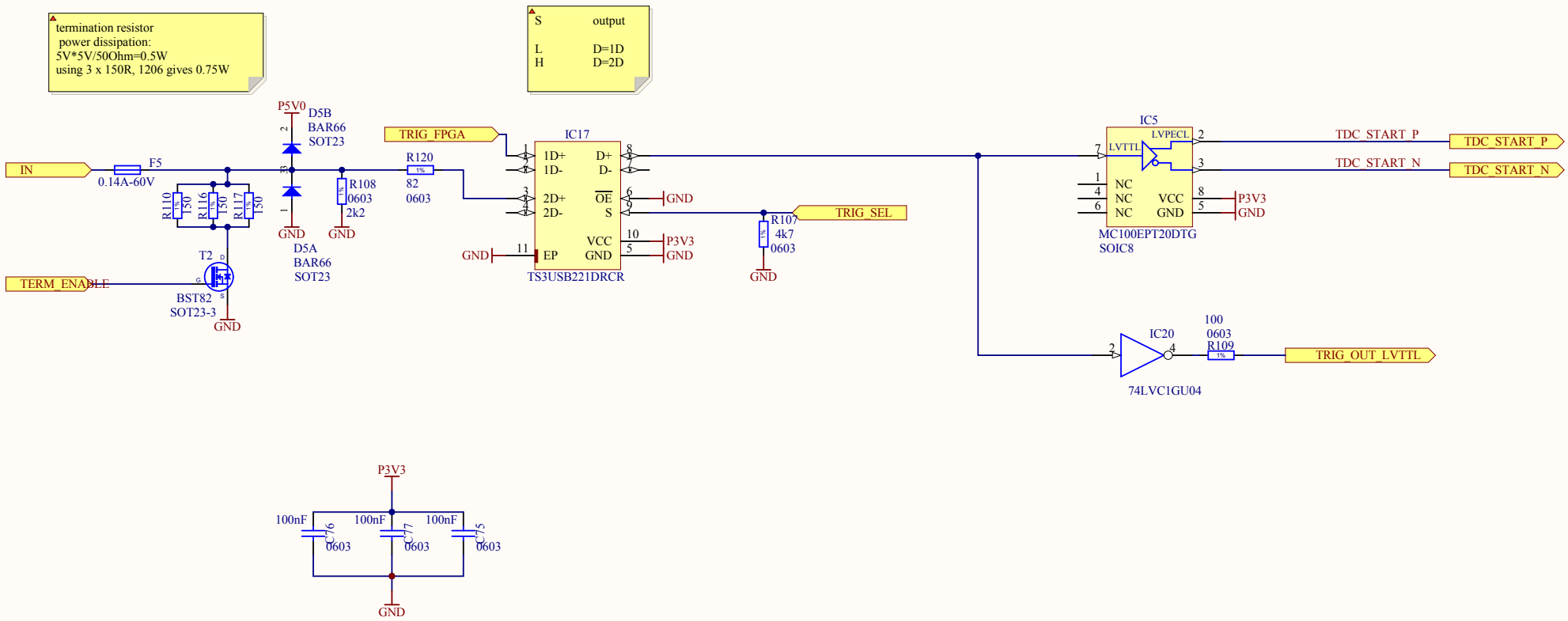
24AA64T = 1 0 1 0 0 GA0 GA1
MCP9801 = 1 0 0 1 0 GA0 GA1

Project/Equipment	FMC Delay 1ns 4cha		
Document	**LED and MEMORY**	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check.by -	-
		Last Mod. -	2010-12-03
		File LED_MEM.SchDoc	
		Print Date 2011-01-18 18:08:32	Sheet 4 of 9
BE-CO	*European Organization for Nuclear Research* *CH-1211 Geneve 23 - Switzerland*	EDA-XXXXX-VX-X	Size A4 / Rev -

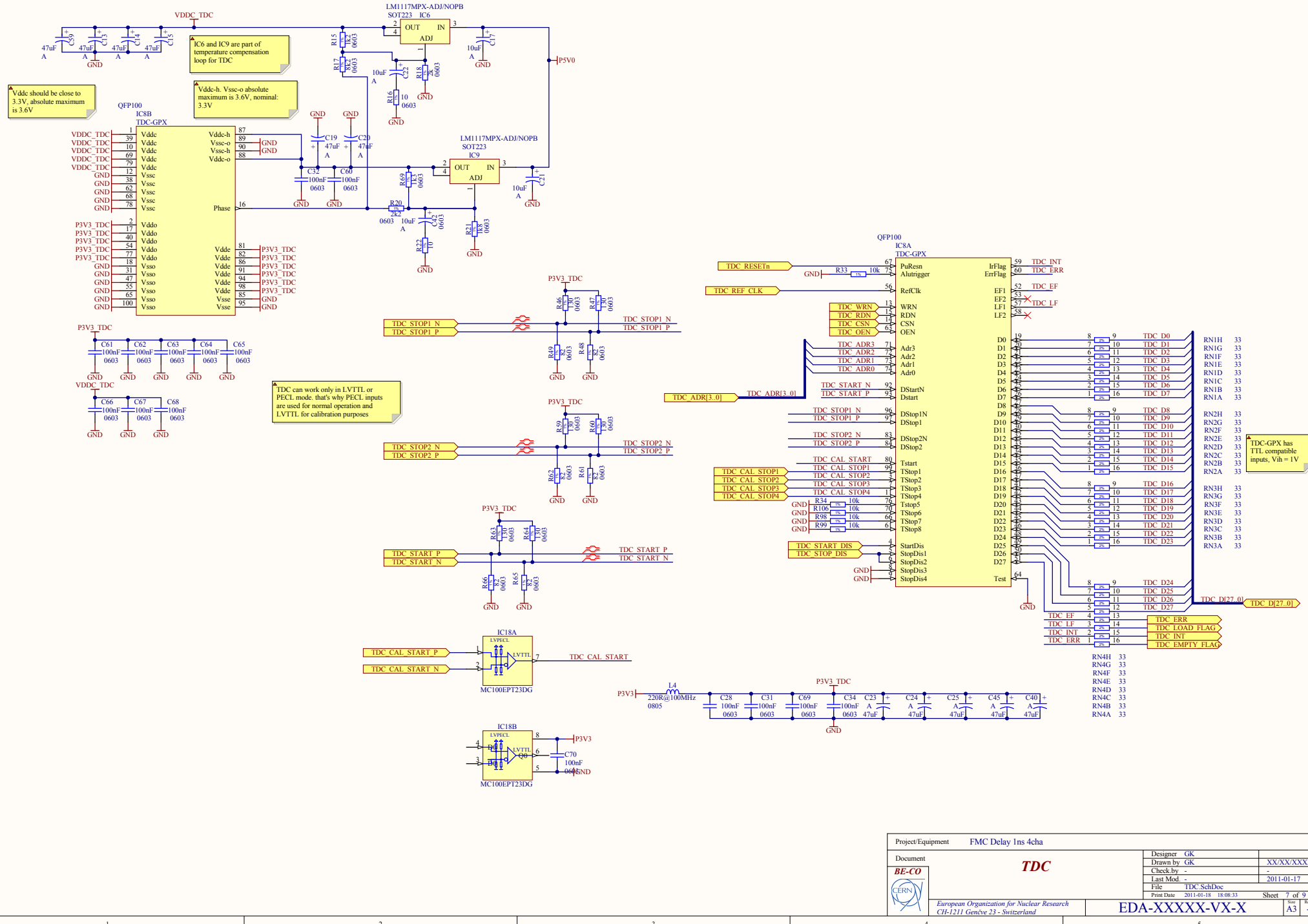




Project/Equipment	FMC Delay 1ns 4cha		
Document	**Power supplies** -	Designer GK	
		Drawn by	
		Check.by -	-
		Last Mod. -	2011-01-05
		File power_supply.SchDoc	
		Print Date 2011-01-18 18:08:32	Sheet 5 of 9
BE-CO CERN	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4 / Rev -



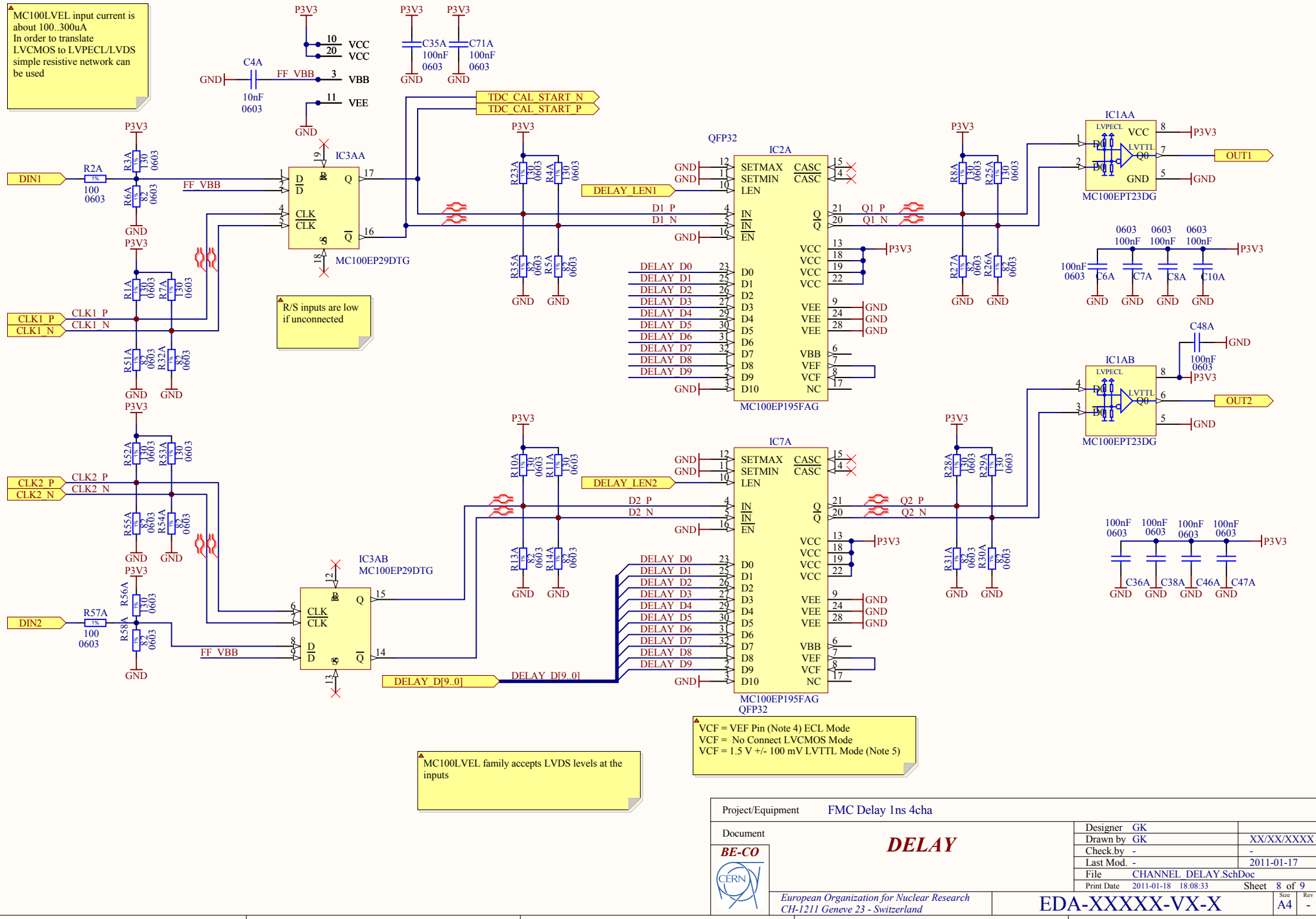
Project/Equipment	FMC Delay 1ns 4cha		
Document	**Input logic** -	Designer GK	
		Drawn by	
		Check.by -	-
		Last Mod. -	2011-01-17
		File INPUT_LOGIC.SchDoc	
		Print Date 2011-01-18 18:08:32	Sheet 6 of 9
BE-CO	European Organization for Nuclear Research, CH-1211 Geneve 23 - Switzerland	EDA-XXXXX-VX-X	Size A4 / Rev -

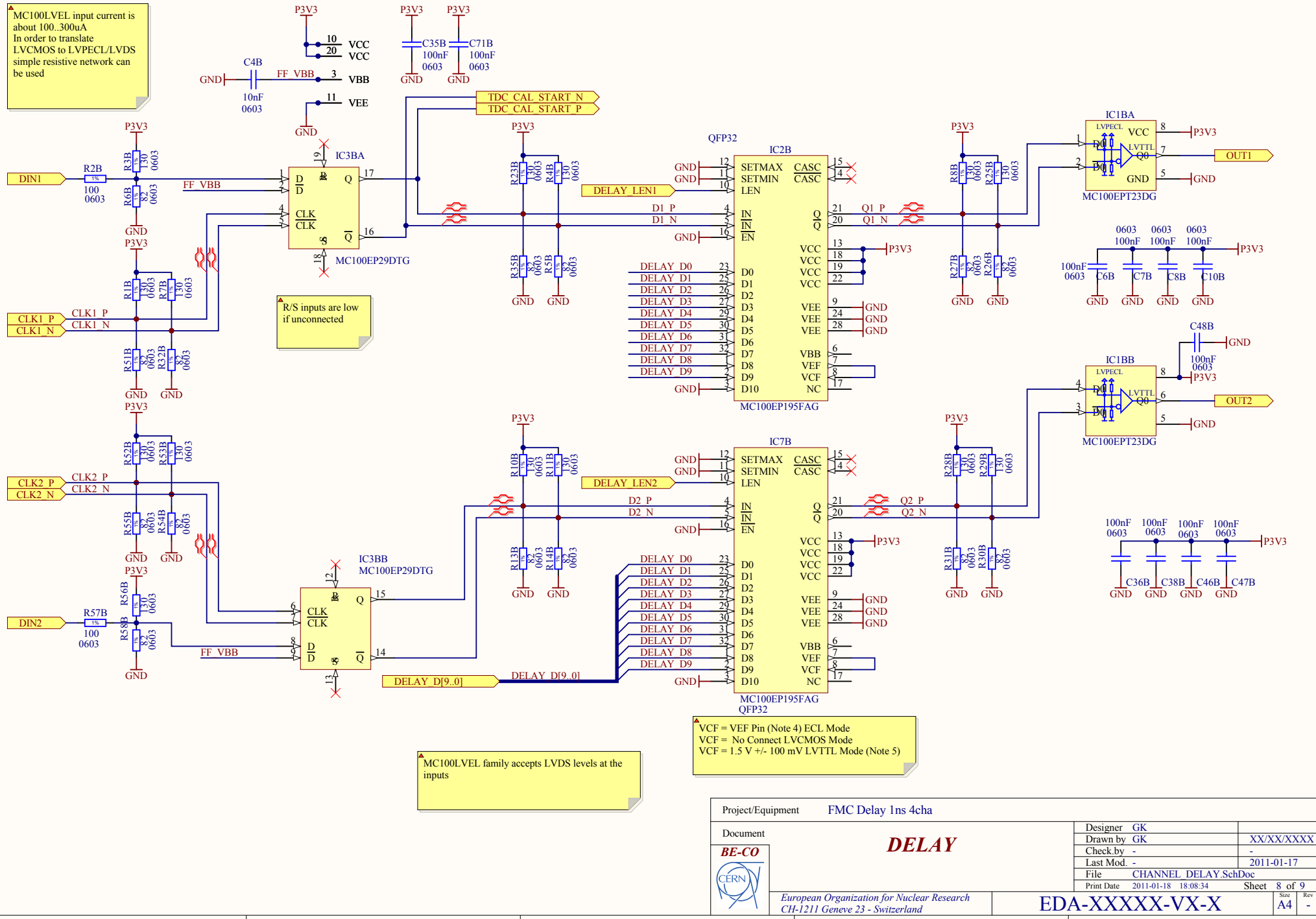


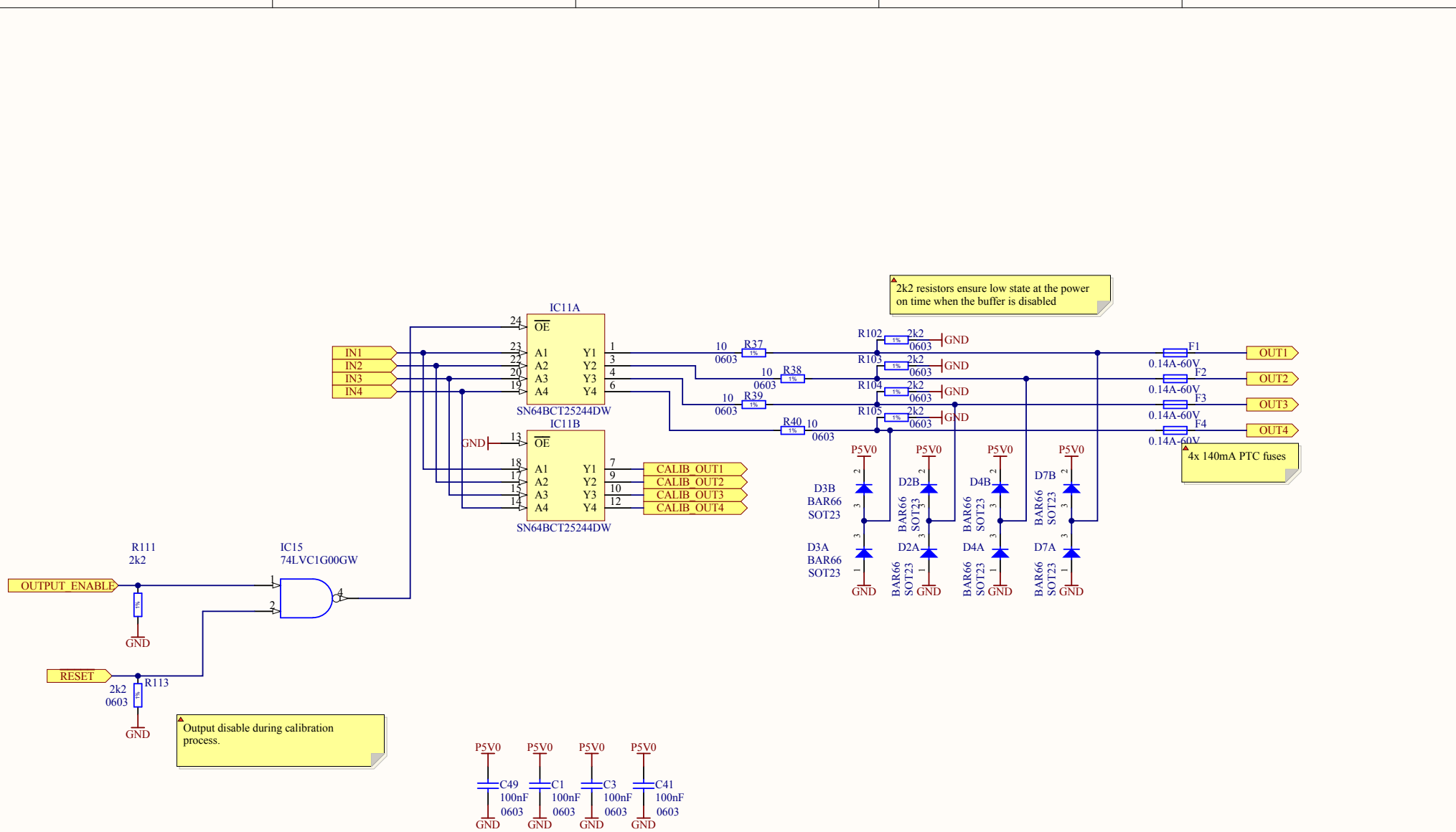
Project/Equipment	FMC Delay 1ns 4cha
Document	TDC
Designer	GK
Drawn by	GK
Check.by	-
Last Mod.	-
File	TDC.SchDoc
Print Date	2011-01-18 18:08:33
Sheet	7 of 9
Size	A3
Rev	-
	XX/XX/XXXX
	2011-01-17
	EDA-XXXXX-VX-X

BE-CO

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland


MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used
P3V3
VCC
VBB
VEE
GND
C4A
10nF
0603
FF_VBB
C35A
C71A
100nF
0603
TDC_CAL_START_N
TDC_CAL_START_P
IC3AA
MC100EP29DTG
DIN1
R2A
100
CLK1_P
CLK1_N
R/S inputs are low if unconnected
QFP32
IC2A
MC100EP195FAG
DELAY_LEN1
DELAY_D0
DELAY_D1
DELAY_D2
DELAY_D3
DELAY_D4
DELAY_D5
DELAY_D6
DELAY_D7
DELAY_D8
DELAY_D9
D1_P
D1_N
Q1_P
Q1_N
IC1AA
MC100EPT23DG
OUT1
IC1AB
OUT2
CLK2_P
CLK2_N
DIN2
R57A
IC3AB
DELAY_LEN2
D2_P
D2_N
Q2_P
Q2_N
IC7A
DELAY_D[9..0]
VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTL Mode (Note 5)
MC100LVEL family accepts LVDS levels at the inputs
Project/Equipment
FMC Delay 1ns 4cha
Document
DELAY
BE-CO
CERN
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
XX/XX/XXXX
Check.by -
Last Mod. -
2011-01-17
File CHANNEL_DELAY.SchDoc
Print Date 2011-01-18 18:08:33
Sheet 8 of 9
EDA-XXXXX-VX-X
Size A4
Rev -


MC100LVEL input current is about 100..300uA
In order to translate LVCMOS to LVPECL/LVDS simple resistive network can be used
P3V3
VCC
VBB
VEE
GND
C4B
10nF
0603
FF_VBB
C35B
C71B
100nF
0603
TDC_CAL_START_N
TDC_CAL_START_P
IC3BA
MC100EP29DTG
DIN1
R2B
100
CLK1_P
CLK1_N
R/S inputs are low if unconnected
QFP32
IC2B
MC100EP195FAG
DELAY_LEN1
D1_P
D1_N
DELAY_D0
DELAY_D1
DELAY_D2
DELAY_D3
DELAY_D4
DELAY_D5
DELAY_D6
DELAY_D7
DELAY_D8
DELAY_D9
Q1_P
Q1_N
IC1BA
MC100EPT23DG
OUT1
IC1BB
OUT2
CLK2_P
CLK2_N
DIN2
R57B
IC3BB
MC100EP29DTG
DELAY_LEN2
D2_P
D2_N
IC7B
MC100EP195FAG
QFP32
Q2_P
Q2_N
DELAY_D[9..0]
VCF = VEF Pin (Note 4) ECL Mode
VCF = No Connect LVCMOS Mode
VCF = 1.5 V +/- 100 mV LVTTL Mode (Note 5)
MC100LVEL family accepts LVDS levels at the inputs
Project/Equipment
FMC Delay 1ns 4cha
Document
DELAY
BE-CO
CERN
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer GK
Drawn by GK
XX/XX/XXXX
Check.by -
Last Mod. -
2011-01-17
File CHANNEL_DELAY.SchDoc
Print Date 2011-01-18 18:08:34
Sheet 8 of 9
EDA-XXXXX-VX-X
Size A4
Rev -



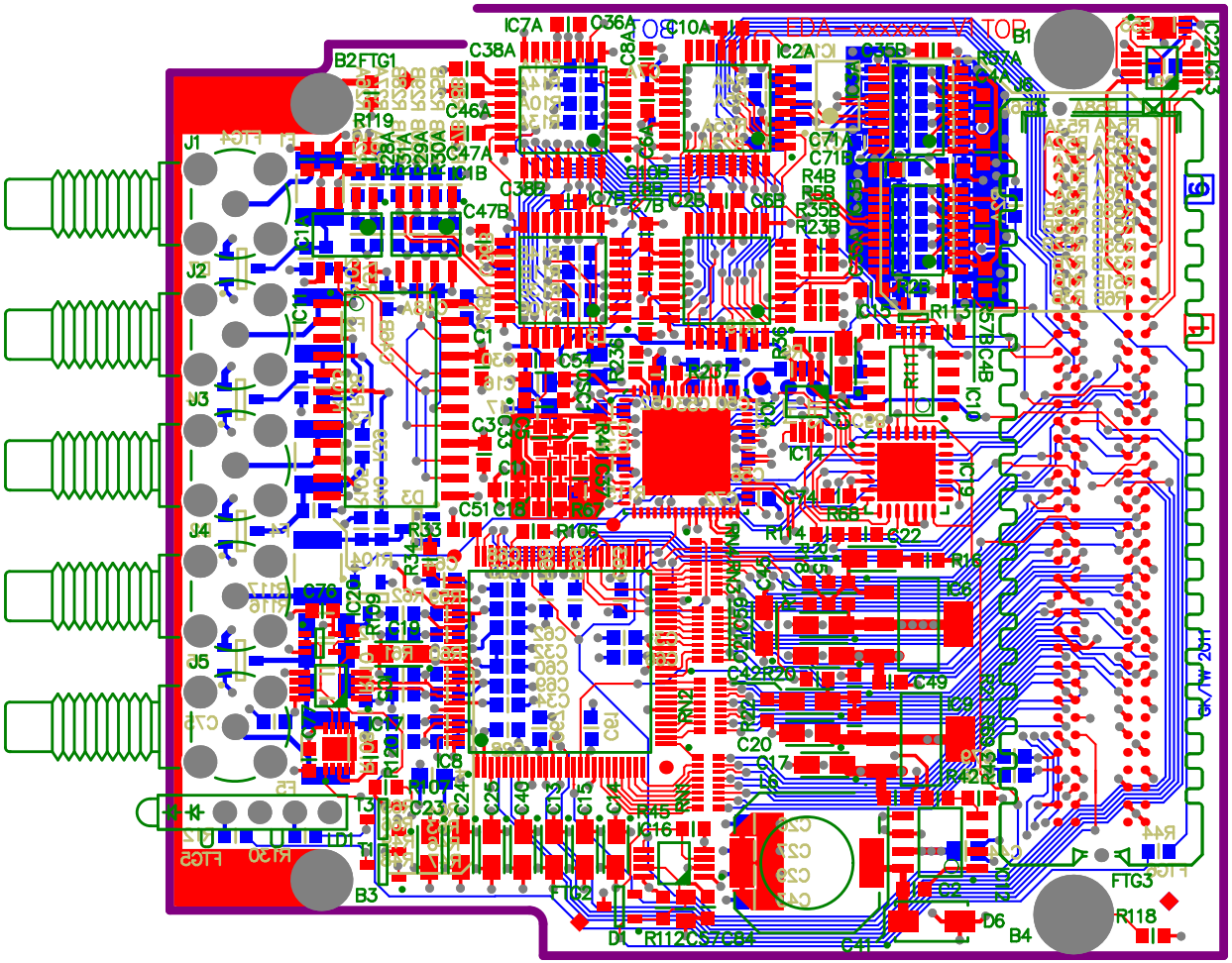
Project/Equipment	FMC Delay 1ns 4cha		
Document	**Output buffer**	Designer GK	
		Drawn by GK	XX/XX/XXXX
		Check.by -	-
		Last Mod. -	2011-01-17
		File OUTPUT_BUFFER.SchDoc	
		Print Date 2011-01-18 18:08:34	Sheet 9 of 9

BE-CO

European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

EDA-XXXXX-VX-X

Size A4 | Rev -


Bottom Overlay
Top Overlay
Top Layer
1
Bottom Layer
6